SDAS227A - JUNE 1984 - REVISED JANUARY 1995

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic
 - SN74ALS666 . . . True Outputs
 - SN74ALS667 . . . Inverted Outputs
- Preset and Clear Inputs
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

description

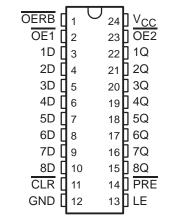
These 8-bit D-type transparent latches are designed specifically for storing the contents of the input data bus, plus reading back the stored data onto the input data bus. In addition, they provide a 3-state buffer-type output and are easily utilized in bus-structured applications.

While the latch enable (LE) is high, the Q outputs of the SN74ALS666 follow the data (D) inputs. The $\overline{\mathbb{Q}}$ outputs of the SN74ALS667 provide the inverse of the data applied to its D inputs. The Q or $\overline{\mathbb{Q}}$ output of both devices is in the high-impedance state if either output-enable ($\overline{\mathsf{OE1}}$ or $\overline{\mathsf{OE2}}$) input is at a high logic level.

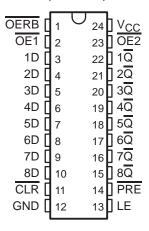
Read back is provided through the read-back control (OERB) input. When OERB is taken low, the data present at the output of the data latches passes back onto the input data bus. When OERB is taken high, the output of the data latches is isolated from the D inputs. OERB does not affect the internal operation of the latches; however, caution should be exercised to avoid a bus conflict.

The SN74ALS666 and SN74ALS667 are characterized for operation from 0°C to 70°C.

SN74ALS666 . . . DW OR NT PACKAGE (TOP VIEW)

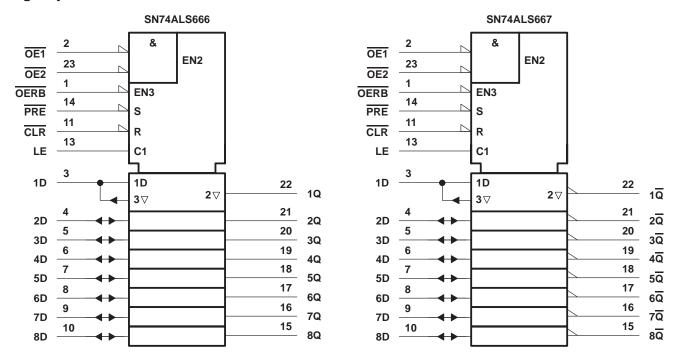


SN74ALS667 . . . DW OR NT PACKAGE (TOP VIEW)



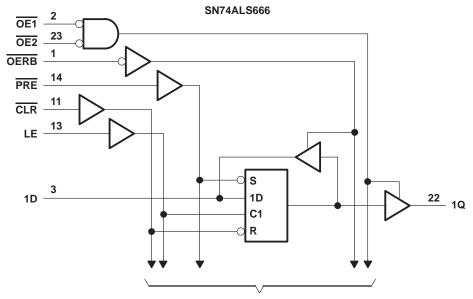
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logic symbols†

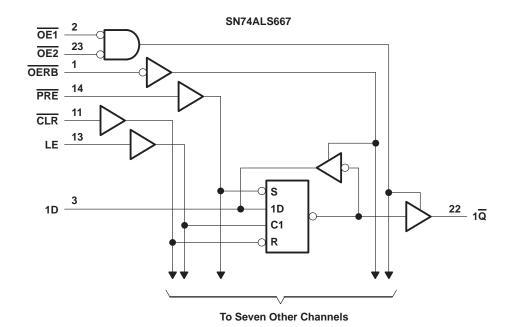


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

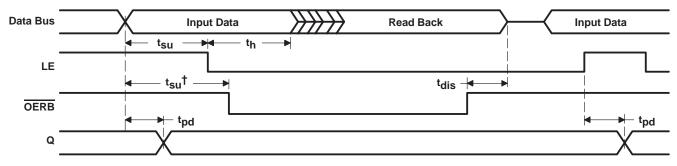


To Seven Other Channels



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timing diagram



 $\overline{\text{CLR}} = \text{H}, \overline{\text{PRE}} = \text{H}, \overline{\text{OE1}} = \text{L}, \overline{\text{OE2}} = \text{L}.$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	7 V
Input voltage, V _I (all inputs except D inputs)	7 V
Voltage applied to D inputs and to disabled 3-state outputs	5.5 V
Operating free-air temperature range, T _A : SN74ALS666, SN74ALS667	0°C to 70°C
Storage temperature range	–65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

				74ALS60 74ALS60		UNIT
			MIN	NOM	MAX	
VCC	Supply voltage		4.5	5	5.5	V
VIH	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
1	High-level output current	Q			-2.6	mA
ЮН	nigh-level output current	D			-0.4	IIIA
1	Low-level output current	Q			24	mA
lOL	Low-level output current	D			8	IIIA
		LE high	10			
t _W	Pulse duration	CLR low	10			ns
		PRE low	10			
	Satura tima	Data before LE↓	10			no
t _{su}	Setup time	Data before OERB↓	10			ns
th	Hold time, data after LE↓		5			ns
TA	Operating free-air temperature	0		70	°C	

[†] This setup time ensures the read-back circuit does not create a conflict on the input data bus.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CON	TEST CONDITIONS					
				MIN	MIN TYPT			
٧ıK		$V_{CC} = 4.5 V,$	$I_{I} = -18 \text{ mA}$			-1.2	V	
\/ - · ·	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V	
VOH	Q or Q	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$	2.4	3.2		V	
	D inputs	V _{CC} = 4.5 V	I _{OL} = 4 mA		0.25	0.4		
\/ a.	Dilipuis	∨CC = 4.5 V	$I_{OL} = 8 \text{ mA}$		0.35	0.5	V	
VOL	0 0 0	V _{CC} = 4.5 V	I _{OL} = 12 mA		0.25	0.4	V	
	Q or Q	∨CC = 4.5 V	I _{OL} = 24 mA		0.35	0.5		
lozh	Q or Q	$V_{CC} = 5.5 V$,	$V_0 = 2.7 \text{ V}$			20	μΑ	
lozL	Q or Q	$V_{CC} = 5.5 V$,	V _O = 0.4 V			-20	μΑ	
ij	D inputs	V _{CC} = 5.5 V	V _I = 5.5 V			0.1	mA	
	All others	vCC = 2:2 v	V _I = 7 V			0.1	IIIA	
1	D inputs‡	V _{CC} = 5.5 V,	V _I = 2.7 V			20		
lН	All others	vCC = 5.5 v,	V = 2.7 V			20	μΑ	
1	D inputs‡	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1	mA	
II∟	All others	S VCC = 3.3 V, V = 0.4 V				-0.1	IIIA	
IO§		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	mA	
			Q outputs high		25	50		
	SN74ALS666	<u>V_{CC} =</u> 5.5 V, OERB high	Q outputs low		40	73		
		OEKB High	Q outputs disabled		30	55		
ICC		V 55V	Q outputs high		25	50	mA	
	SN74ALS667	<u>VCC =</u> 5.5 V, OERB high	Q outputs low		45	79)	
			Q outputs disabled		30	60		

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

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switching characteristics (see Figure 1)

PARAMETER	FROM	то	V _{CC} = 4.5 C _L = 50 pF T _A = MIN to	UNIT	
	(INPUT)	(OUTPUT)	SN74A		
			MIN	MAX	
t _{PLH}	D		3	14	ns
^t PHL	ט	Q	4	18	115
t _{PLH}	LE		6	21	ns
^t PHL	LL	Q	8	27	115
† D	CLR	Q	9	29	ns
^t PHL	CLR	D	11	32	115
t _{PLH}	PRE	Q	7	22	ns
^t PHL	PRE	D	9	28	115
. +	OERB	D	4	21	
t _{en} ‡	OE1, OE2	Q	4	21	ns
t _{dis} §	OERB	D	1	14	
^l dis ³	OE1, OE2	Q	1	14	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM	то	V _{CC} = 4.5 C _L = 50 pF T _A = MIN to	UNIT	
.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	(INPUT)	(OUTPUT)	SN74A		
			MIN	MAX	
t _{PLH}	D	Q	6	20	ns
^t PHL	U	Q	4	15	113
t _{PLH}	LE	ā	9	28	ns
t _{PHL}	LL	Q	7	22	115
4		ā	7	24	
^t PHL	CLR	D	8	26	ns
t _{PLH}	PRE	Q	8	25	ns
t _{PHL}	PRE	D	9	28	115
. +	OERB	D	4	21	
t _{en} ‡	OE1, OE2	Q	4	21	ns
t _{dis} §	OERB	D	1	14	20
^t dis ³	OE1, OE2	Q	1	14	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



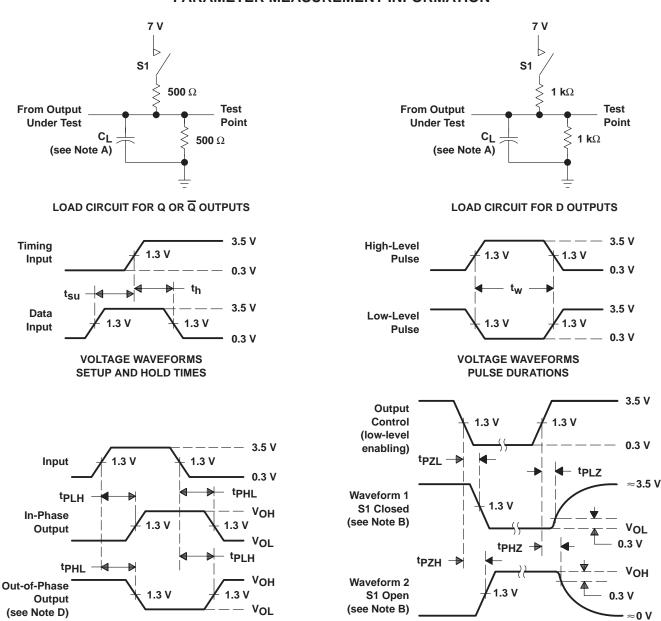
 $t_{en} = t_{PZH} \text{ or } t_{PZL}$ $t_{dis} = t_{PHZ} \text{ or } t_{PLZ}$

 $t_{en} = t_{PZH} \text{ or } t_{PZL}$ $t_{dis} = t_{PHZ} \text{ or } t_{PLZ}$

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
- D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

Figure 1. Load Circuits and Voltage Waveforms





28-Aug-2010

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74ALS666DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS666DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS666DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS666DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS666DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS666DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS666NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS666NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS667DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS667DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS667DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS667NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS667NT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available
SN74ALS667NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

28-Aug-2010

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS666DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS666DWR	SOIC	DW	24	2000	346.0	346.0	41.0

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

The 28 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



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