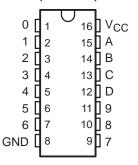
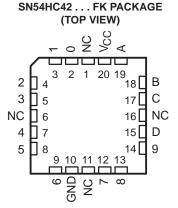
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 14 ns
- ±4-mA Output Drive at 5 V

SN54HC42...J OR W PACKAGE SN74HC42...D, N, OR NS PACKAGE (TOP VIEW)



- Low Input Current of 1 μA Max
- Full Decoding of Input Logic
- All Outputs Are High for Invalid BCD Conditions
- Also for Applications as 3-Line to 8-Line Decoders



NC - No internal connection

description/ordering information

These decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all inputs remain off for all invalid input conditions.

ORDERING INFORMATION

| TA | PACKAG | GE [†] | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|-----------------|--------------------------|---------------------|
| | PDIP – N | Tube of 25 | SN74HC42N | SN74HC42N |
| | | Tube of 40 | SN74HC42D | |
| -40°C to 85°C | SOIC - D | Reel of 2500 | SN74HC42DR | HC42 |
| | | Reel of 250 | SN74HC42DT | |
| | SOP - NS | Reel of 2000 | SN74HC42NSR | HC42 |
| | CDIP – J | Tube of 25 | SNJ54HC42J | SNJ54HC42J |
| –55°C to 125°C | CFP – W | Tube of 150 | SNJ54HC42W | SNJ54HC42W |
| | LCCC - FK | Tube of 55 | SNJ54HC42FK | SNJ54HC42FK |

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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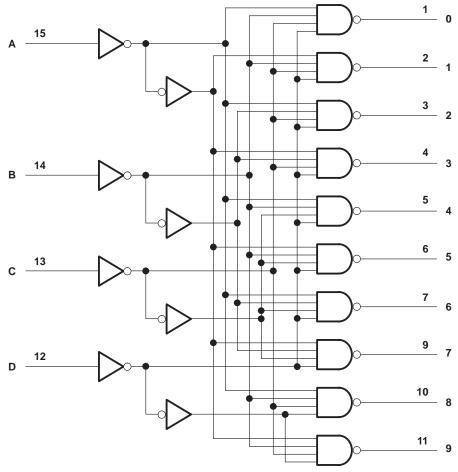
SN54HC42, SN74HC42 4-LINE TO 10-LINE DECODERS (1 of 10)

SCLS091D - DECEMBER 1982 - REVISED SEPTEMBER 2003

FUNCTION TABLE

| NO | | INP | UTS | | | | | | OUTI | PUTS | | | | |
|---------|---|-----|-----|---|---|---|---|---|------|------|---|---|---|---|
| NO. | D | С | В | Α | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | L | L | L | L | L | Н | Н | Н | Н | Н | Н | Н | Н | Н |
| 1 | L | L | L | Н | Н | L | Н | Н | Н | Н | Н | Н | Н | Н |
| 2 | L | L | Н | L | Н | Н | L | Н | Н | Н | Н | Н | Н | Н |
| 3 | L | L | Н | Н | Н | Н | Н | L | Н | Н | Н | Н | Н | Н |
| 4 | L | Н | L | L | Н | Н | Н | Н | L | Н | Н | Н | Н | Н |
| 5 | L | Н | L | Н | Н | Н | Н | Н | Н | L | Н | Н | Н | Н |
| 6 | L | Н | Н | L | Н | Н | Н | Н | Н | Н | L | Н | Н | Н |
| 7 | L | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н | L | Н | Н |
| 8 | Н | L | L | L | Н | Н | Н | Н | Н | Н | Н | Н | L | Н |
| 9 | Н | L | L | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н | L |
| | Н | L | Н | L | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н |
| | Н | L | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н |
| Invalid | Н | Н | L | L | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н |
| invalid | Н | Н | L | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н |
| | Н | Н | Н | L | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н |
| | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н | Н |

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| Supply voltage range, V _{CC} | | 0.5 V to 7 V |
|---|-------------------|----------------|
| Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC}) (see | ee Note 1) | ±20 mA |
| Output clamp current, IOK (VO < 0 or VO > VCO | C) (see Note 1) . | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | | ±25 mA |
| Continuous current through V _{CC} or GND | | ±50 mA |
| Package thermal impedance, θ _{JA} (see Note 2) | : D package | |
| • | N package | 67°C/W |
| | NS package | 64°C/W |
| Storage temperature range, T _{sta} | | –65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



recommended operating conditions (see Note 3)

| | | | S | N54HC4 | 2 | S | N74HC4 | 2 | |
|-------|---------------------------------|-------------------------|------|--------|------|------|--------|------|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | UNIT |
| Vcc | Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| | | V _{CC} = 2 V | 1.5 | | | 1.5 | | | |
| ViH | High-level input voltage | V _{CC} = 4.5 V | 3.15 | | | 3.15 | | | V |
| | | V _{CC} = 6 V | 4.2 | | | 4.2 | | | |
| | | V _{CC} = 2 V | | | 0.5 | | | 0.5 | |
| VIL | Low-level input voltage | V _{CC} = 4.5 V | | | 1.35 | | | 1.35 | V |
| | | VCC = 6 V | | | 1.8 | | | 1.8 | |
| VI | Input voltage | | 0 | | VCC | 0 | | VCC | V |
| VO | Output voltage | | 0 | | VCC | 0 | | VCC | V |
| | | V _{CC} = 2 V | | | 1000 | | | 1000 | |
| Δt/Δν | Input transition rise/fall time | V _{CC} = 4.5 V | | | 500 | | | 500 | ns |
| | | VCC = 6 V | | | 400 | | | 400 | |
| TA | Operating free-air temperature | · | -55 | | 125 | -40 | | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | 7507.00 | NIDITIONS. | ., | Т | A = 25°C | ; | SN54H | 1C42 | SN74H | IC42 | |
|-----------|----------------------------|----------------------------|------------|------|----------|------|-------|-------|-------|-------|------|
| PARAMETER | TEST CC | ONDITIONS | VCC | MIN | TYP | MAX | MIN | MAX | MIN | MAX | UNIT |
| | | | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | | |
| | | $I_{OH} = -20 \mu\text{A}$ | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| Voн | VI = VIH or VIL | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | V |
| | | $I_{OH} = -4 \text{ mA}$ | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | $I_{OH} = -5.2 \text{ mA}$ | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| | | | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | |
| | | I _{OL} = 20 μA | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| VOL | $V_I = V_{IH}$ or V_{IL} | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| | | I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | $I_{OL} = 5.2 \text{ mA}$ | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| lį | $V_I = V_{CC}$ or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| Icc | $V_I = V_{CC}$ or 0, | IO = 0 | 6 V | | | 8 | | 160 | | 80 | μΑ |
| Ci | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

| DADAMETER | FROM | то | ., | T _A = 25°C | | | SN54HC42 | | SN74H | HC42 | LINIT |
|-----------------|-------------------------------|----------|-------|-----------------------|-----|-----|----------|-----|-------|------|-------|
| PARAMETER | (INPUT) | (OUTPUT) | VCC | MIN | TYP | MAX | MIN | MAX | MIN | MAX | UNIT |
| | | | 2 V | | 65 | 150 | | 225 | | 190 | |
| t _{pd} | t _{pd} A, B, C, or D | 0–9 | 4.5 V | | 18 | 30 | | 45 | | 38 | ns |
| · | | | 6 V | | 14 | 26 | | 38 | | 32 | |
| | | | 2 V | | 28 | 75 | | 110 | | 95 | |
| tţ | | Any | 4.5 V | | 8 | 15 | | 22 | | 19 | ns |
| | | | 6 V | | 7 | 13 | | 19 | | 16 | |

operating characteristics, T_A = 25°C

| | PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----------------|-------------------------------|-----------------|-----|------|
| C _{pd} | Power dissipation capacitance | No load | 39 | pF |

PARAMETER MEASUREMENT INFORMATION

VCC From Output Test Input 50% 50% **Under Test Point** C_L = 50 pF ^tPHL tPLH -(see Note A) V_{OH} In-Phase 50% 10% -Output **LOAD CIRCUIT** VOL - tPHL VCC VOH Input 50% 90% **Out-of-Phase** 10% Output 10% 10% VOL

NOTES: A. C_L includes probe and test-fixture capacitance.

VOLTAGE WAVEFORM

INPUT RISE AND FALL TIMES

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50~\Omega$, $t_f = 6$ ns, $t_f = 6$ ns.
- C. The outputs are measured one at a time with one input transition per measurement.
- D. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

5-Sep-2011

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|------------|--------------|--------------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 5962-86821012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Call TI | |
| 5962-8682101EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Call TI | |
| SN54HC42J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN74HC42D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC42DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC42DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC42DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC42DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC42DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC42DT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC42DTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC42DTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC42N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74HC42NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74HC42NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC42NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC42NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SNJ54HC42FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54HC42J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |

⁽¹⁾ The marketing status values are defined as follows:



PACKAGE OPTION ADDENDUM

5-Sep-2011

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54HC42, SN74HC42:

Catalog: SN74HC42

www.ti.com

Military: SN54HC42

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications



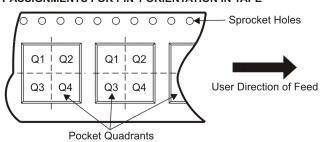
TAPE AND REEL INFORMATION





| | Dimension designed to accommodate the component width |
|----|---|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | | | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|-----------------|--------------------|----|------|--------------------------|--------------------------|---------|---------|---------|------------|-----------|------------------|
| SN74HC42DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC42NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |





*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC42DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC42NSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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