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SCAS292Q - JANUARY 1993-REVISED DECEMBER 2010

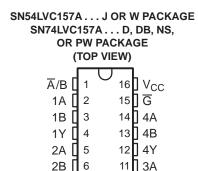
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

Check for Samples: SN54LVC157A, SN74LVC157A

FEATURES

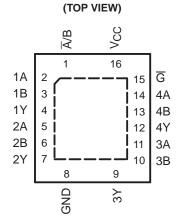
- Operate From 1.65 V to 3.6 V
- Specified From -40°C to 85°C, -40°C to 125°C, and -55°C to 125°C
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.2 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C

- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

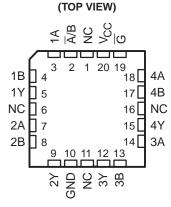


2Y 🛮 7

GND



SN74LVC157A...RGY PACKAGE



SN54LVC157A...FK PACKAGE

NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

10 3B

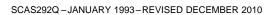
9**∏** 3Y

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 1.65-V to 3.6-V V_{CC} operation.

The 'LVC157A devices feature a common strobe (\overline{G}) input. When \overline{G} is high, all outputs are low. When \overline{G} is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide true data.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





ORDERING INFORMATION

T _A	PA	ACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC157ARGYR	LC157A
		Tube of 40	SN74LVC157AD	
–40°C to 125°C	SOIC - D	Reel of 2500	SN74LVC157ADRG3	LVC157A
		Reel of 250	SN74LVC157ADT	
	SOP - NS	Reel of 2000	SN74LVC157ANSR	LVC157A
-40°C to 125°C	SSOP - DB	Reel of 2000	SN74LVC157ADBR	LC157A
		Tube of 90	SN74LVC157APW	
	TSSOP - PW	Reel of 2000	SN74LVC157APWR	LC157A
		Reel of 250	SN74LVC157APWT	
	CDIP – J	Tube of 25	SNJ54LVC157AJ	SNJ54LVC157AJ
–55°C to 125°C	CFP – W	Tube of 150	SNJ54LVC157AW	SNJ54LVC157AW
	LCCC - FK	Tube of 55	SNJ54LVC157AFK	SNJ54LVC157AFK

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

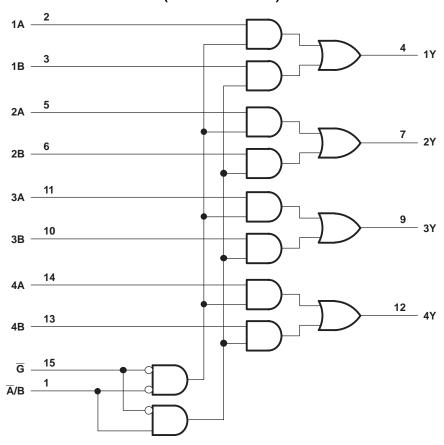
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

FUNCTION TABLE

	INP	JTS		OUTPUT
G	Ā/B	Α	В	Υ
Н	Х	X	Х	L
L	L	L	X	L
L	L	Н	X	Н
L	Н	X	L	L
L	Н	X	Н	Н



LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the D, DB, J, NS, PW, RGY, and W packages.



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V _{CC}	Supply voltage range		-0.5	6.5	V	
VI	Input voltage range ⁽²⁾		-0.5	6.5	V	
Vo	Output voltage range (2) (3)		-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-50	mA	
I _{OK}	Output clamp current	V _O < 0		-50	mA	
Io	Continuous output current			±50	mA	
	Continuous current through V _{CC} or GND			±100	mA	
		D package ⁽⁴⁾		73		
		DB package ⁽⁴⁾		82		
θ_{JA}	Package thermal impedance	NS package ⁽⁴⁾		64 108		
		PW package ⁽⁴⁾				
		RGY package ⁽⁵⁾		39		
T _{stg}	Storage temperature range		-65	150	°C	
P _{tot}	Power dissipation ^{(6) (7)}	$T_A = -40^{\circ}\text{C to } 125^{\circ}\text{C}$		500	mW	

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

Recommended Operating Conditions⁽¹⁾

			SN54LV	C157A	
			−55 TO	125°C	UNIT
			MIN	MAX	
	Complexional	Operating	2	3.6	.,
V _{CC}	Supply voltage	Data retention only	1.5		V
V_{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
VI	Input voltage	·	0	5.5	V
Vo	Output voltage		0	V _{CC}	V
	High level code of compart	V _{CC} = 2.7 V		-12	A
I _{OH}	High-level output current	V _{CC} = 3 V		-24	mA
	Law law law a subset as success	V _{CC} = 2.7 V		12	A
I _{OL}	Low-level output current	V _{CC} = 3 V		24	mA

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

The value of V_{CC} is provided in the recommended operating conditions table.

The package thermal impedance is calculated in accordance with JESD 51-7.

The package thermal impedance is calculated in accordance with JESD 51-5. For the D package, above 70°C the value of P_{tot} derates linearly with 8 mW/K. For the DB, NS, and PW packages, above 60°C the value of P_{tot} derates linearly with 5.5 mW/K.

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Recommended Operating Conditions⁽¹⁾

					SN74L	/C157A				
			T _A =	25°C	-40 To	O 85°C	-40 TC	125°C	UNIT	
			MIN	MAX	MIN	MAX	MIN	MIN MAX		
.,	Commissional	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V	
V_{CC}	Supply voltage	Data retention only	1.5		1.5		1.5		V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		0.65 × V _{CC}		0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		1.7		1.7		V	
	voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		2		2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}		0.35 × V _{CC}		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7		0.7		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		0.8		0.8		
V_{I}	Input voltage		0	5.5	0	5.5	0	5.5	V	
Vo	Output voltage		0	V _{CC}	0	V _{CC}	0	V_{CC}	V	
		V _{CC} = 1.65 V		-4		-4		-4		
	High-level output	V _{CC} = 2.3 V		-8		-8		-8	A	
I _{OH}	current	V _{CC} = 2.7 V		-12		-12		-12	mA	
		V _{CC} = 3 V		-24		-24		-24		
		V _{CC} = 1.65 V		4		4		4		
	Low-level output	V _{CC} = 2.3 V		8		8		8	A	
I _{OL}		V _{CC} = 2.7 V		12		12		12	mA	
		V _{CC} = 3 V		24		24		24		
Δt/Δν	Input transition rise	e or fall rate		10		10		10	ns/V	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

				SN54LVC1	57A				
PARAMETER	TEST CONDITIONS		V _{cc}	–55 TO 125	5°C	UNIT			
				MIN	MAX				
	$I_{OH} = -100 \mu A$		2.7 V to 3.6 V	$V_{\rm CC}-0.2$					
V _{OH}	40 4	2.7 V	2.2		.,				
	$I_{OH} = -12 \text{ mA}$	10H = -12 11IV				V			
	$I_{OH} = -24 \text{ mA}$	3 V	2.2		<u> </u>				
	I _{OL} = 100 μA	2.7 V to 3.6 V		0.2					
V_{OL}	I _{OL} = 12 mA	2.7 V		0.4	V				
	I _{OL} = 24 mA	3 V		0.55					
I _I All inputs	V _I = 5.5 V or GND		3.6 V		±5	μΑ			
I _{CC}	$V_I = V_{CC}$ or GND $I_O = 0$		3.6 V		10	μΑ			
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V		500	μΑ			



Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

							SI	N74LVC157	Ά				
PA	RAMETER	TEST COND	TIONS	V _{CC}	T _A :	$T_A = 25^{\circ}C$		-40 TO 8	35°C	-40 TO 1	25°C	UNIT	
					MIN	TYP	MAX	MIN	MAX	MIN	MAX		
		$I_{OH} = -100 \mu A$		1.65 V to 3.6 V	V _{CC} - 0.2			V _{CC} - 0.2		V _{CC} - 0.3			
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.29			1.2		1.05			
.,		$I_{OH} = -8 \text{ mA}$		2.3 V	1.9			1.7		1.55		V	
V _{OH}		10 m A		2.7 V	2.2			2.2		2.05		V	
		$I_{OH} = -12 \text{ mA}$		3 V	2.4			2.4		2.25			
$I_{OH} = -24 \text{ mA}$		$I_{OH} = -24 \text{ mA}$		3 V	2.3			2.2		2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.1		0.2		0.3		
		I _{OL} = 4 mA		1.65 V			0.24		0.45		0.6		
V_{OL}		I _{OL} = 8 mA		2.3 V			0.3		0.7		0.75	V	
		I _{OL} = 12 mA		2.7 V			0.4		0.4		0.6		
		I _{OL} = 24 mA		3 V			0.55		0.55		0.8		
II	All inputs	V _I = 5.5 V or GNI)	3.6 V			±1		±5		±20	μΑ	
I _{CC}		V _I = V _{CC} or GND	I _O = 0	3.6 V			1		10		40	μΑ	
ΔI_{CC}	One input at $V_{CC} = 0.6 \text{ V}$, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500		500		5000	μΑ		
Ci		$V_I = V_{CC}$ or GND		3.3 V		5						pF	

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN54LV	C157A	
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	–55 TO 125°C		UNIT
	(iidi O1)	(6611 61)		MIN	MAX	
	A or D		2.7 V		6.2	
	A or B		3.3 V ± 0.3 V	0.8	5.4	
	Ā/B		2.7 V		8.2	no
t _{pd}	A/D	ī	$3.3 \text{ V} \pm 0.3 \text{ V}$	0.8	7	ns
	G		2.7 V		7.8	
	9		3.3 V ± 0.3 V	0.8	6.5	



Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			3. (1			SN	N74LVC15	7A				
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	$T_A = 25^{\circ}C$			–40 TO	85°C	–40 TO	125°C	UNIT	
	,	(331131)	(0011 01)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
			1.8 V ± 0.15 V	1	5.5	13.5	1	14	1	15.5		
	A or B		2.5 V ± 0.2 V	1	3.2	7.4	1	7.9	1	10		
	AUD		2.7 V	1	3.6	5.7	1	5.9	1	7.4		
			3.3 V ± 0.3 V	1	3	5	1	5.2	1	6.4		
	Ā/B	Y	1.8 V ± 0.15 V	1	6	15.5	1	16	1	17.5	ns	
			2.5 V ± 0.2 V	1	3.7	9.6	1	10.1	1	12.2		
t _{pd}	A/D		2.7 V	1	4.1	7.9	1	8.1	1	10		
			3.3 V ± 0.3 V	1	3.4	6.6	1	6.8	1	8.4		
			1.8 V ± 0.15 V	1	5.9	13.5	1	14	1	15.5		
	G		2.5 V ± 0.2 V	1	3.5	9.3	1	9.8	1	11.9		
	G		2.7 V	1	3.9	7.6	1	7.8	1	9.3		
			3.3 V ± 0.3 V	1	3.3	6.3	1	6.5	1	7.9		
			1.8 V ± 0.15 V					2		2.5	20	
t _{sk(o)}			3.3 V ± 0.3 V					1		1.5	ns	

Operating Characteristics

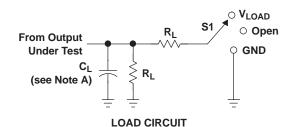
 $T_{\Lambda} = 25^{\circ}C$

1 _A – 2	PARAMETER	TEST CONDITIONS	V _{CC}	TYP	UNIT
			1.8 V	14 ⁽¹⁾	
C_{pd}	Power dissipation capacitance	f = 10 MHz	2.5 V	15 ⁽¹⁾	pF
			3.3 V	16	ı

⁽¹⁾ On products compliant to MIL-PRF-38535, this parameter does not apply.

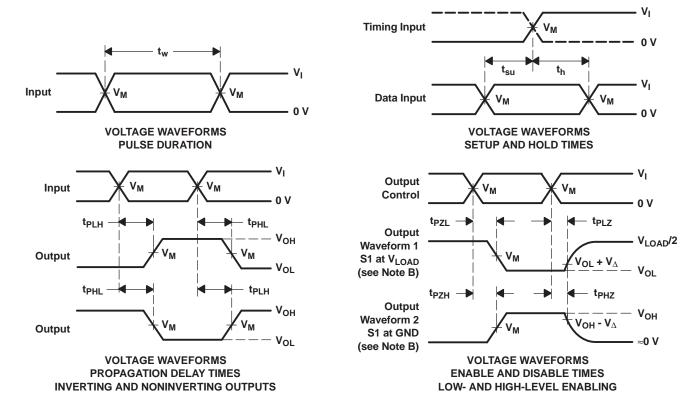


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

.,	INI	PUTS	,,	.,		_	.,
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	$oldsymbol{V}_{\Delta}$
1.8 V ± 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
33V+03V	27 V	<2.5 ns	15 V	6 V	50 nF	500 ()	03V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-0050601Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-0050601QEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
5962-0050601QFA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
SN74LVC157AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157ADBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	
SN74LVC157ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157ADBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157ADRG3	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
SN74LVC157ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157ADT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157ADTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157ADTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





5-Sep-2011

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LVC157ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157APWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	
SN74LVC157APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157APWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157ARGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN74LVC157ARGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SNJ54LVC157AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LVC157AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LVC157AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

PACKAGE OPTION ADDENDUM



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(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54LVC157A, SN74LVC157A:

Catalog: SN74LVC157A

Automotive: SN74LVC157A-Q1, SN74LVC157A-Q1

■ Enhanced Product: SN74LVC157A-EP. SN74LVC157A-EP

Military: SN54LVC157A

NOTE: Qualified Version Definitions:

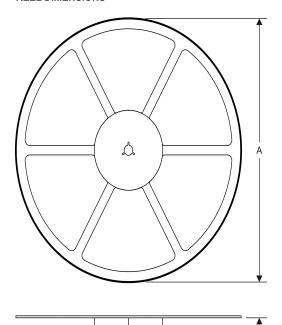
- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC157ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LVC157ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC157APWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LVC157APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC157APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC157ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC157ADBR	SSOP	DB	16	2000	346.0	346.0	33.0
SN74LVC157ANSR	SO	NS	16	2000	346.0	346.0	33.0
SN74LVC157APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LVC157APWR	TSSOP	PW	16	2000	346.0	346.0	29.0
SN74LVC157APWT	TSSOP	PW	16	250	346.0	346.0	29.0
SN74LVC157ARGYR	VQFN	RGY	16	3000	346.0	346.0	29.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



RGY (R-PVQFN-N16)

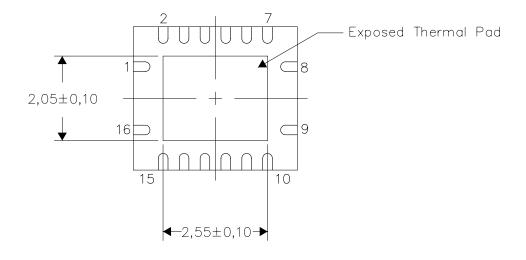
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

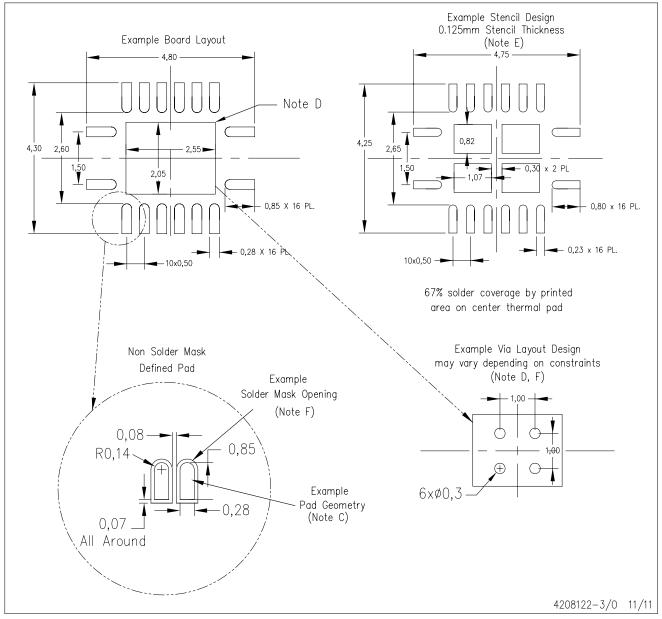
4206353-3/0 11/11

NOTE: All linear dimensions are in millimeters



RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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