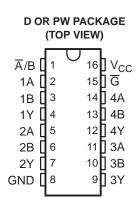
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QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

FEATURES

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Operates From 2 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.4 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C



DESCRIPTION/ORDERING INFORMATION

The SN74LVC157A quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The device features a common strobe (\overline{G}) input. When \overline{G} is high, all outputs are low. When \overline{G} is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The device provides true data.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION(1)

T _A	PACK	AGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 125°C	SOIC - D	Tape and reel	SN74LVC157AQDRQ1	L157AQ1	
-40 C to 125°C	TSSOP - PW	Tape and reel	SN74LVC157AQPWRQ1	L157AQ1	

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

FUNCTION TABLE

	OUTPUT			
G	Ā/B	Α	В	Υ
Н	Х	Х	Х	L
L	L	L	Χ	L
L	L	Н	Χ	Н
L	Н	Χ	L	L
L	Н	Χ	Н	Н

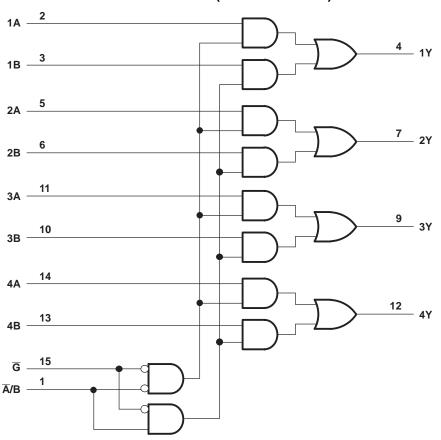


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

⁽²⁾ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V	
VI	Input voltage range (2)		-0.5	6.5	V
Vo	Output voltage range ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		– 50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
0	Package thermal impedance ⁽⁴⁾	D package		73	°C/W
θ_{JA}	rackage memai impedance 🗥	PW package		108	C/VV
T _{stg}	Storage temperature range			150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51.



Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V	Cumplicialitana	Operating	2	3.6	V
V_{CC}	Supply voltage	Data retention only	1.5		V
V_{IH}	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		٧
V_{IL}	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	٧
V_{I}	Input voltage		0	5.5	٧
Vo	Output voltage		0	V_{CC}	V
	High level output ourrent	V _{CC} = 2.7 V		-12	mΑ
I _{OH}	High-level output current	V _{CC} = 3 V		-24	ША
	Low lovel output ourrent	V _{CC} = 2.7 V		12	^ ~
I _{OL}	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	125	С

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAM	IETER	TES	V _{cc}	MIN	MAX	UNIT	
		I _{OH} = -100 μA		2.7 V to 3.6 V	V _{CC} - 0.2		
V		12 m 1		2.7 V	2.2		V
V _{OH}		$I_{OH} = -12 \text{ mA}$	3 V 2.4 3 V 2.2			V	
		I _{OH} = -24 mA					
		I _{OL} = 100 μA		2.7 V to 3.6 V		0.2	
V_{OL}		I _{OL} = 12 mA	2.7 V		0.4	V	
		I _{OL} = 24 mA	3 V		0.55		
I _I All	l inputs	V _I = 5.5 V or GND		3.6 V		±5	μΑ
I _{CC}		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V		10	μΑ
ΔI _{CC}		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μΑ

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INFOT)	(001701)	MIN MAX	MIN	MAX	
	A or B		6.2	8.0	5.4	
t _{pd}	Ā/B	Υ	8.2	0.8	7	ns
	G		7.8	0.8	6.5	

Operating Characteristics

 $T_A = 25^{\circ}C$

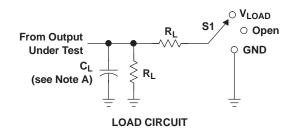
	PARAMETER	TEST CONDITIONS	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	15	16	pF

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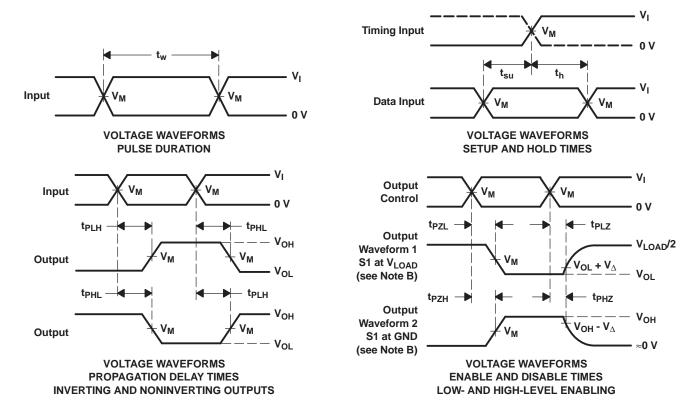


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL} t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	Open V _{LOAD} GND

.,	INPUTS		V	V		1	V
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	C _L	R_L	$oldsymbol{V}_\Delta$
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

12-Oct-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CLVC157AQPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157AQDRG4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157AQDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC157AQPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC157A-Q1:





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● Catalog: SN74LVC157A

Enhanced Product: SN74LVC157A-EP

● Military: SN54LVC157A

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

• Military - QML certified for Military and Defense Applications

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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