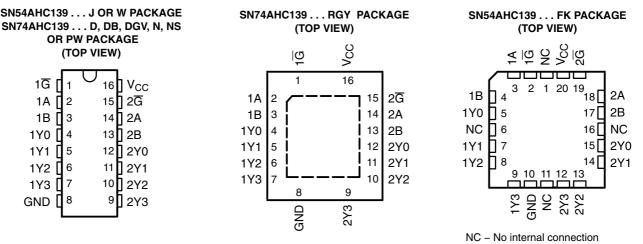
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- Operating Range 2-V to 5.5-V V<sub>CC</sub>
- Designed Specifically for High-Speed Memory Decoders and Data-Transmission Systems
- Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



#### description/ordering information

The 'AHC139 devices are dual 2-line to 4-line decoders/demultiplexers designed for 2-V to 5.5-V  $V_{CC}$  operation. These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

#### **ORDERING INFORMATION**

T <sub>A</sub>	PACKA	PACKAGE <sup>†</sup> ORDERABLE PART NUMBER		TOP-SIDE MARKING
	QFN – RGY	Tape and reel	SN74AHC139RGYR	HA139
	PDIP – N	Tube	SN74AHC139N	SN74AHC139N
	SOIC - D	Tube	SN74AHC139D	4110100
	50IC - D	Tape and reel	SN74AHC139DR	AHC139
–40°C to 85°C	SOP – NS	Tape and reel	SN74AHC139NSR	AHC139
	SSOP – DB	Tape and reel	SN74AHC139DBR	HA139
	TSSOP – PW	Tube	SN74AHC139PW	HA139
	1550P - PW	Tape and reel	SN74AHC139PWR	HA139
	TVSOP – DGV	Tape and reel	SN74AHC139DGVR	HA139
	CDIP – J	Tube	SNJ54AHC139J	SNJ54AHC139J
–55°C to 125°C	CFP – W	Tube	SNJ54AHC139W	SNJ54AHC139W
	LCCC – FK	Tube	SNJ54AHC139FK	SNJ54AHC139FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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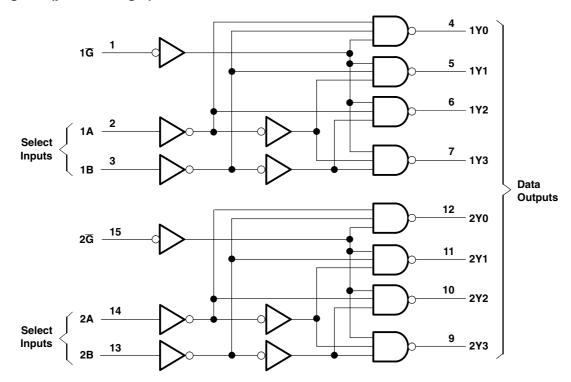
#### description/ordering information (continued)

The active-low enable ( $\overline{G}$ ) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

	(each decoder/demultiplexer)											
	INPUTS			OUTPUTS								
G	SEL	ECT		001	-015							
5	B A		Y0	Y1	Y2	Y3						
Н	х х		Н	Н	Н	Н						
L	L	L	L	Н	н	н						
L	LH		н	L	н	н						
L	H L		н	Н	L	н						
L	Н	Н	Н	Н	Н	L						

#### FUNCTION TABLE (each decoder/demultiplex

#### logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.



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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. The package thermal impedance is calculated in accordance with JESD 51-7.
- 3. The package thermal impedance is calculated in accordance with JESD 51-5.

#### recommended operating conditions (see Note 4)

			SN54AH	IC139	SN74A	HC139	
			MIN	MAX	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5.5	2	5.5	V
		$V_{CC} = 2 V$	1.5		1.5		
VIH	High-level input voltage	$V_{CC} = 3 V$	2.1		2.1		V
		V <sub>CC</sub> = 5.5 V	3.85		3.85		
		$V_{CC} = 2 V$		0.5		0.5	
VIL	Low-level input voltage	$V_{CC} = 3 V$		0.9		0.9	V
		V <sub>CC</sub> = 5.5 V		1.65		1.65	
VI	Input voltage	·	0	5.5	0	5.5	V
Vo	Output voltage		0	V <sub>CC</sub>	0	$V_{CC}$	V
		$V_{CC} = 2 V$	200	-50		-50	μA
l <sub>OH</sub>	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	R	-4		-4	
		$V_{CC}$ = 5 V ± 0.5 V	~	-8		-8	mA
		V <sub>CC</sub> = 2 V		50		50	μA
l <sub>OL</sub>	Low-level output current	$V_{CC}=3.3~V\pm0.3~V$		4		4	
		$V_{CC}$ = 5 V ± 0.5 V		8		8	mA
		$V_{CC}=3.3~V\pm0.3~V$		100		100	
$\Delta t / \Delta v$	Input transition rise or fall rate	$V_{CC}$ = 5 V ± 0.5 V		20		20	ns/V
T <sub>A</sub>	Operating free-air temperature	•	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			Т	ק = 25°C		SN54AH	IC139	SN74A	HC139	
PARAMETER	TEST CONDITIONS	v <sub>cc</sub>	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		2 V	1.9	2		1.9		1.9		
	l <sub>OH</sub> = -50 μA	3 V	2.9	3		2.9		2.9		
V <sub>OH</sub>		4.5 V	4.4	4.5		4.4		4.4		v
0.1	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48	5W	2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8	EU	3.8		
		2 V			0.1	0	0.1		0.1	
	l <sub>OL</sub> = 50 μA	3 V			0.1	د <i>ک</i>	0.1		0.1	
V <sub>OL</sub>		4.5 V			0.1	$\gamma_{Q_{i}}$	0.1		0.1	v
	I <sub>OL</sub> = 4 mA	3 V			0.36	PAC	0.5		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.5		0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	μA
I <sub>CC</sub>	$V_{I} = V_{CC} \text{ or GND}, \qquad I_{O} = 0$	5.5 V			4		40		40	μA
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10				10	pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at  $V_{CC}$  = 0 V.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

	FROM	то	LOAD	Т	<sub>A</sub> = 25°C	;	SN54A	HC139	SN74A	HC139	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t <sub>PLH</sub>	A an D	Y	0 15 55		7.2**	11**	1**	13**	1	13	
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 15 pF		7.2**	11**	1**	13**	1	13	ns
t <sub>PLH</sub>	G	Y	0 45 - 5		6.4**	9.2**	1**	11**	1	11	
t <sub>PHL</sub>	5	Ŷ	C <sub>L</sub> = 15 pF		6.4**	9.2**	1**	11**	1	11	ns
t <sub>PLH</sub>	A	V.	0 50		9.7	14.5	16	16.5	1	16.5	
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 50 pF		9.7	14.5	70	16.5	1	16.5	ns
t <sub>PLH</sub>	G	Y	C = 50 pF		8.9	12.7	4	14.5	1	14.5	
t <sub>PHL</sub>	G	T	C <sub>L</sub> = 50 pF		8.9	12.7	1	14.5	1	14.5	ns

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

	FROM	то	LOAD	T,	₄ = 25°C	;	SN54A	HC139	SN74A	HC139	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t <sub>PLH</sub>	A or D	Y	0 15 55		5**	7.2**	1**	8.5**	1	8.5	
t <sub>PHL</sub>	A or B	Ŷ	C <sub>L</sub> = 15 pF		5**	7.2**	1**	8.5**	1	8.5	ns
t <sub>PLH</sub>	×	V.	0 15 5		4.4**	6.3**	1**	7.5**	1	7.5	
t <sub>PHL</sub>	G	Y	C <sub>L</sub> = 15 pF		4.4**	6.3**	1**	7.5**	1	7.5	ns
t <sub>PLH</sub>	A or D	Y	0 50 55		6.5	9.2	10	10.5	1	10.5	
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 50 pF		6.5	9.2	50	10.5	1	10.5	ns
t <sub>PLH</sub>	G	Y	C <sub>1</sub> = 50 pF		5.9	8.3	4 4	9.5	1	9.5	20
t <sub>PHL</sub>	5	ŕ	$C_L = 50 \text{ pr}$		5.9	8.3	1	9.5	1	9.5	ns

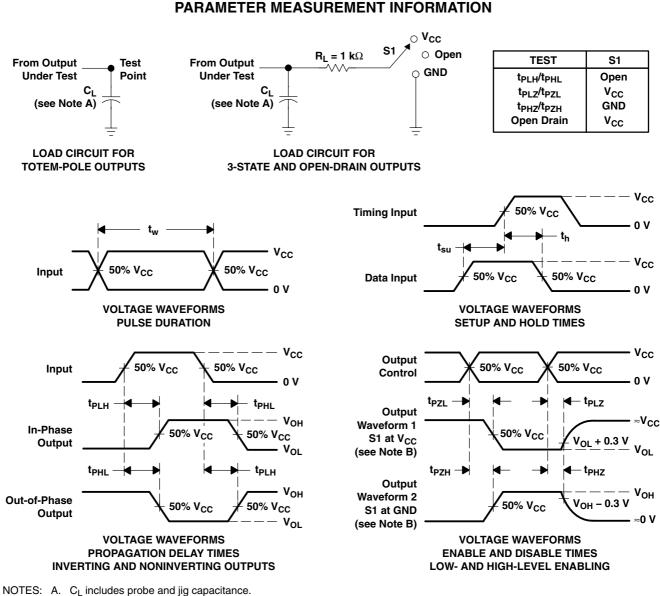
\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

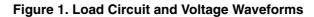


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#### operating characteristics, $V_{CC} = 5 V$ , $T_A = 25^{\circ}C$ PARAMETER **TEST CONDITIONS** TYP UNIT Cpd Power dissipation capacitance No load. f = 1 MHz13 pF



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>Q</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  3 ns, t<sub>f</sub>  $\leq$  3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.





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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AHC139D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI
SN74AHC139DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHC139NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHC139NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139PWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI
SN74AHC139PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS &	CU NIPDAU	Level-2-260C-1 YEAR



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Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing		kage Ity	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
						no Sb/Br)		
SN74AHC139RGYRG4	ACTIVE	VQFN	RGY	16 30	000 (	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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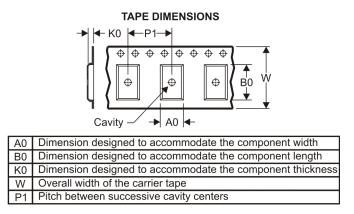
## PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC139DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHC139DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC139DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC139NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC139PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC139RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

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## PACKAGE MATERIALS INFORMATION

30-Jul-2010



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC139DBR	SSOP	DB	16	2000	346.0	346.0	33.0
SN74AHC139DGVR	TVSOP	DGV	16	2000	346.0	346.0	29.0
SN74AHC139DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74AHC139NSR	SO	NS	16	2000	346.0	346.0	33.0
SN74AHC139PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
SN74AHC139RGYR	VQFN	RGY	16	3000	346.0	346.0	29.0

## N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



PLASTIC SMALL-OUTLINE

MPDS006C - FEBRUARY 1996 - REVISED AUGUST 2000

#### DGV (R-PDSO-G\*\*)

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153

14/16/20/56 Pins – MO-194



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  $\beta$ . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



## LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- Ε. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Æ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
- The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



## RGY (R-PVQFN-N16)

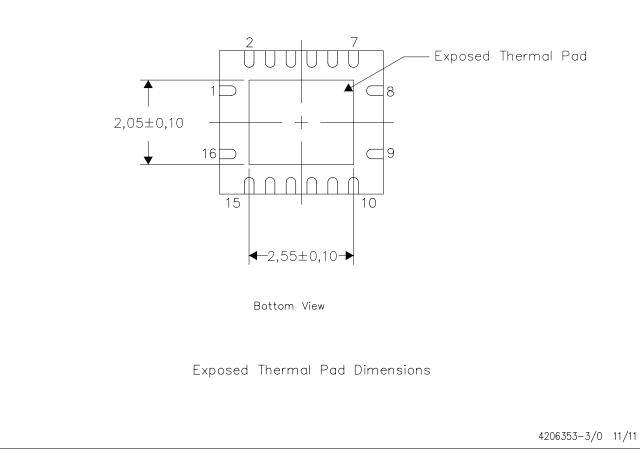
## PLASTIC QUAD FLATPACK NO-LEAD

#### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

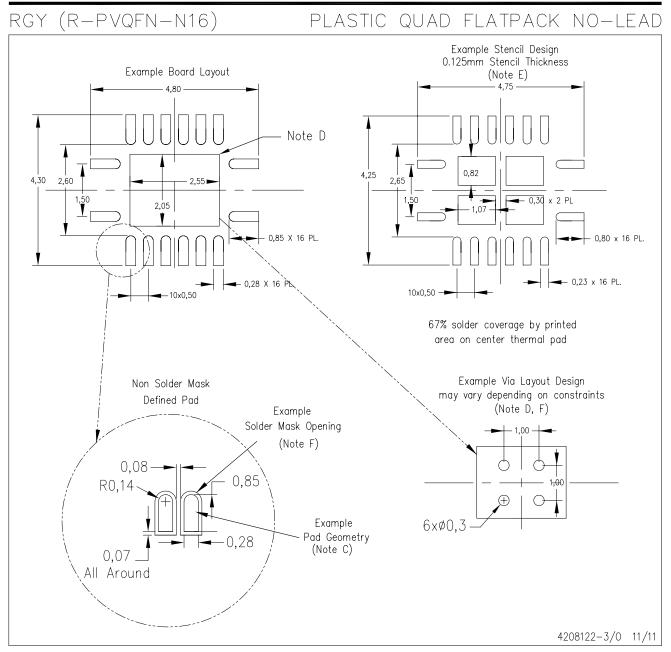
For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



#### NOTE: All linear dimensions are in millimeters





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="http://www.ti.com">http://www.ti.com</a>.

- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



#### PLASTIC SMALL-OUTLINE PACKAGE

#### 0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 $\bigcirc$ Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS \*\* 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G\*\*)

**14-PINS SHOWN** 

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

### DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



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