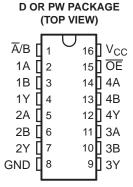
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FEATURES

- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Operates From 2 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.6 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C



DESCRIPTION/ORDERING INFORMATION

The SN74LVC257A-EP quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The device is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable (\overline{OE}) input is at a high logic level.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T _A	PACKA	GE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC - D	Reel of 2500	SN74LVC257AQDREP	C257AEP
	TSSOP – PW	Reel of 2000	SN74LVC257AQPWREP	C257AEP
5500 to 40500	SOIC - D	Reel of 2500	SN74LVC257AMDREP ⁽²⁾	C257AME
–55°C to 125°C	TSSOP – PW	Reel of 2000	SN74LVC257AMPWREP	C257AME

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) Product Preview



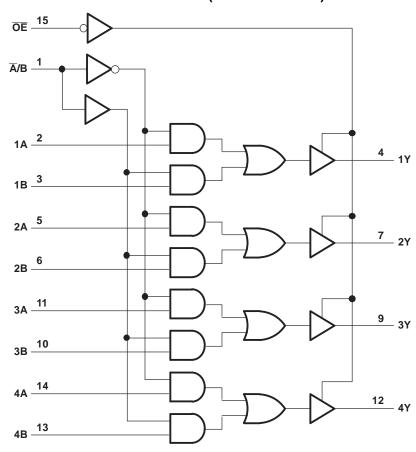
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



FUNCTION TABLE

	INPU	JTS		ОИТРИТ
ŌĒ	Ā/B	Α	В	Y
Н	Х	Х	Х	Z
L	L	L	X	L
L	L	Н	X	Н
L	Н	X	L	L
L	Н	X	Н	Н

LOGIC DIAGRAM (POSITIVE LOGIC)





SN74LVC257A-EP QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS736B-NOVEMBER 2005-REVISED JANUARY 2007

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range ⁽²⁾		-0.5	6.5	V
Vo	Output voltage range (2)(3)		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		mA	
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GN	D		±100	mA
Δ	Package thermal impedance ⁽⁴⁾	D package		73	°C/W
θ_{JA}	rackage mermai impedance (**)	PW package		108	C/VV
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
\/	Cupply valtage	Operating	2	3.6	V
V_{CC}	Supply voltage	Data retention only	1.5		V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	V
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V _{CC}	V
	High lovel output ourrent	V _{CC} = 2.7 V		-12	A
I _{OH}	High-level output current	V _{CC} = 3 V	-24		mA
	Low lovel output ourront	V _{CC} = 2.7 V		12	mA
I _{OL}	Low-level output current	V _{CC} = 3 V		24	ША
Δt/Δν	Input transition rise or fall rate			10	ns/V
_	Operating free air temperature	Q-temp	-40	125	°C
T_A	Operating free-air temperature	M-temp	-55	125	٠.

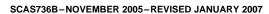
⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

⁽²⁾ he input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC257A-EP QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS





Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP(1)	MAX	UNIT
	$I_{OH} = -100 \mu\text{A}$	2.7 V to 3.6 V	V _{CC} – 0.2		
V	l - 12 mΔ	2.7 V	2.2		V
V_{OH}	$I_{OH} = -12 \text{ mA}$	3 V	2.4		V
	$I_{OH} = -24 \text{ mA}$	3 V	2.2		
	I _{OL} = 100 μA	2.7 V to 3.6 V		0.2	
V _{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
I _I	V _I = 5.5 V or GND	3.6 V		±5	μΑ
I _{OZ}	$V_O = V_{CC}$ or GND	3.6 V		±15	μΑ
I _{cc}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μΑ
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V		500	μΑ
C _I	$V_I = V_{CC}$ or GND	3.3 V	5		pF
C _o	$V_O = V_{CC}$ or GND	3.3 V	5		pF

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} =	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	
	A or B	V		5.4	1	4.6	
^L pd	Ā/B	Y		7.5	1	6.4	ns
t _{en}	ŌĒ	Y		6.7	1	5.6	ns
t _{dis}	ŌĒ	Y		4.7	0.5	4.3	ns
t _{sk(o)}						1	ns

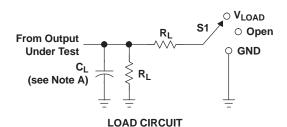
Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
	FARAMETER	TEST CONDITIONS	TYP	TYP	ONII
C _{pd}	Power dissipation capacitance	f = 10 MHz	14.5	15.5	pF

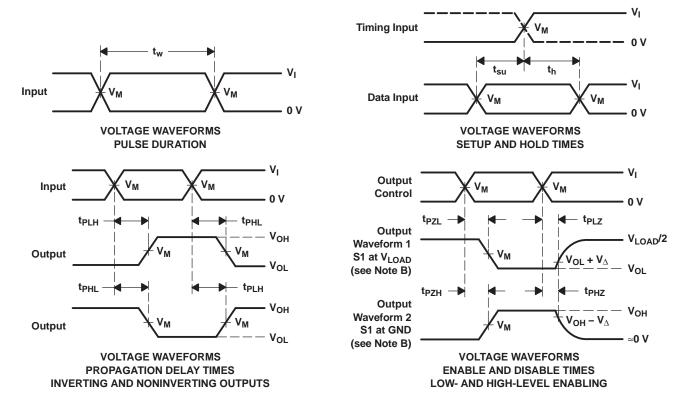
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

		PUTS	.,	V	•	1	.,
V _{CC}	VI	t _r /t _f	V _M V _{LOAD}		CL	R_L	$V_{\!\scriptscriptstyle \Delta}$
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM



.com 18-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC257AMPWREP	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC257AQDREP	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC257AQPWREP	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04660-01XE	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04660-01YE	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04660-02YE	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC257A-EP:

Catalog: SN74LVC257A

Automotive: SN74LVC257A-Q1

Military: SN54LVC257A

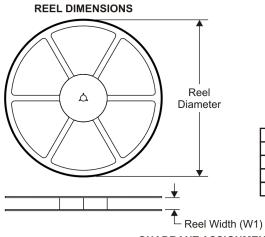
NOTE: Qualified Version Definitions:

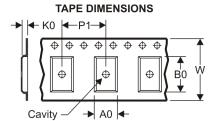
- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC257AMPWREP	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257AQDREP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC257AQPWREP	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

www.ti.com 30-Jul-2010



*All dimensions are nominal

7 il dimensione de nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC257AMPWREP	TSSOP	PW	16	2000	346.0	346.0	29.0
SN74LVC257AQDREP	SOIC	D	16	2500	333.2	345.9	28.6
SN74LVC257AQPWREP	TSSOP	PW	16	2000	346.0	346.0	29.0

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



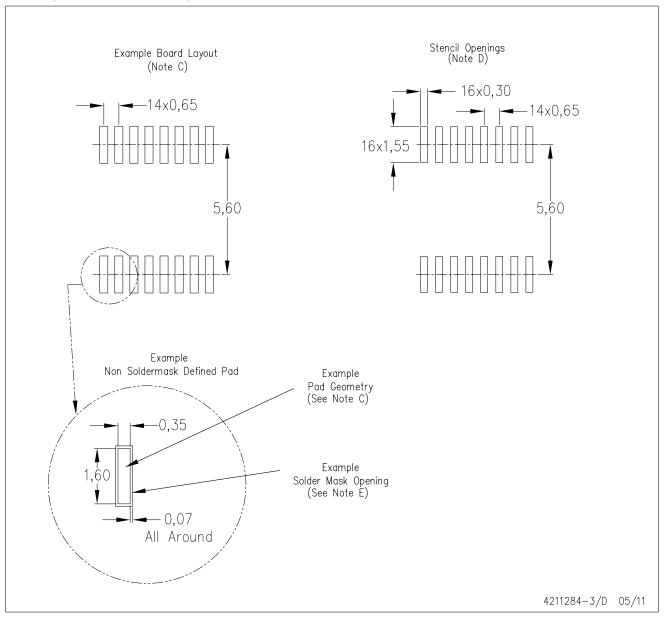
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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