

STPIC6A259

POWER LOGIC 8-BIT ADDRESSABLE LATCH

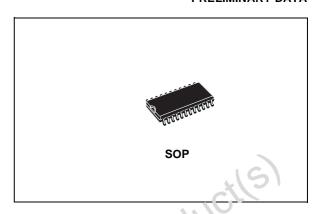
PRELIMINARY DATA

- LOW R_{DS(on)}: 1Ω TYP
- OUTPUT SHORT-CIRCUIT PROTECTION
- 75mJ AVAILANCHE ENERGY
- EIGHT 350mA DMOS OUTPUTS
- 50V SWITCHING CAPABILITY
- FOUR DISTINCT FUNCTION MODES
- LOW POWER CONSUMPTION



This power logic 8-bit addressable latch controls open-drain DMOS transistor outputs and is general-purpose designed for applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multifunctional device capable of operating as an 8-line addressable latches or eight demultiplexer with active-low DMOS outputs. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

Four distinct modes of operation are selectable by controlling the clear (CLR) and enable (G) inputs and enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressable latch. The addressed DMOS-transistor output inverts the data input with all unadressable latch. The data input with all unadressable latch. In the MOS-transistor output remaining in their previous state. In the MOS-transistor outputs, remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneus data in the latch, enable G should be



held high (inactive) while the address lines are changing. In the 8-line demoultiplexing mode, the addressed output is inverted with respect to the D input and all other output are high. In the clear mode, all outputs are high and unaffected by the address and data inputs.

Sepa at power ground (PGND) and logic ground (LCND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are interally connected, and each pGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logi and load circuits.

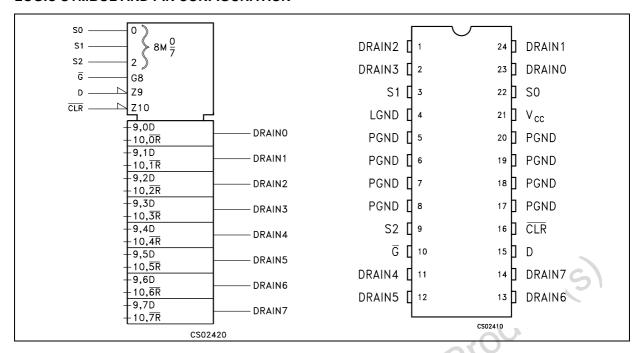
The STPIC6A259 is offered in a termally enhanced SO-24 package. The STPIC6A259 is characterized for operation over the operating case temperature range -40°C to 125°C.

ORDIERING CODES

Туре	Package	Comments	
STPIC6A259M	SO-24 Batwing (Tube)	50parts per tube / 20tube per box	
STPIC6A259MTR	SO-24 Batwing (Tape & Reel)	2500 parts per reel	

March 2001 1/13

LOGIC SYMBOL AND PIN CONFIGURATION



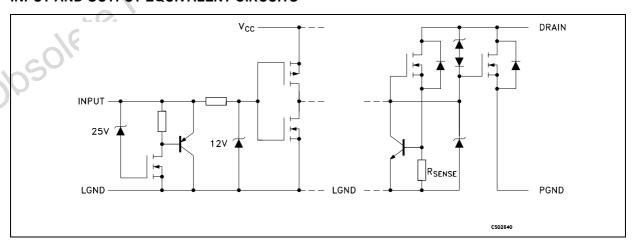
FUNCTIONAL TABLE

INI	INPUTS		OUTPUT OF	EACH	FUNCTION	
CLR	G	D	ADDRESSED DRAIN	OTHER DRAIN	FUNCTION	
Н	L	Н	L	Q _{io}	Addressable	
Н	L	L	Н	Q_{io}	Latch	
Н	Н	Χ	Q _{io}	Q_{io}	Memory	
L	L	Τ	L	Н	8-Line	
L	L	L	Н	Н	Demultiplexer	
L	Η	Χ	Н	Н	Clear	

FUNCTIONAL TABLE

SELECT INPUTS			DRAIN ADDRESSED		
S2	S1	S0	DRAIN ADDRESSED		
Ð	L	L	0		
Q _L	L	Н	1		
L	Н	L	2		
L	Н	Н	3		
Н	L	L	4		
Н	L	Н	5		
Н	Н	L	6		
Н	Н	Н	7		

INPUT AND OUTPUT EQUIVALENT CIRCUITS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Logic Supply Voltage (See Note 2)	7	V
V _I	Logic Input Voltage Range	-0.3 to 7	V
V _{DS}	Power DMOS Drain to Source Voltage (See Note 2)	50	V
I _{DS}	Continuous Source to Drain Diode Anode Current	1	Α
I _{DS}	Pulsed Source to Drain Diode Anode Current (See Note 3)	2	Α
I _D	Pulsed Drain Current, Each Output, All Output ON (T _C =25°C)	1.1	Α
I _D	Continuous Current, Each Output, All Output ON (T _C =25°C)	350	mA
I _D	Peak Drain Current Single Output (T _C =25°C) (See Note 3)	1.1	Α
E _{AS}	Single Pulse Avalanche Energy (See Note 6)	75	mJ
I _{AS}	Avalanche Current (See Note 4)	600	mA
P_d	Continuous total dissipation (T _C ≤ 25°C)	1750	mW
P _d	Continuous total dissipation (T _C = 125°C)	350	mW
T _J	Operating Virtual Junction Temperature Range	-40 to +150	°C
T _C	Operating Case Temperature Range	-40 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature 1.6mm (1/16inch) from case for 10 seconds	260	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

THERMAL DATA

Symbol	Parameter		Unit
R _{thj-case}	Thermal Resistance Junction-case	10	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	50	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Logic Supply Voltage	4.5	5.5	V
V _{IH}	High Level Input Voltage	0.85V _{CC}	V _{CC}	V
V_{IL}	Low Level Input Voltage	0	0.15V _{CC}	V
I _{DP}	Pulse Drain Output Current (T _C =25°C, V _{CC} =5V) (see note 3, 5)	-1.8	0.6	Α
t _{su}	Set-up Time, D High Before G ↑ (see Figure 2)	10		ns
t _h	Hold Time, D High Before G ↑ (see Figure 2)	5		ns
t _W	Pulse Duration (see Figure 2)	15		ns
T _C	Operating Case Temperature	-40	125	°C

577

DC CHARACTERISTICS (V_{CC} =5V, T_{C} = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSX}	Drain-to-Source breakdown Voltage	I _D = 1mA	50			V
V _{SD}	Source-to-Drain Diode Forward Voltage	I _F = 350 mA (See Note 3)		0.8	1.1	V
I _{IH}	High Level Input Current	$V_I = V_{CC}$			1	μΑ
I _{IL}	Low Level Input Current	V _I = 0			-1	μΑ
I _{CC}	Logic Supply Current	I _O = 0		0.5	5	mA
I _{OK}	Output Current at Which Chopping Starts	$T_C = 25^{\circ}C$ (See Note 3 and Figg. 3, 4)	0.6	0.8	1.1	Α
I _(nom)	Nominal Current	$V_{DS(on)} = 0.5V$ $I_{(nom)} = I_D$ $V_{CC} = 5V$ $T_C = 85^{\circ}C$ (See Note 5, 6, 7)		350		mA
I _D	Off-State Drain Current	$V_{DS} = 40V$ $T_{C}=25$ °C		0.1	1	μΑ
		$V_{DS} = 40V$ $T_{C}=125^{\circ}C$		0.2	5 -	μΑ
R _{DS(on)}	Termination Resistance	$I_D = 350 \text{mA}$ $T_C = 25^{\circ}\text{C}$		1	1.5	Ω
	(See Note 5, 6 and figg. 9, 10)	$I_D = 350 \text{mA}$ $T_C = 125 ^{\circ}\text{C}$		1.7	2.5	Ω

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_C= 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{PHL}	Propagation Dealy Time, High to Low Level Output from D	C _L = 30pF I _D = 350mA (See Figg. 1, 2, 11)	3,	30		ns
t _{PLH}	Propagation Dealy Time, Low to High Level Output from D	00501		125		ns
t _r	Rise Time, Drain Output			60		ns
t _f	Fall Time, Drain Output			30		ns
t _a	Reverse Recovery Current Rise Time	I _F = 350mA di/dt = 20A/μs (See Note 5, 6 and Fig. 5)		100		ns
t _{rr}	Reverse Recovery Time			300		ns

Note 1: All Voltage valuea are with respect to LGND and PGND Note 2: Each power DMOS source is internally connected to GND

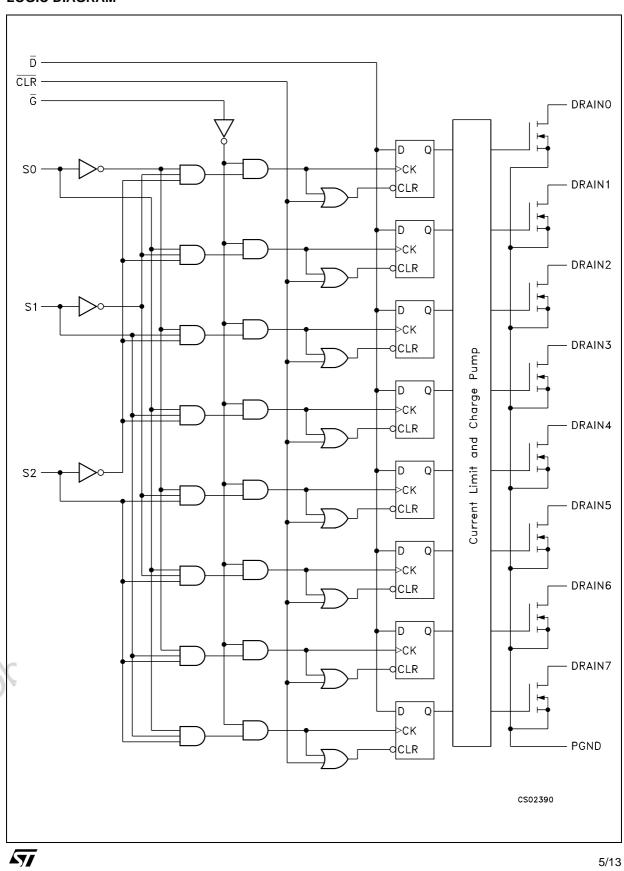
Note 3: Pulse duration \leq 100ms and duty cycle \leq 2%

Note 4: Drain Supply Voltage = 15V, starting junction temperature (T_{JS}) = 25°C. L = 210 μ H and I_{AS} = 600mA (See Fig. 6) Note 5: Technique should limit T_J - T_C to 10°C maximum

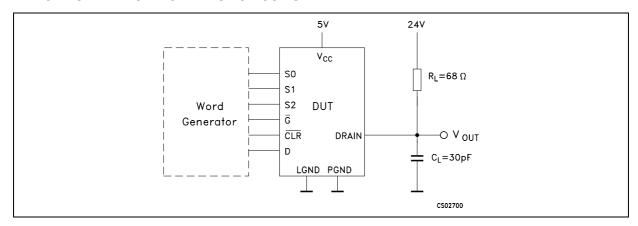
Note 6: These parameters are measured with voltage sensing contacts separate from the current-carrying contacts.

Note 7: Nominal Current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5V at $T_C = 85^{\circ}C$.

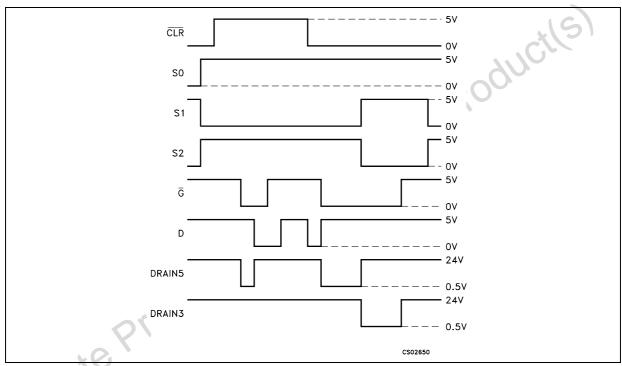
LOGIC DIAGRAM



TYPICAL OPERATION MODE TEST CIRCUITS

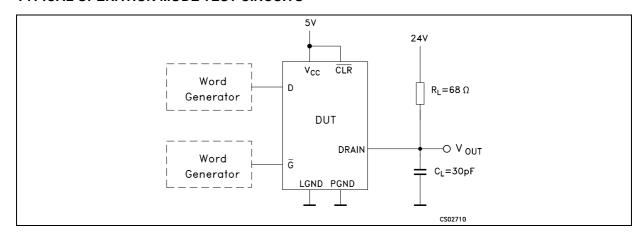


TYPICAL OPERATION MODE WAVEFORMS

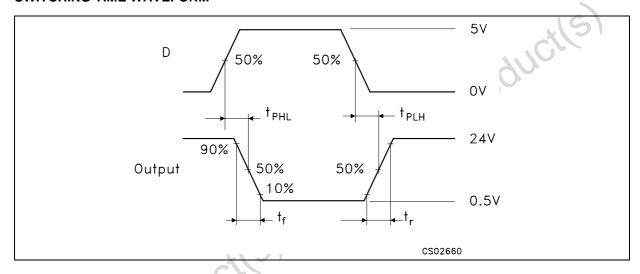


NOTE: A) The word generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulse repetition rate (PRR) = 5KHz, $Z_O = 50\Omega$ B) C_L includes probe and jig capacitance.

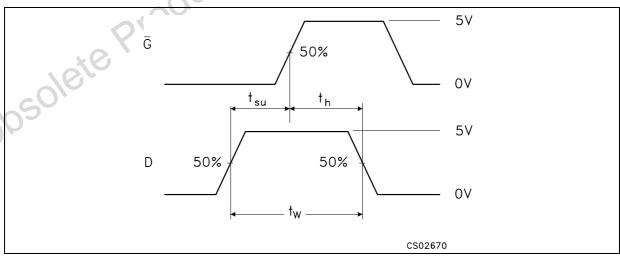
TYPICAL OPERATION MODE TEST CIRCUITS



SWITCHING TIME WAVEFORM



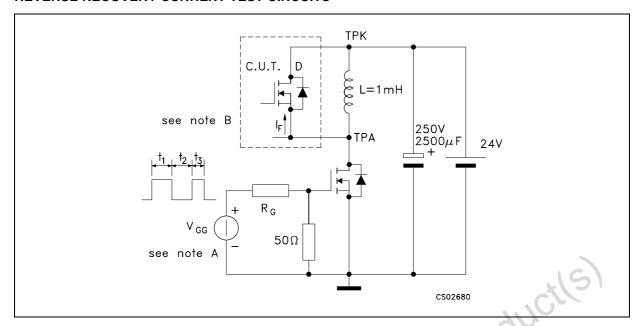
INPUT SETUP AND HOLD WAVEFORM



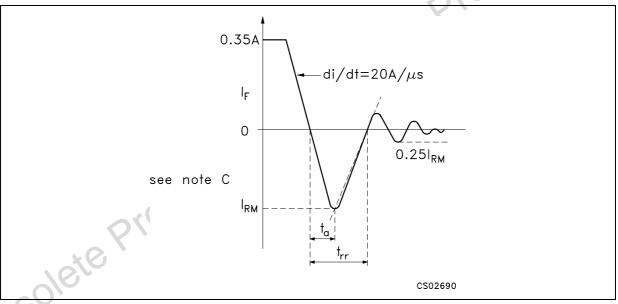
NOTE: A) The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulse repetition rate (PRR) = 5KHz, $Z_O = 50\Omega$ B) C_L includes probe and jig capacitance.

4

REVERSE RECOVERY CURRENT TEST CIRCUITS



SOURCE DRAIN DIODE WAVEFORM

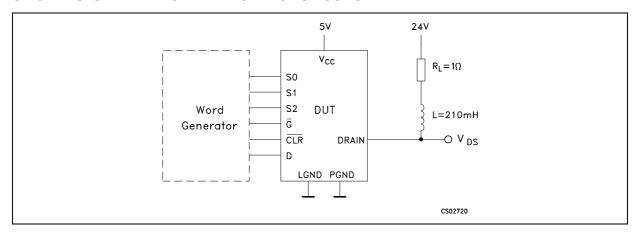


NOTE: A) The V_{GG} amplitude and R_{G} are adjusted for di/dt = 20A/ μ s. A V_{GG} double-pulse trainn is used to set I_{F} = 0.35A. where t_{1} = 10 μ s, t_{2} = 7 μ s and t_{3} = 3 μ s

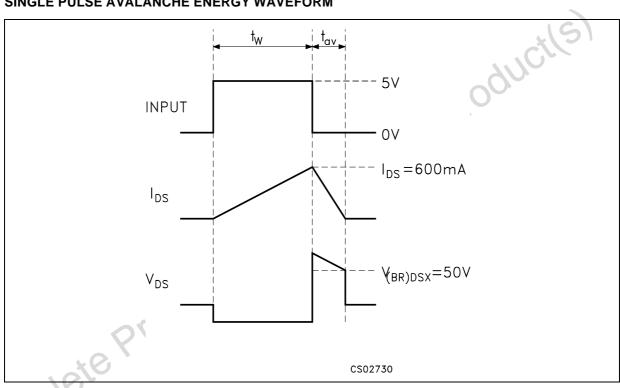
B) The Drain terminal under test is connected to the TPK test point. All other terminals are connected together and connected to the TPA test point.

C) I_{RM} = maximum recovery current.

SINGLE PULSE AVALANCHE ENERGY TEST CIRCUITS



SINGLE PULSE AVALANCHE ENERGY WAVEFORM



NOTE: A) The word generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 1$

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified T_i = 25°C)

Figure 1 : Maximum Continuous Drain Current vs Number of Outputs Conducting Simultaneously

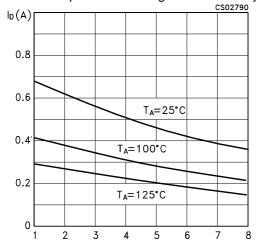


Figure 2 : Static Drain-Source ON-State Resistance vs Drain Current

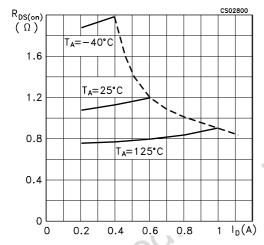


Figure 3: MaximumPeak Drain Current vs Number of Outputs Conducting Simultaneously

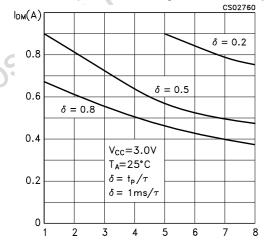


Figure 4 : Static Drain-Source ON-State Resistance vs Logic Supply Voltage

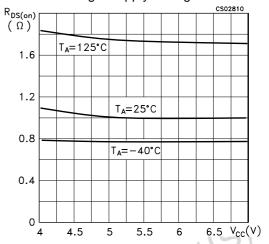


Figure 5 : Chopping Mode Characteristics

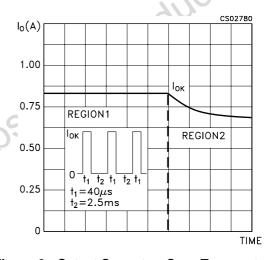


Figure 6 : Output Current vs Case Temperature

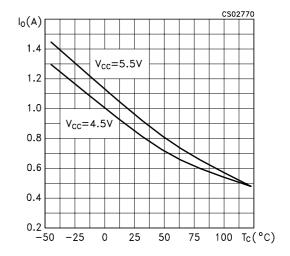


Figure 7: Switching Time vs Case Temperature

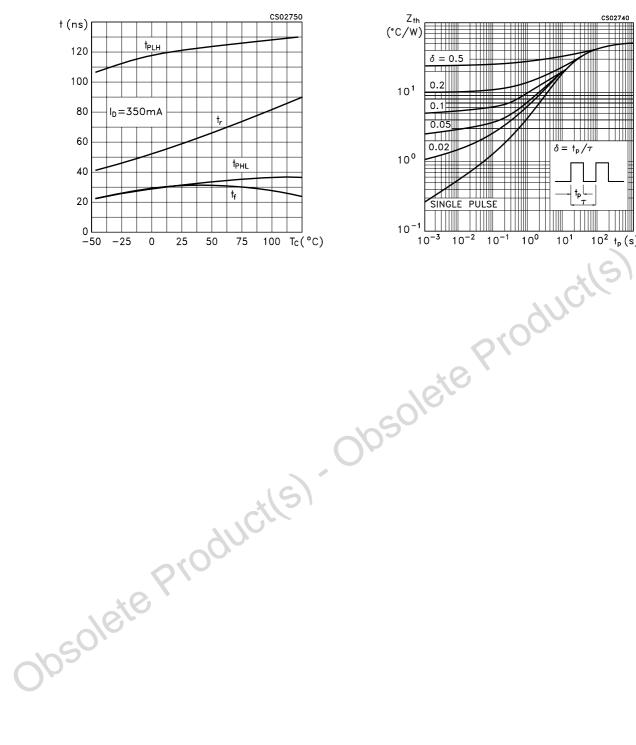
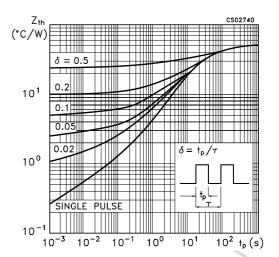
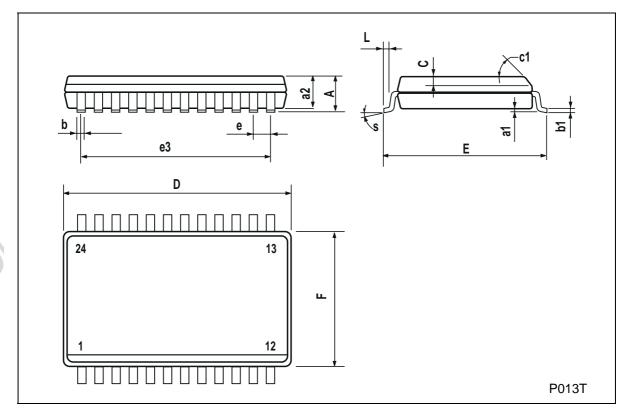


Figure 8: Switching Time vs Case Temperature



SO-24 MECHANICAL DATA

DIM.		mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
А			2.65			0.104	
a1	0.10		0.20	0.004		0.007	
a2			2.45			0.096	
b	0.35		0.49	0.013		0.019	
b1	0.23		0.32	0.009		0.012	
С		0.50			0.020		
c1			45 ((typ.)			
D	15.20		15.60	0.598		0.614	
Е	10.00		10.65	0.393		0.420	
е		1.27			0.05		
e3		13.97			0.55		
F	7.40		7.60	0.291		0.299	
L	0.50		1.27	0.19		0.050	
S	8 (max.)						



Informations on the production of the production Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics. © The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco Singapore - Spain - Sweden - Switzerland - United Kingdom © http://www.st.com

