# TEXAS INSTRUMENTS

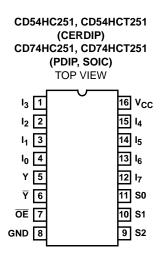
Data sheet acquired from Harris Semiconductor SCHS169C

November 1997 - Revised October 2003

### Features

- Selects One of Eight Binary Data Inputs
- Three-State Output Capability
- True and Complement Outputs
- Typical (Data to Output) Propagation Delay of 14ns at  $V_{CC}$  = 5V,  $C_L$  = 15pF,  $T_A$  = 25 $^{o}C$
- Fanout (Over Temperature Range)
  - Standard Outputs ..... 10 LSTTL Loads
  - Bus Driver Outputs ..... 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: NIL = 30%, NIH = 30% of V<sub>CC</sub> at V<sub>CC</sub> = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,
    V<sub>IL</sub>= 0.8V (Max), V<sub>IH</sub> = 2V (Min)
  - CMOS Input Compatibility, II  $\leq$  1 $\mu\text{A}$  at V\_OL, V\_OH

#### Pinout



# CD54HC251, CD74HC251, CD54HCT251, CD74HCT251

## High-Speed CMOS Logic 8-Input Multiplexer, Three-State

### Description

The 'HC251 and 'HCT251 are 8-channel digital multiplexers with three-state outputs, fabricated with high-speed silicongate CMOS technology. Together with the low power consumption of standard CMOS integrated circuits, they possess the ability to drive 10 LSTTL loads. The three-state feature makes them ideally suited for interfacing with bus lines in a bus-oriented system.

This multiplexer features both true (Y) and complement  $(\overline{Y})$  outputs as well as an output enable  $(\overline{OE})$  input. The  $\overline{OE}$  must be at a low logic level to enable this device. When the  $\overline{OE}$  input is high, both outputs are in the high-impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and  $\overline{Y}$  outputs. The 'HCT251 logic family is speed, function, and pin-compatible with the standard 'LS251.

### **Ordering Information**

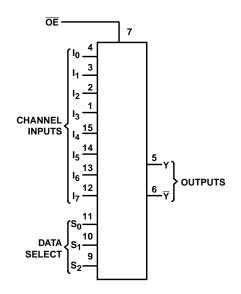
PART NUMBER	TEMP. RANGE ( <sup>o</sup> C)	PACKAGE
CD54HC251F3A	-55 to 125	16 Ld CERDIP
CD54HCT251F3A	-55 to 125	16 Ld CERDIP
CD74HC251E	-55 to 125	16 Ld PDIP
CD74HC251M	-55 to 125	16 Ld SOIC
CD74HC251MT	-55 to 125	16 Ld SOIC
CD74HC251M96	-55 to 125	16 Ld SOIC
CD74HCT251E	-55 to 125	16 Ld PDIP
CD74HCT251M	-55 to 125	16 Ld SOIC
CD74HCT251MT	-55 to 125	16 Ld SOIC
CD74HCT251M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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## Functional Diagram



#### TRUTH TABLE

		NPUTS		OUTPUT			
	SELECT		OUTPUT				
\$2	S1	<b>S</b> 0	CONTROL OE	Y	Ŧ		
X	Х	Х	Н	Z	Z		
L	L	L	L	Ι <sub>Ο</sub>	Ī <sub>0</sub>		
L	L	Н	L	I <sub>1</sub>	Ī <sub>1</sub>		
L	Н	L	L	l <sub>2</sub>	Ī2		
L	Н	Н	L	I <sub>3</sub>	Ī3		
н	L	L	L	I <sub>4</sub>	Ī4		
н	L	Н	L	I <sub>5</sub>	Ī5		
н	Н	L	L	I <sub>6</sub>	Ī <sub>6</sub>		
н	Н	Н	L	I <sub>7</sub>	Ī7		

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, Z = High Impedance (Off),  $I_0$ ,  $I_1...I_7$  = the level of the respective input.

#### **Absolute Maximum Ratings**

DC Supply Voltage, V <sub>CC</sub>
For $V_1 < -0.5V$ or $V_1 > V_{CC} + 0.5V$
DC Output Diode Current, I <sub>OK</sub>
For $V_0 < -0.5V$ or $V_0 > V_{CC} + 0.5V$
DC Drain Current, per Output, I <sub>O</sub>
For -0.5V < V <sub>O</sub> < V <sub>CC</sub> +0.5V
DC Output Source or Sink Current per Output Pin, IO
For $V_0 > -0.5V$ or $V_0 < V_{CC} + 0.5V$
DC V <sub>CC</sub> or Ground Current, I <sub>CC</sub> ±50mA

#### **Operating Conditions**

Temperature Range (T <sub>A</sub> )55°C to 125°C
Supply Voltage Range, V <sub>CC</sub>
HC Types
HCT Types4.5V to 5.5V
DC Input or Output Voltage, VI, VO 0V to VCC
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

### **Thermal Information**

Thermal Resistance (Typical, Note 1)	θ <sub>JA</sub> ( <sup>o</sup> C/W)
E (PDIP) Package	67
M (SOIC) Package	73
Maximum Junction Temperature	
Maximum Storage Temperature Range	65 <sup>0</sup> C to 150 <sup>0</sup> C
Maximum Lead Temperature (Soldering 10s)	
(SOIC - Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

#### **DC Electrical Specifications**

		TEST CONDITIONS		V <sub>CC</sub>	25 <sup>0</sup> C			-40°C TO 85°C		-55°C TO 125°C		4
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES					-		-	-	-	-	_	-
High Level Input	VIH	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	VIL	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output	1		-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output	1		-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V

## CD54HC251, CD74HC251, CD54HCT251, CD74HCT251

		TES CONDI		Vcc		25 <sup>0</sup> C		-40 <sup>о</sup> С т	O 85°C	-55 <sup>0</sup> С Т	O 125 <sup>0</sup> C	
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Input Leakage Current	lı	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA
Three-State Leakage Current	-	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	6	-	-	±0.5	-	±5.0	-	±10	μΑ
HCT TYPES												
High Level Input Voltage	VIH	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	VIL	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V <sub>CC</sub> and GND	0	5.5	-		±0.1	-	±1	-	±1	μA
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Three-State Leakage Current	-	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	6	-	-	±0.5	-	±5.0	-	±10	μΑ
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	∆I <sub>CC</sub> (Note 2)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

2. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

### **HCT Input Loading Table**

INPUT	UNIT LOADS
S0, S1, S2	0.55
10 - 17	0.5
ŌĒ	2.65

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

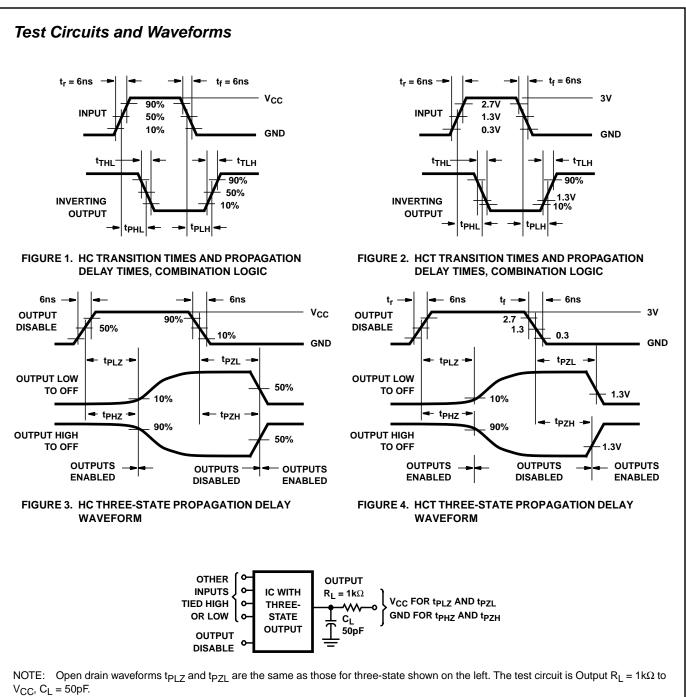
## CD54HC251, CD74HC251, CD54HCT251, CD74HCT251

#### Switching Specifications Input tr, tf = 6ns

		TEST			25 <sup>0</sup> C			с то °С		C TO 5°C	
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	MIN	ТҮР	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES	•										
Propagation Delay	<sup>t</sup> PLH, <sup>t</sup> PHL	C <sub>L</sub> = 50pF	2	-	-	245	-	305	-	370	ns
Select to Outputs			4.5	-	-	49	-	61	-	74	ns
		C <sub>L</sub> =15pF	5	-	21	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	42	-	52	-	63	ns
Data to Outputs	<sup>t</sup> PLH, <sup>t</sup> PHL	C <sub>L</sub> = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		C <sub>L</sub> =15pF	5	-	12	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	30	-	37	-	45	ns
Enable to High Z and Enable	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	140	-	175	-	210	ns
from High Z			4.5	-	-	28	-	35	-	42	ns
		C <sub>L</sub> =15pF	5	-	11	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	24	-	30	-	36	ns
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C <sub>IN</sub>	-	-	-	-	10	-	10	-	10	pF
Three-State Output Capacitance	со	-	-	-	-	15	-	15	-	15	pF
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	-	5	-	60	-	-	-	-	-	pF
HCT TYPES			<u>.</u>								
Propagation Delay	t <sub>PLH</sub> , t <sub>PHL</sub>										
Select to Outputs		C <sub>L</sub> = 50pF	4.5	-	-	42	-	53	-	63	ns
		C <sub>L</sub> =15pF	5	-	18	-	-		-	-	ns
Data to Outputs	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	35	-	44	-	53	ns
		C <sub>L</sub> =15pF	5	-	12	-	-	-	-	-	ns
Enable to High Z and Enable	t <sub>PLH</sub> , t <sub>PHL</sub>	$C_L = 50 pF$	4.5	-		30	-	38	-	45	ns
from High Z		C <sub>L</sub> =15pF	5	-	12	-	-	-	-	-	ns
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C <sub>IN</sub>	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	-	5		60	-	-	-	-	-	pF

NOTES:

3.  $C_{PD}$  is used to determine the dynamic power consumption, per package. 4.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.



#### FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT



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### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-9052401MEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
CD54HC251F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD54HC251F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD54HCT251F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD74HC251E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC251EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC251M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC251M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC251M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC251M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC251ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC251MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC251MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC251MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC251MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT251E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT251EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT251M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT251M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT251M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CD74HCT251M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT251ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT251MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT251MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT251MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT251MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and package, or 2) lead-based die adhesive used between the die and pa

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF CD54HC251, CD54HCT251, CD74HC251, CD74HCT251 :

• Catalog: CD74HC251, CD74HCT251

• Military: CD54HC251, CD54HCT251

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

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### TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC251M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT251M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1



## PACKAGE MATERIALS INFORMATION

19-Mar-2008



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC251M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT251M96	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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# D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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