# CD54ACT151, CD74ACT151 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCHS338 - MARCH 2003

- Inputs Are TTL-Voltage Compatible
- 8-Line to 1-Line Multiplexers Can Perform as:
  - Boolean Function Generators
  - Parallel-to-Serial Converters
  - Data Source Selectors
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ±24-mA Output Drive Current
  - Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883. Method 3015

#### CD54ACT151...F PACKAGE CD74ACT151... M PACKAGE (TOP VIEW) 16 V<sub>CC</sub> D3 D2 **1**2 15 D4 D1 [ 14 D5 D0 **∏** 4 13 D6 Υ 12 D7 W 11 **∏** A 6 G 10 🛮 B GND 8 9] C

#### description/ordering information

These data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe  $(\overline{G})$  input must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

#### ORDERING INFORMATION

| TA             | PACKA    | AGE†          | ORDERABLE<br>PART NUMBER | TOP-SIDE<br>MARKING |  |
|----------------|----------|---------------|--------------------------|---------------------|--|
| –55°C to 125°C | SOIC - M | Tape and reel | CD74ACT151M96            | ACT151M             |  |
| -55°C 10 125°C | CDIP – F | Tube          | CD54ACT151F3A            | CD54ACT151F3A       |  |

T Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

|   | II            | OUTI | PUTS |    |    |
|---|---------------|------|------|----|----|
| , | SELECT STROBE |      |      |    | w  |
| С | В             | Α    | G    | '  | ** |
| Х | Х             | Х    | Н    | L  | Н  |
| L | L             | L    | L    | D0 | D0 |
| L | L             | Н    | L    | D1 | D1 |
| L | Н             | L    | L    | D2 | D2 |
| L | Н             | Н    | L    | D3 | D3 |
| Н | L             | L    | L    | D4 | D4 |
| Н | L             | Н    | L    | D5 | D5 |
| Н | Н             | L    | L    | D6 | D6 |
| Н | н н н         |      | L    | D7 | D7 |

D0, D1 . . . D7 = the level of the respective D input

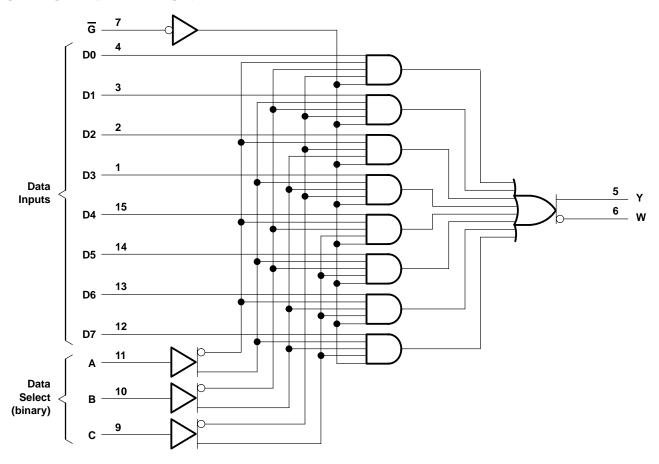


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SCHS338 - MARCH 2003

#### logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| Supply voltage range, V <sub>CC</sub>  | 0.5 V to 6 V   |
|--|----------------|
| Input clamp current, $I_{IK}$ ( $V_I < 0 \text{ V or } V_I > V_{CC}$ ) (see Note 1)                            |                |
| Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>CC</sub> ) (see Note 1) |                |
| Continuous output current, I <sub>O</sub> (V <sub>O</sub> > 0 V or V <sub>O</sub> < V <sub>CC</sub> )          | ±50 mA         |
| Continuous current through V <sub>CC</sub> or GND  | ±100 mA        |
| Package thermal impedance, $\hat{\theta}_{JA}$ (see Note 2   | 73°C/W         |
| Storage temperature range, T <sub>stq</sub>  | –65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



SCHS338 - MARCH 2003

#### recommended operating conditions (see Note 3)

|       |                                    | T <sub>A</sub> = 1  | T <sub>A</sub> = 25°C |     | T <sub>A</sub> = 25°C |     | C to<br>°C | –40°C to<br>85°C |  | UNIT |
|-------|------------------------------------|---------------------|-----------------------|-----|-----------------------|-----|------------|------------------|--|------|
|       |                                    | MIN MAX MIN MAX MIN |                       | MIN | MAX                   |     |            |                  |  |      |
| Vcc   | Supply voltage                     | 4.5                 | 5.5                   | 4.5 | 5.5                   | 4.5 | 5.5        | V                |  |      |
| VIH   | High-level input voltage           | 2                   |                       | 2   |                       | 2   |            | V                |  |      |
| VIL   | Low-level input voltage            |                     | 0.8                   |     | 0.8                   |     | 0.8        | V                |  |      |
| ٧I    | Input voltage                      | 0                   | VCC                   | 0   | VCC                   | 0   | VCC        | V                |  |      |
| ٧o    | Output voltage                     | 0                   | VCC                   | 0   | VCC                   | 0   | VCC        | V                |  |      |
| IOH   | High-level output current          |                     | -24                   |     | -24                   |     | -24        | mA               |  |      |
| loL   | Low-level output current           |                     | 24                    |     | 24                    |     | 24         | mA               |  |      |
| Δt/Δν | Input transition rise or fall rate |                     | 10                    |     | 10                    |     | 10         | ns/V             |  |      |

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER          | TEST CON                         | Vcc                                 | T <sub>A</sub> = 25°C |      | –55°C to<br>125°C |      | –40°C to<br>85°C |      | UNIT |    |  |
|--------------------|----------------------------------|-------------------------------------|-----------------------|------|-------------------|------|------------------|------|------|----|--|
|                    |                                  |                                     |                       | MIN  | MAX               | MIN  | MAX              | MIN  | MAX  |    |  |
|                    |                                  | ΙΟΗ = -50 μΑ                        | 4.5 V                 | 4.4  |                   | 4.4  |                  | 4.4  |      |    |  |
| V                  | \\. = \\ or \\.                  | $I_{OH} = -24 \text{ mA}$           | 4.5 V                 | 3.94 |                   | 3.7  |                  | 3.8  |      | ., |  |
| VOH                | $V_I = V_{IH}$ or $V_{IL}$       | $I_{OH} = -50 \text{ mA}^{\dagger}$ | 5.5 V                 |      |                   | 3.85 |                  |      |      | V  |  |
|                    |                                  | $I_{OH} = -75 \text{ mA}^{\dagger}$ | 5.5 V                 |      |                   |      |                  | 3.85 |      |    |  |
|                    |                                  | I <sub>OL</sub> = 50 μA             | 4.5 V                 |      | 0.1               |      | 0.1              |      | 0.1  |    |  |
| V                  | VI = VIH or VIL                  | I <sub>OL</sub> = 24 mA             | 4.5 V                 |      | 0.36              |      | 0.5              |      | 0.44 | V  |  |
| VOL                |                                  | I <sub>OL</sub> = 50 mA†            | 5.5 V                 |      |                   |      | 1.65             |      |      | V  |  |
|                    |                                  | $I_{OL} = 75 \text{ mA}^{\dagger}$  | 5.5 V                 |      |                   |      |                  |      | 1.65 |    |  |
| IĮ                 | $V_I = V_{CC}$ or GND            |                                     | 5.5 V                 |      | ±0.1              |      | ±1               |      | ±1   | μΑ |  |
| Icc                | $V_I = V_{CC}$ or GND,           | IO = 0                              | 5.5 V                 |      | 8                 |      | 160              |      | 80   | μΑ |  |
| Δl <sub>CC</sub> ‡ | $V_{I} = V_{CC} - 2.1 \text{ V}$ |                                     | 4.5 V to 5.5 V        |      | 2.4               |      | 3                |      | 2.8  | mA |  |
| Ci                 |                                  |                                     |                       |      | 10                |      | 10               |      | 10   | pF |  |

Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C. Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

#### **ACT INPUT LOAD TABLE**

| INPUT      | UNIT LOAD |
|------------|-----------|
| D          | 1         |
| G          | 1         |
| A, B, or C | 1         |

Unit Load is  $\Delta I_{CC}$  limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).



# CD54ACT151, CD74ACT151 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCHS338 - MARCH 2003

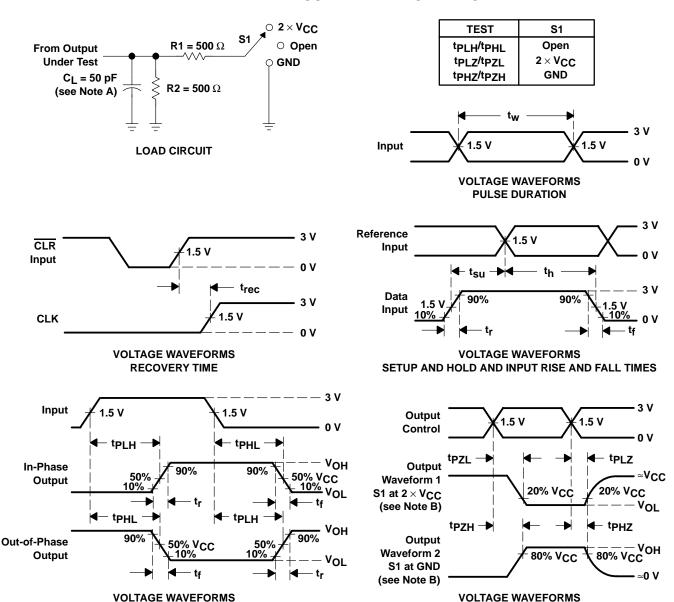
# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | −55°<br>125 |      | –40°C to<br>85°C |      | UNIT |
|------------------|-----------------|----------------|-------------|------|------------------|------|------|
|                  | (1141 01)       | (6611 61)      | MIN         | MAX  | MIN              | MAX  |      |
| t <sub>PLH</sub> | D               | Y              | 3.9         | 15.5 | 4                | 14.1 | ns   |
| t <sub>PHL</sub> | ט               | r              | 3.9         | 15.5 | 4                | 14.1 | 115  |
| <sup>t</sup> PLH | D               |                | 4.2         | 16.9 | 4.4              | 15.4 | ns   |
| <sup>t</sup> PHL |                 | W              | 4.2         | 16.9 | 4.4              | 15.4 | 115  |
| <sup>t</sup> PLH | A, B, or C      | Υ              | 5.1         | 20.2 | 5.2              | 18.4 | ns   |
| <sup>t</sup> PHL |                 | T              | 5.1         | 20.2 | 5.2              | 18.4 | 113  |
| <sup>t</sup> PLH | A, B, or C      |                | 5.4         | 21.6 | 5.6              | 19.6 | no   |
| t <sub>PHL</sub> | A, B, OI C      | W              | 5.4         | 21.6 | 5.6              | 19.6 | ns   |
| t <sub>PLH</sub> | G               | V              | 3           | 12.1 | 3.1              | 11   | ns   |
| t <sub>PHL</sub> | 9               | Υ              | 3           | 12.1 | 3.1              | 11   | 115  |
| <sup>t</sup> PLH | G               | W              | 3.4         | 13.5 | 3.5              | 12.3 | nc   |
| <sup>t</sup> PHL | 9               | VV             | 3.4         | 13.5 | 3.5              | 12.3 | ns   |

# operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

|                 | PARAMETER                     | TYP | UNIT |
|-----------------|-------------------------------|-----|------|
| C <sub>pd</sub> | Power dissipation capacitance | 120 | pF   |

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and test-fixture capacitance.

PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \ \Omega$ ,  $t_f = 3 \ ns$ ,  $t_f = 3 \ ns$ . Phase relationships between waveforms are arbitrary.

**OUTPUT ENABLE AND DISABLE TIMES** 

- D. For clock inputs, f<sub>max</sub> is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. tpLH and tpHL are the same as tpd.
- G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- H. tpLZ and tpHZ are the same as tdis.
- I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



#### PACKAGE OPTION ADDENDUM

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#### **PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package<br>Type | Package<br>Drawing | Pins | Package<br>Qty | e Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|-----------------|--------------------|------|----------------|---------------------------|------------------|------------------------------|
| CD54ACT151F3A    | ACTIVE                | CDIP            | J                  | 16   | 1              | TBD                       | A42              | N / A for Pkg Type           |
| CD74ACT151M96    | ACTIVE                | SOIC            | D                  | 16   | 2500           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74ACT151M96E4  | ACTIVE                | SOIC            | D                  | 16   | 2500           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74ACT151M96G4  | ACTIVE                | SOIC            | D                  | 16   | 2500           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <a href="http://www.ti.com/productcontent">http://www.ti.com/productcontent</a> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### TAPE AND REEL INFORMATION



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

|    | Dimension designed to accommodate the component width     |
|----|---|
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

| Device        | Package<br>Type | Package<br>Drawing |    |      | Reel<br>Diameter<br>(mm) | Reel<br>Width<br>W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1<br>(mm) | W<br>(mm) | Pin1<br>Quadrant |
|---------------|-----------------|--------------------|----|------|--------------------------|--------------------------|---------|---------|---------|------------|-----------|------------------|
| CD74ACT151M96 | SOIC            | D                  | 16 | 2500 | 330.0                    | 16.4                     | 6.5     | 10.3    | 2.1     | 8.0        | 16.0      | Q1               |





#### \*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74ACT151M96 | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |

### 14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# D (R-PDS0-G16)

#### PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# D (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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