

Data sheet acquired from Harris Semiconductor

CD74AC251, CD74ACT251

August 1998

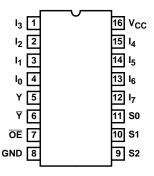
8-Input Multiplexer, Three-State

Features

- Buffered Inputs
- Typical Propagation Delay
 - 6ns at $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 50pF$
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption
- Balanced Propagation Delays
- AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply
- ±24mA Output Drive Current
 - Fanout to 15 FAST™ ICs
 - Drives 50Ω Transmission Lines

Pinout

CD74AC251, CD74ACT251 (PDIP, SOIC) TOP VIEW



Description

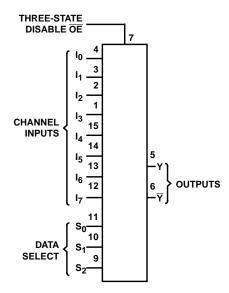
The CD74AC251 and CD74ACT251 8-input multiplexers that utilize the Harris Advanced CMOS Logic technology. This multiplexer features both true (Y) and complement (\overline{Y}) outputs as well as an Output Enable (\overline{OE}) input. The OE must be at a LOW logic level to enable this device. When the \overline{OE} input is HIGH, both outputs are in the high-impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and \overline{Y} outputs.

Ordering Information

PART NUMBER	TEMP. RANGE (^o C)	PACKAGE	PKG. NO.
CD74AC251E	0 to 70 ^o C, -40 to 85, -55 to 125	16 Ld PDIP	E16.3
CD74ACT251E	0 to 70°C, -40 to 85, -55 to 125	16 Ld PDIP	E16.3
CD74AC251M	0 to 70°C, -40 to 85, -55 to 125	16 Ld SOIC	M16.15
CD74ACT251M	0 to 70°C, -40 to 85, -55 to 125	16 Ld SOIC	M16.15

- 1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
- Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Functional Diagram



TRUTH TABLE

	INPUTS						
	SELECT	-					
S2	S1	S0	OUTPUT ENABLE OE	Y	Y		
Х	Х	Х	Н	Z	Z		
L	L	L	L	I ₀	Īō		
L	L	Н	L	I ₁	ĪΤ		
L	Н	L	L	l ₂	Ī₂		
L	Н	Н	L	I ₃	Ī ₃		
Н	L	L	L	l ₄	Ī ₄		
Н	L	Н	L	l ₅	Ī <u>5</u>		
Н	Н	L	L	I ₆	Ī _ē		
Н	Н	Н	L	l ₇	Ī 7		

$$\label{eq:Hamiltonian} \begin{split} H &= \text{High logic level, L} = \text{Low logic level, Z} = \text{High impedance (off),} \\ X &= \text{Irrelevant, I}_0, \, \text{I}_1...\text{I}_7 = \text{The level of the respective input} \end{split}$$

Absolute Maximum Ratings

DC Supply Voltage, VCC ... -0.5V to 6V DC Input Diode Current, I $_{\rm IK}$ For V $_{\rm I}$ < -0.5V or V $_{\rm I}$ > VCC + 0.5V ±20mA DC Output Diode Current, I $_{\rm OK}$ For V $_{\rm O}$ < -0.5V or V $_{\rm O}$ > VCC + 0.5V ±50mA DC Output Source or Sink Current per Output Pin, I $_{\rm O}$ For V $_{\rm O}$ > -0.5V or V $_{\rm O}$ < VCC + 0.5V ±50mA DC V $_{\rm CC}$ or Ground Current, I $_{\rm CC}$ or I $_{\rm GND}$ (Note 3) ... ±100mA

Thermal Information

Thermal Resistance (Typical, Note 5)	θ _{JA} (^o C/W)
PDIP Package	·
SOIC Package	
Maximum Junction Temperature (Plastic Package)	150 ⁰ C
Maximum Storage Temperature Range	65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	

Operating Conditions

Temperature Range, T _A 55°C to 125°C Supply Voltage Range, V _{CC} (Note 4)
AC Types
**
ACT Types
DC Input or Output Voltage, V _I , V _O
Input Rise and Fall Slew Rate, dt/dv
AC Types, 1.5V to 3V 50ns (Max)
AC Types, 3.6V to 5.5V
ACT Types, 4.5V to 5.5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- 3. For up to 4 outputs per device, add ± 25 mA for each additional output.
- 4. Unless otherwise specified, all voltages are referenced to ground.
- 5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

		1	TEST CONDITIONS		25	°c		C TO °C		C TO 5°C	
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
AC TYPES											
High Level Input Voltage	V _{IH}	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
Low Level Input Voltage	V _{IL}	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V

DC Electrical Specifications (Continued)

		TEST CONDITIONS		v _{cc}	25	°c		C TO °C	-55°C TO 125°C		
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Low Level Output Voltage	V_{OL}	V _{IH} or V _{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	Ι _Ι	V _{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	μА
Three-State Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND	-	5.5	-	±0.5	-	±5	-	±10	μА
Quiescent Supply Current MSI	I _{CC}	V _{CC} or GND	0	5.5	-	8	-	80	-	160	μΑ
ACT TYPES											
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V_{OL}	V _{IH} or V _{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I _I	V _{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	μΑ
Three-State or Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND	-	5.5	-	±0.5	-	±5	-	±10	μА
Quiescent Supply Current MSI	Icc	V _{CC} or GND	0	5.5	-	8	-	80	-	160	μА
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	Δl _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

- 6. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- 7. Test verifies a minimum 50Ω transmission-line-drive capability at 85° C, 75Ω at 125° C.

ACT Input Load Table

INPUT	UNIT LOAD
S0, S1, S3	1
OE	1
I ₀ - I ₇	1

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

Switching Specifications Input t_r , t_f = 3ns, C_L = 50pF (Worst Case)

			-40 ⁴	C TO 85°	С	-55	^O C TO 12	5°C	
PARAMETER	SYMBOL	V _{CC} (V)	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
AC TYPES		:		•		•		•	•
Propagation Delay,	t _{PLH} , t _{PHL}	1.5	-	-	153	-	-	169	ns
Data to Y Output		3.3 (Note 9)	4.9	-	17.2	4.7	-	18.9	ns
		5 (Note 10)	3.5	-	12.3	3.4	-	13.5	ns
Propagation Delay,	t _{PLH} , t _{PHL}	1.5	-	-	169	-	-	186	ns
Data to		3.3	5.4	-	19	5.2	-	20.9	ns
		5	3.8	-	13.5	3.7	-	14.9	ns
Propagation Delay,	t _{PLH} , t _{PHL}	1.5	=	-	207	-	-	228	ns
Select to Y Output		3.3	6.6	-	23.2	6.4	-	25.5	ns
		5	4.7	-	16.5	4.6	-	18.2	ns
Propagation Delay,	t _{PLH} , t _{PHL}	1.5	-	-	223	-	-	245	ns
Select to \overline{Y} Output		3.3	7.1	-	24.9	6.9	-	27.4	ns
		5	5.1	-	17.8	4.9	-	19.6	ns
Propagation Delay,	t _{PZH} , t _{PZL} , t _{PHZ} , t _{PLZ}	1.5	-	-	155	-	-	169	ns
Output Enable and Output Disable to Output		3.3	5.2	-	18.7	5.1	-	20.3	ns
		5	3.5	-	12.3	3.4	-	13.5	ns
Three-State Output Capacitance	CO	-	-	-	15	-	-	15	pF
Input Capacitance	C _I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C _{PD} (Note 11)	-	-	120	-	-	120	-	pF
ACT TYPES									•
Propagation Delay, Data to Y Output	t _{PLH} , t _{PHL}	5 (Note 10)	3.5	-	12.3	3.4	-	13.5	ns
Propagation Delay, Data to ₹ Output	t _{PLH} , t _{PHL}	5	3.8	-	13.5	3.7	-	14.9	ns
Propagation Delay, Select to Y Output	t _{PLH} , t _{PHL}	5	4.7	-	16.5	4.6	-	18.2	ns
Propagation Delay, Select to ₹ Output	t _{PLH} , t _{PHL}	5	5.1	-	17.8	4.9	-	19.6	ns
Propagation Delay, Output Enable and Output Disable to Output	t _{PZH} , t _{PZL} , t _{PHZ} , t _{PLZ}	5	3.5	-	12.3	3.4	-	13.5	ns

Switching Specifications Input t_r , t_f = 3ns, C_L = 50pF (Worst Case) (Continued)

			-40°C TO 85°C			-55			
PARAMETER	SYMBOL	V _{CC} (V)	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Three-State Output Capacitance	CO								
Input Capacitance	Cl	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C _{PD} (Note 11)	-	-	45	-	-	45	-	pF

- 8. Limits tested 100%.
- 9. 3.3V Min is at 3.6V. Max is at 3V.
- 10. 5V Min is at 5.5V, Max is at 4.5V.
- 11. C_{PD} is used to determine the dynamic power consumption per device. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i input frequency, C_L is output load capacitance, V_{CC} is supply voltage.

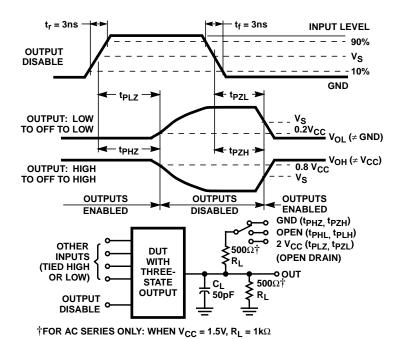


FIGURE 1. THREE-STATE PROPAGATION DELAY WAVEFORMS AND TEST CIRCUIT

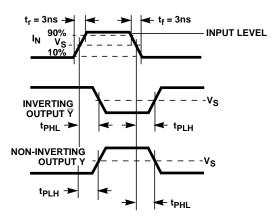
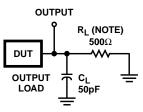


FIGURE 2. PROPAGATION DELAY TIMES



NOTE: For AC Series Only: When V_{CC} = 1.5V, R_L = 1k Ω .

	CD74AC	CD74ACT
Input Level	V _{CC}	3V
Input Switching Voltage, V _S	0.5 V _{CC}	1.5V
Output Switching Voltage, V _S	0.5 V _{CC}	0.5 V _{CC}

FIGURE 3. PROPAGATION DELAY TIMES





.com 23-Apr-2007

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74AC251M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC251M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC251M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC251M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC251ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC251MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC251M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC251M96	SOIC	D	16	2500	333.2	345.9	28.6

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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