

# CD54HC283, CD74HC283, CD54HCT283

Data sheet acquired from Harris Semiconductor SCHS176D

November 1997 - Revised October 2003

## High-Speed CMOS Logic 4-Bit Binary Full Adder with Fast Carry

#### Features

- Adds Two Binary Numbers
- · Full Internal Lookahead
- Fast Ripple Carry for Economical Expansion
- Operates with Both Positive and Negative Logic
- Fanout (Over Temperature Range)
- Bus Driver Outputs ...... 15 LSTTL Loads
- Wide Operating Temperature Range  $\ldots$  -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL}$  = 30%,  $N_{IH}$  = 30% of  $V_{CC}$  at  $V_{CC}$  = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,
     V<sub>IL</sub>= 0.8V (Max), V<sub>IH</sub> = 2V (Min)
  - CMOS Input Compatibility, I<sub>I</sub>  $\leq$  1 $\mu$ A at V<sub>OL</sub>, V<sub>OH</sub>

### Description

The 'HC283 and 'HCT283 binary full adders add two 4-bit binary numbers and generate a carry-out bit if the sum exceeds 15.

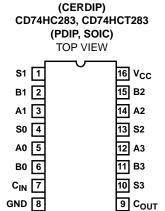
Because of the symmetry of the add function, this device can be used with either all active-high operands (positive logic) or with all active-low operands (negative logic). When using positive logic the carry-in input must be tied low if there is no carry-in.

### **Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC283F3A	-55 to 125	16 Ld CERDIP
CD54HCT283F3A	-55 to 125	16 Ld CERDIP
CD74HC283E	-55 to 125	16 Ld PDIP
CD74HC283M	-55 to 125	16 Ld SOIC
CD74HC283MT	-55 to 125	16 Ld SOIC
CD74HC283M96	-55 to 125	16 Ld SOIC
CD74HCT283E	-55 to 125	16 Ld PDIP
CD74HCT283M	-55 to 125	16 Ld SOIC
CD74HCT283MT	-55 to 125	16 Ld SOIC
CD74HCT283M96	-55 to 125	16 Ld SOIC

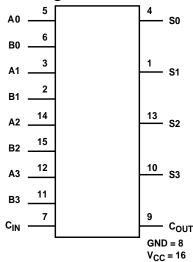
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

### **Pinout**



CD54HC283, CD54HCT283

### Functional Diagram



#### **Absolute Maximum Ratings** DC Supply Voltage, V $_{CC}$ .....-0.5V to 7V DC Input Diode Current, I<sub>IK</sub> For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ..... $\pm 20$ mA DC Output Diode Current, $I_{OK}$ For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ......±20mA DC Drain Current, per Output, IO For $-0.5V < V_O < V_{CC} + 0.5V$ ......±25mA DC Output Source or Sink Current per Output Pin, IO

#### **Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
E (PDIP) Package	67
M (SOIC) Package	73
Maximum Junction Temperature	150 <sup>0</sup> C
Maximum Storage Temperature Range	65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300 <sup>o</sup> C
(SOIC - Lead Tips Only)	

#### **Operating Conditions**

Temperature Range, T <sub>A</sub>	55°C to 125°C
Supply Voltage Range, V <sub>CC</sub>	
HC Types	2V to 6V
DC Input or Output Voltage, V <sub>I</sub> , V <sub>O</sub>	0V to V <sub>CC</sub>
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6\/	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

1. The package thermal impedance is calculated in accordance with JESD 51-7.

### **DC Electrical Specifications**

		TE: CONDI		V <sub>CC</sub>		25°C		-40°C 1	O 85°C	-55°C T	O 125°C							
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(S)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS						
HC TYPES																		
High Level Input	V <sub>IH</sub>	-	-	2	1.5	-	-	1.5	-	1.5	-	V						
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	>						
				6	4.2	-	-	4.2	-	4.2	-	V						
Low Level Input	V <sub>IL</sub>	-	-	2	-	-	0.5	-	0.5	-	0.5	V						
Voltage										4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V						
High Level Output	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	2	1.9	-	-	1.9	-	1.9	-	V						
Voltage CMOS Loads			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V						
OWOO LOAGS			-0.02	6	5.9	-	-	5.9	-	5.9	-	V						
High Level Output	7		-	-	-	-	-	-	-	-	-	V						
Voltage TTL Loads				-4	4.5	3.98	-	-	3.84	-	3.7	-	V					
TTE LOGUS			-5.2	6	5.48	-	-	5.34	-	5.2	-	V						
Low Level Output	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	2	-	-	0.1	-	0.1	-	0.1	V						
Voltage CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V						
CIVIOS LOAGS		-	-	f	F	-	, <b> </b>	1	0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output	1		-	-	-	-	-	-	-	-	-	V						
Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V						
TTL LUaus			5.2	6	-	-	0.26	-	0.33	-	0.4	V						
Input Leakage Current	II	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μΑ						
Quiescent Device Current	lcc	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μΑ						

### DC Electrical Specifications (Continued)

		TES CONDI		V <sub>CC</sub>		25°C		-40°C 1	O 85°C	-55°C TO 125°C		
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HCT Types					-	-	-	-	-			
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	Voн	V <sub>IL</sub> or V <sub>IH</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads	V <sub>ОН</sub>	V <sub>IL</sub> or V <sub>IH</sub>	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lį	V <sub>CC</sub> to GND	-	5.5	-	-	±0.1	-	±1	-	±1	μΑ
Quiescent Device Current	ICC	V <sub>CC</sub> or GND	-	5.5	-	-	8	-	80	-	160	μА
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μΑ

### NOTE:

### **HCT Input Loading Table**

INPUT	UNIT LOADS
C <sub>IN</sub>	1.5
B1, A1, A0	1
В0	0.4
B3, A3, A2, B2	0.5

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g., 360 $\mu A$  max at  $25^{o}C.$ 

### **Switching Specifications** Input t<sub>r</sub>, t<sub>f</sub> = 6ns

		TEST	TEST		25°C			-40°C TO 85°C		-55°C TO 125°C	
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES											
Propagation Delay	t <sub>PLH</sub> , t <sub>PHL</sub>	$C_L = 50pF$	2	-	-	160	-	200	-	240	ns
C <sub>IN</sub> to S0			4.5	-	-	32	-	40	-	48	ns
		C <sub>L</sub> = 15pF	5	-	13	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	i	-	27	-	34	ı	41	ns

<sup>2.</sup> For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

### Switching Specifications Input $t_{\rm f},\,t_{\rm f}=6{\rm ns}$ (Continued)

		TEST			25°C			C TO °C		C TO 5°C	
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
C <sub>IN</sub> to S1	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	180	-	225	-	270	ns
			4.5	-	-	36	-	45	-	54	ns
		C <sub>L</sub> = 15pF	5	-	15	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	31	-	38	-	46	ns
C <sub>IN</sub> to S2, C <sub>IN</sub> to C <sub>OUT</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	195	-	245	-	295	ns
			4.5	-	-	39	-	49	-	59	ns
		C <sub>L</sub> = 15pF	5	-	16	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	33	-	42	-	50	ns
C <sub>IN</sub> to S3	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	230	-	290	-	345	ns
			4.5	-	-	46	-	58	-	69	ns
		C <sub>L</sub> = 15pF	5	-	19	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	39	-	49	-	59	ns
An, Bn to C <sub>OUT</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	195	-	245	-	295	ns
			4.5	-	-	39	-	49	-	59	ns
		C <sub>L</sub> = 15pF	5	-	16	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	33	-	42	-	50	ns
An, Bn to Sn	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	210	-	265	-	315	ns
			4.5	-	-	42	-	53	-	63	ns
		C <sub>L</sub> = 15pF	5	-	18	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	36	-	45	-	54	ns
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C <sub>IN</sub>	C <sub>L</sub> = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance, (Notes 3, 4)	C <sub>PD</sub>	-	5	-	70	-	-	-	-	-	pF
HCT TYPES	<b>I</b>										
Propagation Delay											
C <sub>IN</sub> to S0	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 15pF	5	-	13	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	4.5	-	-	31	-	39	-	47	ns
C <sub>IN</sub> to S1	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 15pF	5	-	18	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	4.5	-		43	-	54	-	65	ns
C <sub>IN</sub> to S2, C <sub>IN</sub> to C <sub>OUT</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 15pF	5	-	19	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	4.5	-		46	-	58	-	69	ns
C <sub>IN</sub> to S3	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 15pF	5	-	22	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	4.5	-		53	-	66	-	80	ns
An, Bn to C <sub>OUT</sub>	t <sub>PLH</sub> , t <sub>PH</sub> L	C <sub>L</sub> = 15pF	5	-	20	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	4.5	-		48	-	60	-	72	ns
An, Bn to Sn	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 15pF	5	-	21	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	4.5	-		49	-	61	-	74	ns
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	4.5	-		15	-	19	-	22	ns

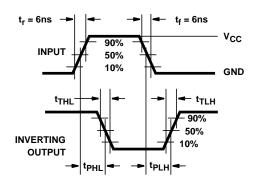
### Switching Specifications Input $t_r$ , $t_f = 6ns$ (Continued)

		TEST			25°C		-40 <sup>0</sup> ( 85	с то °С	-55 <sup>0</sup> ( 125		
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Input Capacitance	C <sub>IN</sub>	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance, (Notes 3, 4)	C <sub>PD</sub>	-	5	-	82	-	-	-	-	-	pF

#### NOTES:

- 3.  $C_{\mbox{\scriptsize PD}}$  is used to determine the dynamic power consumption, per package.
- 4.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where:  $f_i = Input$  Frequency,  $C_L = Output$  Load Capacitance,  $V_{CC} = Supply$  Voltage.

### Test Circuits and Waveforms



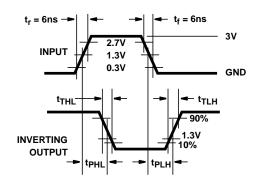


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGA-TION DELAY TIMES, COMBINATION LOGIC

FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

5-Sep-2011

### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-8976501EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
CD54HC283F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD54HCT283F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD74HC283E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC283EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC283M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC283M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC283M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC283M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC283ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC283MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC283MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC283MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC283MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT283E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT283EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT283M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT283M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT283M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT283M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





5-Sep-2011

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CD74HCT283ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT283MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT283MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT283MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT283MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD54HC283, CD54HCT283, CD74HC283, CD74HCT283:





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● Catalog: CD74HC283, CD74HCT283

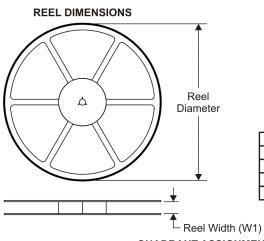
• Military: CD54HC283, CD54HCT283

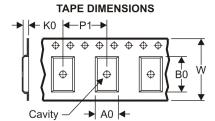
NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications



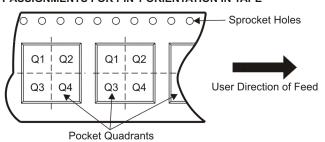
### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

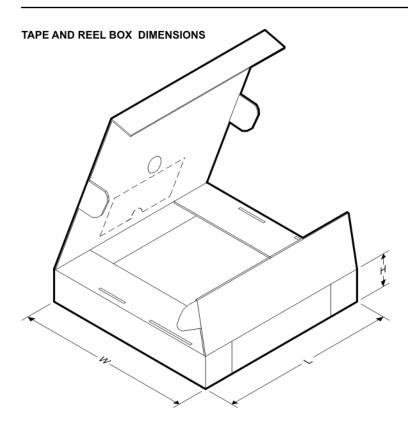
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC283M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT283M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1





\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC283M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT283M96	SOIC	D	16	2500	333.2	345.9	28.6

#### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

### N (R-PDIP-T\*\*)

### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



### D (R-PDS0-G16)

### PLASTIC SMALL OUTLINE

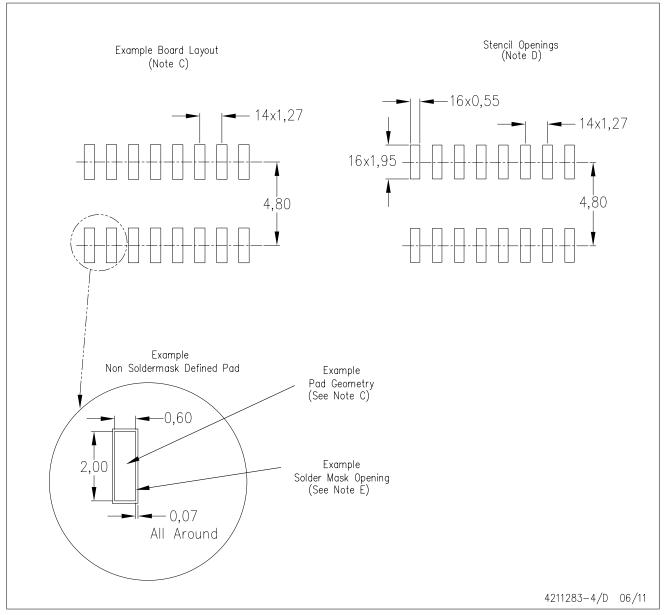


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



## D (R-PDSO-G16)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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