SDLS147 - SEPTEMBER 1972 - REVISED MARCH 1988

- Three-State Version of SN54/74LS153, SN54/74S153
- Schottky-Diode-Clamped Transistors
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to Serial Conversion
- Fully Compatible with Most TTL Circuits
- Low Power Dissipation
 1 S253
 35 mW Typic

'LS253 . . . 35 mW Typical 'S253 . . . 225 mW Typical

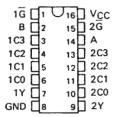
description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

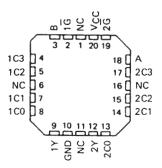
The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

SN54LS253, SN54S253 . . . J OR W PACKAGE SN74LS253, SN74S253 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS253, SN54S253 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

FUNCTION TABLE

1	ECT UTS		DATA	INPUTS		OUTPUT CONTROL	ОUТРUТ
В	Α	CO	C1	C2	C3	Ğ	Υ
X	X	X	X	X	X	Н	Z
Ł	L	L	X	X	X	L	L
L	L	Н	X	X	X	L	н
L	Н	×	L	X	Х	L	L
L	Н	×	Н	X	X	L	н
Н	L	×	×	L	×	L	L
н	L	×	X	Н	X	L	Н
H	Н	×	X	X	L	L	L
Н	H	X	X	X	Н	L	Н

Address inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

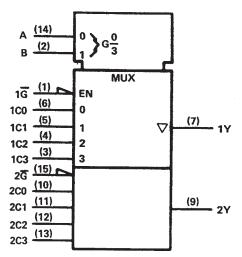
Supply voltage, VCC (see Note 1)	7 V
Input voltage: 'LS253	7 V
'\$253	5.5 V
Off-state output voltage	
Operating free-air temperature range: SN54LS253, SN54S253	125°C
SN74LS253, SN74S253 0°C t	
Storage temperature range – 65°C to	150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS

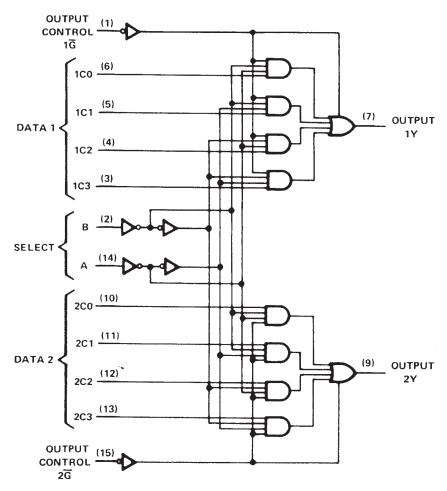
SDLS147 - SEPTEMBER 1972 - REVISED MARCH 1988

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

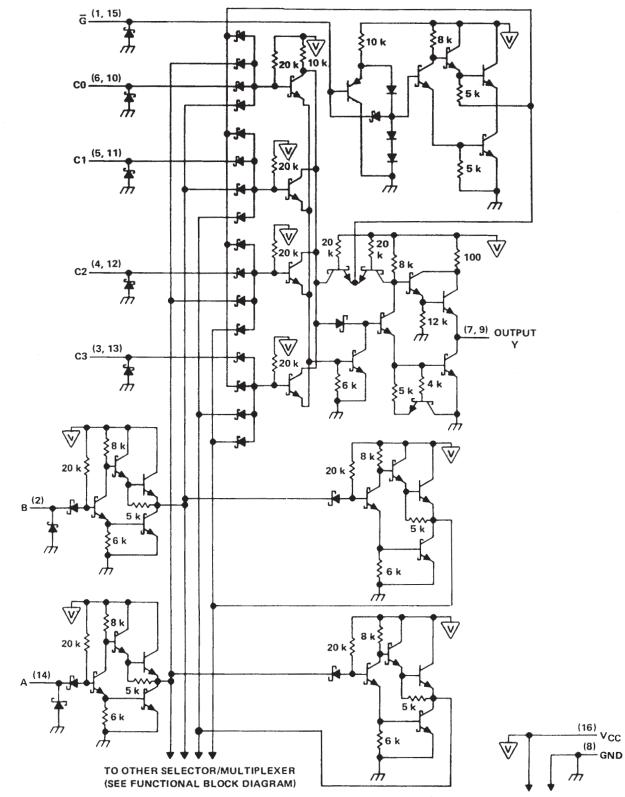
logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.



schematic (each selector/multiplexer, and the common select section)



Pin numbers shown are for D, J, N, and W packages.



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recommended operating conditions

		s	SN54LS253			SN74LS253			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
Іон	High-level output current			- 1			- 2.6	mA	
IOL	Low-level output current			4			8	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITI	onet		S	N54LS2	53	S	N74LS2	53	
FANAMETEN		MIN	TYP \$	MAX	MIN	TYP‡	MAX	UNIT			
VIK	V _{CC} = MIN,	$I_1 = -18 \text{ mA}$					- 1.5			- 1.5	V
VOH	V _{CC} = MIN,	V _{IH} = 2 V,	VIL = MAX,	1 _{OH} = MAX	2.4	3.4		2.4	3.1		V
VOL	V _{CC} = MIN,	V _{IH} = 2 V,	1/ - 14AV	IOL = 4 mA		0.25	0.4		0.25	0.4	V
VOL	ACC - MIIA	VIH - 2 V,	VIL = MAX	IOL = 8 mA		****			0.25	0.5	
loz	VCC = MAX,	V _{IH} = 2 V		V _O = 2.7 V			20			20	
102	VCC - WAX,	VIH - Z V		V _O = 0.4 V			- 20			20	μΑ
11	V _{CC} = MAX,	V ₁ = 7 V					0.1			0.1	mΑ
liH.	V _{CC} = MAX,	V _I = 2.7 V					20			20	μΑ
1	V _{CC} = MAX,	V ₁ = 0.4 V		Ğ			- 0.2			- 0.2	
115	VCC - MIAA,	V - 0.4 V		All other			- 0.4			- 0.4	, mA
Ios§	V _{CC} = MAX				- 30		- 130	- 30		- 130	mA
loo	V _{CC} = MAX,	See Note 2		Condition A		7	12		7	12	
¹cc	VCC - WAX,	See Note 2		Condition B		8.5	14		8.5	14	mA

[†] For conditions shown as MIN or MAX, use the appropriate value spcified under recommended operating conditions.

NOTE 2: I_{CC} is measured with the outputs open under the following conditions:

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH .	Data	Y			17	25	
tPHL.	Data	'			13	20	ns
^t PLH	Select		$C_L = 15 pF$, $R_L = 2 k\Omega$,		30	45	
tPHL.	Select	'	See Note 3		21	32	ns
^t PZH	Output				15	28	
^t PZL	Control	'			15	23	ns
^t PHZ	Output		$C_L = 5 pF$, $R_L = 2 k\Omega$,		27	41	
^t PLZ	Control	Y	See Note 3		18	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ} \text{C}$.

[§] Not more than one output should be shorted at a time, and duration for the short-circuit should exceed one second.

A. All inputs grounded.

B. Output control at 4.5 V, all inputs grounded.

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recommended operating conditions

			N54S2	53	8			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			-2			- 6.5	mA
IOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	- 55		125	0		70	°c

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDIT	rions†		MIN	түр‡	MAX	UNIT
VIK	VCC = MIN,	I ₁ = - 18 mA						- 1.2	V
Vон	VCC = MIN,	V _{1H} = 2 V,	V _{1L} = 0.8 V,	LOW - MAY	Series 54S	2,5	3.4		V
* OH	VCC - WITH,	VIH - 2 V,	V _{IL} = 0.8 V, I _{OH} = MAX	Series 74S	2.7	3.4		1 V	
VOL	VCC = MIN,	VIH = 2 V,	VIL = 0.8 V,	IOL = 20 mA				0.5	V
loz	Vcc = MAX,	VIH = 2 V			V _O = 2.4 V			50	
	VCC - WAX,	VIH - Z V			V _O = 0.5 V			- 50	μА
1 ₁	V _{CC} = MAX,	V1 = 5.5 V						1	mA
IН	V _{CC} = MAX,	V _I = 2.7 V						50	μΑ
111	V00 - 110 V	V: - 0.5 V			G = 0.8 V			- 2	
•11.	VCC = MAX,	$V_1 = 0.5 V$			G = 2 V			- 0.25	mA
los§	V _{CC} = MAX				1	- 40		- 100	mA
¹cc	V _{CC} = MAX,	See Note 2			Condition A		45	70	
	TOG = WAX,	See Note 2			Condition B		65	85	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTE 2: ICC is measured with the outputs open under the following conditions:

- A. All inputs grounded.
- B. Output control at 4.5 V, all inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ} \text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CON	IDITIONS	MIN TYP	MAX	UNIT
^t PLH	Data	~			6	9	
^t PHL	Data	1			6	9	ns
^t PLH	Select	· ·	R _L = 280 Ω,	C _L = 15 pF	11.5	18	
^t PHL] 00.001	'	See Note 3	o_ ,o p.	12	18	ns
^t PZH	Output	· ·	***************************************		11	16.5	
^t PZL	Control				12	18	ns
^t PHZ	Output	V	R _L = 280 Ω,	C _L = 5 pF	6.5	9.5	
^t PLZ	Control	1	See Note 3		10	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ} \text{C}$.

1-Jun-2012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
76017012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
7601701EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
7601701EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
7601701FA	NRND	CFP	W	16	1	TBD	Call TI	Call TI	
7601701FA	NRND	CFP	W	16	1	TBD	Call TI	Call TI	
JM38510/30908B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/30908B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/30908BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
JM38510/30908BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
JM38510/30908BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
JM38510/30908BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
M38510/30908B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/30908B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/30908BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
M38510/30908BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
M38510/30908BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
M38510/30908BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SN54LS253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54LS253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN74LS253D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LS253DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	
SN74LS253J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	
SN74LS253N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS253N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS253N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74LS253N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74LS253NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS253NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS253NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S253N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74S253N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SNJ54LS253FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS253FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS253W	NRND	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS253W	NRND	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54LS253, SN74LS253:

Catalog: SN74LS253





1-Jun-2012

• Military: SN54LS253

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications



TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

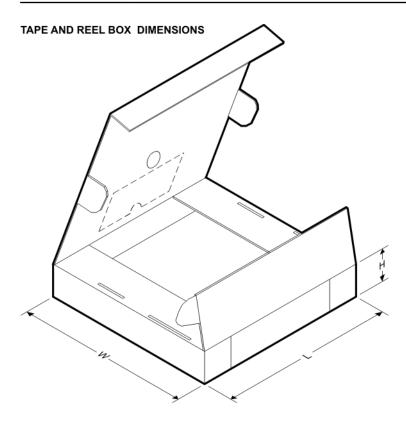
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS253DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS253NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS253DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS253NSR	SO	NS	16	2000	346.0	346.0	33.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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