- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

#### description

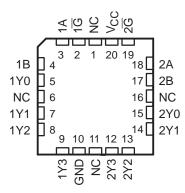
The 'ALS139 are dual 2-line to 4-line decoders/demultiplexers designed for use in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these devices can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. Therefore, the effective system decoder is negligible.

The 'ALS139 comprise two individual 2-line to 4-line decoders in a single package. The active-low enable  $(\overline{G})$  input can be used as a data line in demultiplexing applications. These

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SN54ALS139 J PACKAGE SN74ALS139 D OR N PACKAGE (TOP VIEW)						
1 G 1 A 1 B 1 Y0 1 Y1 1 Y2 1 Y3 GND	2 3 4 5 6	16 15 14 13 12 11 10 9	] V <sub>CC</sub> ] 2G ] 2A ] 2B ] 2Y0 ] 2Y1 ] 2Y2 ] 2Y3			

SN54ALS139 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

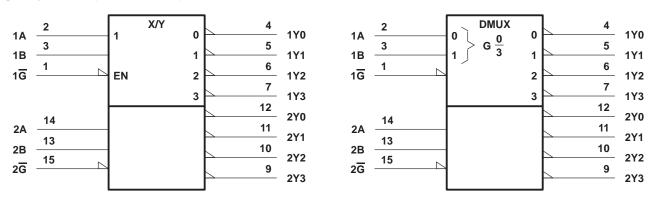
decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line ringing and simplify system design.

The SN54ALS139 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ALS139 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE									
IN	IPUTS			OUTPUTS					
ENABLE	SEL	ECT		001	-015				
G	В	Α	Y0	Y1	Y2	Y3			
Н	Х	Х	Н	Н	Н	Н			
L	L	L	L	Н	Н	н			
L	L	н	н	L	Н	н			
L	Н	L	н	Н	L	н			
L	Н	Н	н	Н	Н	L			

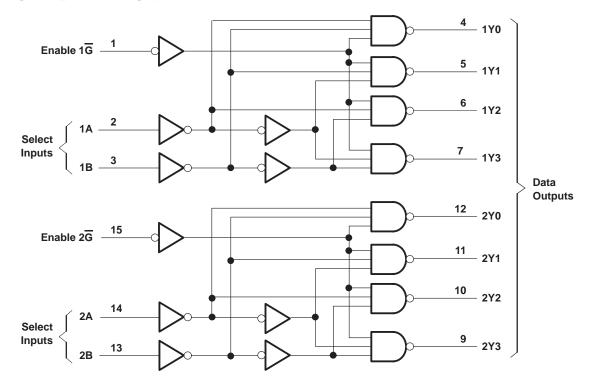
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#### logic symbols (alternatives)<sup>†</sup>



<sup>†</sup> These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

#### logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.



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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, V <sub>CC</sub> Input voltage, V <sub>I</sub>	
Operating free-air temperature range, T <sub>A</sub> : SN54ALS139	–55°C to 125°C
SN74ALS139	0°C to 70°C
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

		SN	SN54ALS139		SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-0.4			-0.4	mA
IOL	Low-level output current			4			8	mA
TA	Operating free-air temperature	-55		125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COM	SN54ALS139			SN	UNIT			
PARAMETER	TEST COM	NDITIONS	MIN	TYP‡	MAX	MIN	typ‡	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	II = -18 mA			-1.2			-1.2	V
VOH	$V_{CC}$ = 4.5 V to 5.5 V,	$I_{OH} = -0.4 \text{ mA}$	V <sub>CC</sub> -2	2		V <sub>CC</sub> -2	2		V
Vol	V <sub>CC</sub> = 4.5 V	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
VOL	VCC = 4.5 V	I <sub>OL</sub> = 8 mA					0.35	0.5	v
lj	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V			0.1			0.1	mA
Чн	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20			20	μΑ
Ι <sub>ΙL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-0.1			-0.1	mA
۱ <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-20		-112	-30		-112	mA
ICC	V <sub>CC</sub> = 5.5 V			8	13		8	13	mA

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

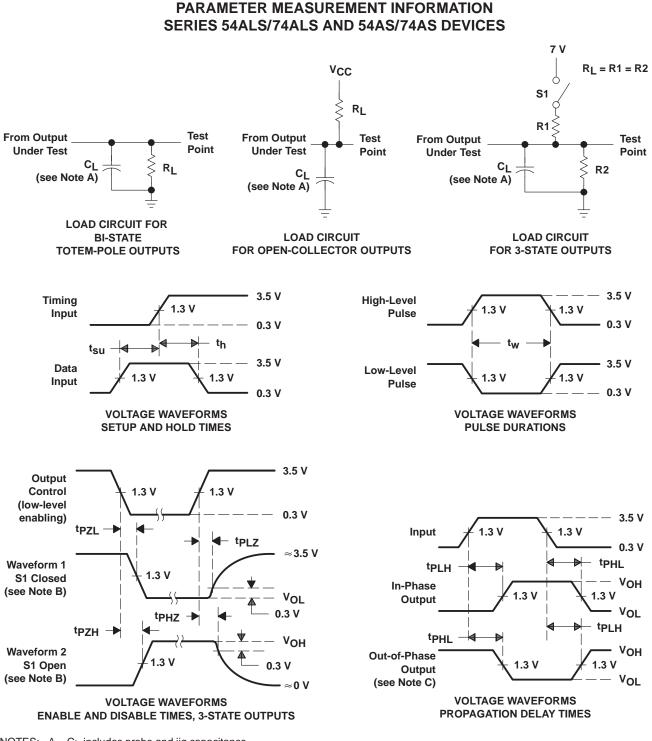
#### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	l RL	= 500 🖸	V to 5.5 <del>,</del> 2, o MAX¶		UNIT
			SN54A	LS139	SN74A		
			MIN	MAX	MIN	MAX	
<sup>t</sup> PLH	A or B	V	3	17	3	14	
<sup>t</sup> PHL	AUD	Ť	3	17	3	14	ns
<sup>t</sup> PLH	G	v	3	17	3	14	
<sup>t</sup> PHL	6	Т	3	18	3	15	ns

 $\P$  For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR  $\leq$  1 MHz, t<sub>r</sub> = t<sub>f</sub> = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

#### Figure 1. Load Circuits and Voltage Waveforms





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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-87683012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8768301EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
5962-8768301FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
SN54ALS139J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN74ALS139D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS139DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS139DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS139DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS139DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS139DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS139N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS139N3	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI	
SN74ALS139NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS139NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS139NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS139NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54ALS139FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS139J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS139W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect. NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.



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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available. **OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and pa

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN54ALS139, SN74ALS139 :

• Catalog: SN74ALS139

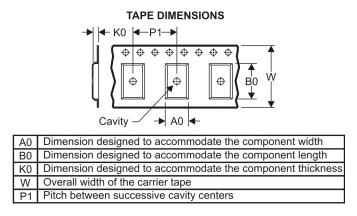
Military: SN54ALS139

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

### TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*A	Il dimensions are nominal												
	Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	SN74ALS139DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
	SN74ALS139NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



# PACKAGE MATERIALS INFORMATION

19-Mar-2008



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS139DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74ALS139NSR	SO	NS	16	2000	346.0	346.0	33.0

J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N\*\*) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



# N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/D 06/11

# D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### MECHANICAL DATA

#### PLASTIC SMALL-OUTLINE PACKAGE

#### 0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 $\bigcirc$ Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS \*\* 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G\*\*)

**14-PINS SHOWN** 

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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