

Data sheet acquired from Harris Semiconductor

# CD54HC221, CD74HC221, CD74HCT221

## High-Speed CMOS Logic Dual Monostable Multivibrator with Reset

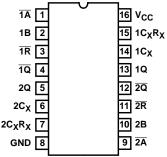
November 1997 - Revised October 2003

#### **Features**

- Overriding RESET Terminates Output Pulse
- Triggering from the Leading or Trailing Edge
- Q and Q Buffered Outputs
- Separate Resets
- · Wide Range of Output-Pulse Widths
- Schmitt Trigger on B Inputs
- Fanout (Over Temperature Range)
  - Standard Outputs......10 LSTTL Loads
  - Bus Driver Outputs ................ 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N $_{IL}$  = 30%, N $_{IH}$  = 30% of V $_{CC}$  at V $_{CC}$  = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,
     V<sub>IL</sub>= 0.8V (Max), V<sub>IH</sub> = 2V (Min)
  - CMOS Input Compatibility,  $I_I \leq 1 \mu \text{A}$  at  $V_{\mbox{\scriptsize OL}},\, V_{\mbox{\scriptsize OH}}$

### **Pinout**

CD54HC221 (CERDIP) CD74HC221 (PDIP, SOIC, SOP, TSSOP) CD74HCT221 (PDIP, SOIC) TOP VIEW



### Description

The 'HC221 and CD74HCT221 are dual monostable multivibrators with reset. An external resistor  $(R_X)$  and an external capacitor  $(C_X)$  control the timing and the accuracy for the circuit. Adjustment of  $R_X$  and  $C_X$  provides a wide range of output pulse widths from the Q and  $\overline{\rm Q}$  terminals. Pulse triggering on the B input occurs at a particular voltage level and is not related to the rise and fall time of the trigger pulse.

Once triggered, the outputs are independent of further trigger inputs on  $\overline{A}$  and B. The output pulse can be terminated by a LOW level on the Reset  $(\overline{R})$  pin. Trailing Edge triggering  $(\overline{A})$  and leading-edge-triggering (B) inputs are provided for triggering from either edge of the input pulse. On power up, the IC is reset. If either Mono is not used each input (on the unused device) must be terminated either high or low.

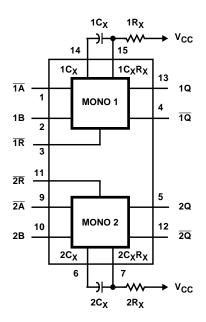
The minimum value of external resistance, R<sub>X</sub>, is typically 500 $\Omega$  The minimum value of external capacitance, C<sub>X</sub>, is 0pF. The calculation for the pulse width is t<sub>W</sub> = 0.7 R<sub>X</sub>C<sub>X</sub> at V<sub>CC</sub> = 4.5V.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC221F3A	-55 to 125	16 Ld CERDIP
CD74HC221E	-55 to 125	16 Ld PDIP
CD74HC221M	-55 to 125	16 Ld SOIC
CD74HC221MT	-55 to 125	16 Ld SOIC
CD74HC221M96	-55 to 125	16 Ld SOIC
CD74HC221NSR	-55 to 125	16 Ld SOP
CD74HC221PW	-55 to 125	16 Ld TSSOP
CD74HC221PWR	-55 to 125	16 Ld TSSOP
CD74HC221PWT	-55 to 125	16 Ld TSSOP
CD74HCT221E	-55 to 125	16 Ld PDIP
CD74HCT221M	-55 to 125	16 Ld SOIC
CD74HCT221MT	-55 to 125	16 Ld SOIC
CD74HCT221M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

## Functional Diagram

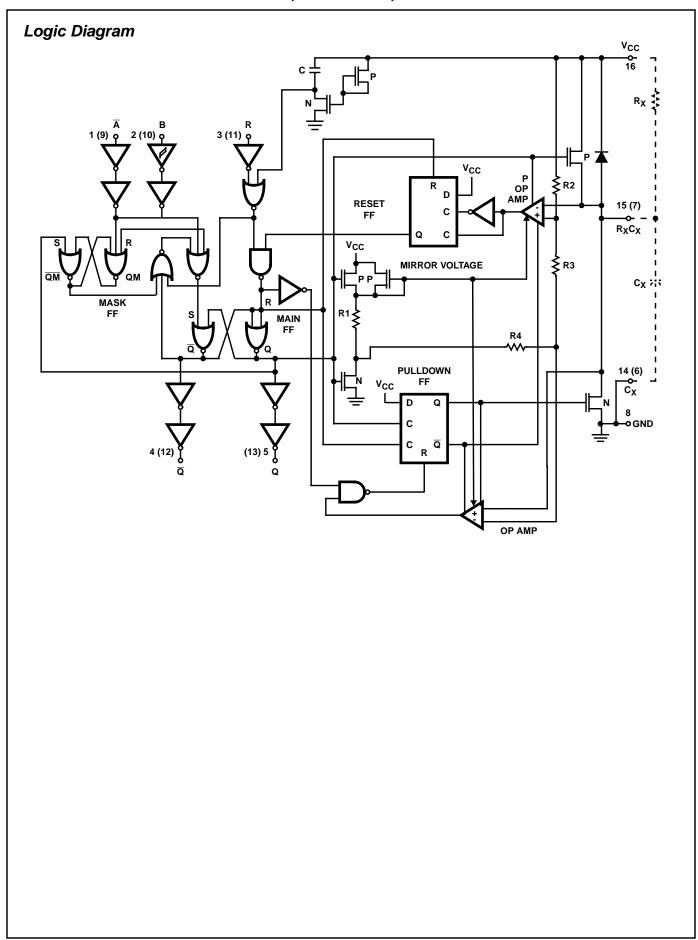


**TRUTH TABLE** 

	INPUTS		OUTI	PUTS
Ā	В	R	Q	Q
Н	Х	Н	L	Н
Х	L	Н	L	Н
L	1	Н	4	5
$\downarrow$	Н	Η	Ę	5
Х	Х	L	L	Н
L	Н	1	(Note 3)	(Note 3)

H = High Voltage Level, L = Low Voltage Level, X = Irrelevant,  $\uparrow$  = Transition from Low to High Level,  $\downarrow$  = Transition from High to Low Level,  $\bot$  = One High Level Pulse,  $\bot$  = One Low Level Pulse NOTE:

 For this combination the reset input must be low and the following sequence must be used: pin 1 (or 9) must be set high or pin 2 (or 10) set low; then pin 1 (or 9) must be low and pin 2 (or 10) set high. Now the reset input goes from lowto-high and the device will be triggered.



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#### **Thermal Information**

### **Operating Conditions**

Temperature Range, T <sub>A</sub> 55°C to 125°C
Supply Voltage Range, V <sub>CC</sub>
HC Types2V to 6V
HCT Types
DC Input or Output Voltage, V <sub>I</sub> , V <sub>O</sub>
Input Rise and Fall Time, $t_r$ , $t_f$ on Inputs $\overline{A}$ and $\overline{R}$
2V
4.5V 500ns (Max)
6V
Input Rise and Fall Time, t <sub>r</sub> , t <sub>f</sub> on Input B
2V Unlimited ns (Max)
4.5V Unlimited ns (Max)
6V Unlimited ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

2. The package thermal impedance is calculated in accordance with JESD 51-7.

### **DC Electrical Specifications**

		TEST CONDITIONS		v <sub>cc</sub>		25°C		-40°C 1	O 85°C	-55°C T	O 125°C	4
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES												
High Level Input	V <sub>IH</sub>	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input	V <sub>IL</sub>	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output	VoH	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
Voltage CMOS Loads			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
OWOO LOUGS			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output	1		-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
TTE Education			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
C.I.OO EOGGO			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output	7		-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V

## DC Electrical Specifications (Continued)

		TES CONDI		v <sub>cc</sub>		25°C		-40°C 1	O 85°C	-55°C T	O 125°C	
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(8)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Input Leakage Current	l <sub>l</sub>	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μΑ
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μΑ
HCT TYPES		•			•		•	•		•		
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>ОН</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V <sub>CC</sub> and GND	0	5.5	-		±0.1	-	±1	-	±1	μΑ
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μΑ
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 3)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μΑ

#### NOTE:

### **HCT Input Loading Table**

INPUT	UNIT LOADS
All Inputs	0.3

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Table, e.g., 360µA max at  $25^{o}C.$ 

## **Prerequisite For Switching Function**

				25°C		-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES		-		-		-		-	-	
Input Pulse Width	t <sub>WL</sub>	2	70	-	-	90	-	105	-	ns
Ā		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns
Input Pulse Width	t <sub>WH</sub>	2	70	-	-	90	-	105	-	ns
В		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns

<sup>3.</sup> For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

## Prerequisite For Switching Function (Continued)

				25°C		-40°C T	O 85°C	-55°C T	O 125°C	
PARAMETER	SYMBOL	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Input Pulse Width	t <sub>WL</sub>	2	70	-	-	90	-	105	-	ns
Reset		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns
Recovery Time	t <sub>SU</sub>	2	0	-	-	0	-	0	-	ns
$\overline{R}$ to $\overline{A}$ or $B$		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
Output Pulse Width Q or $\overline{Q}$ $C_X = 0.1 \mu F R_X = 10 k\Omega$	t <sub>W</sub>	5	630	-	770	602	798	595	805	μѕ
Output Pulse Width Q or Q $C_X = 28pF$ , $R_X = 2k\Omega$	t <sub>W</sub>	4.5	-	140	-	-	-	-	-	ns
$C_X = 1000 pF, R_X = 2k\Omega$	t <sub>W</sub>	4.5	-	1.5	-	-	-	-	-	μs
$C_X = 1000 pF, R_X = 10 k\Omega$	t <sub>W</sub>	4.5	-	7	-	-	-	-	-	μs
HCT TYPES										
Input Pulse Width $\overline{A}$	t <sub>W</sub> ∟	4.5	14	-	-	18	-	21	-	ns
Input Pulse Width B	t <sub>WH</sub>	4.5	14	-	-	18	-	21	-	ns
Input Pulse Width Reset	t <sub>WL</sub>	4.5	18	-	-	23	-	27	-	ns
Recovery Time R to A or B	t <sub>SU</sub>	4.5	0	-	-	0	-	0	-	ns
Output Pulse Width Q or $\overline{Q}$ $C_X = 0.1 \mu F R_X = 10 k\Omega$	t <sub>W</sub>	5	630	-	770	602	798	595	805	μs
Output Pulse Width Q or Q $C_X = 28pF$ , $R_X = 2k\Omega$	t <sub>W</sub>	4.5	-	140	-	-	-	-	-	ns
$C_X = 1000 pF$ , $R_X = 2k\Omega$	t <sub>W</sub>	4.5	-	1.5	-	-	-	-	-	μs
$C_X = 1000 pF, R_X = 10 k\Omega$	t <sub>W</sub>	4.5	-	7	-	-	-	-	-	μs

## Switching Specifications Input $t_{r}$ , $t_{f} = 6 \text{ns}$

		TEST		25°C			-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES			-			_		_		-	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	2	-	-	210	-	265	-	315	ns
Trigger $\overline{A}$ , B, $\overline{R}$ to Q		C <sub>L</sub> = 50pF	4.5	-	-	42	-	53	-	63	ns
		C <sub>L</sub> = 50pF	6	-	-	36	-	45	-	54	ns
		C <sub>L</sub> = 15pF	5	-	18	-	-	-	-	-	ns
Propagation Delay,	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	170	-	215	-	255	ns
Trigger $\overline{A}$ , $B$ , $\overline{R}$ to $\overline{Q}$		C <sub>L</sub> = 50pF	4.5	-	-	34	-	43	-	51	ns
		C <sub>L</sub> = 50pF	6	-	-	29	-	37	-	43	ns
		C <sub>L</sub> = 15pF	5	-	14	-	-	-	-	-	ns

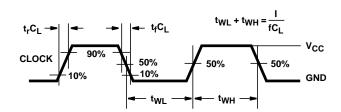
# Switching Specifications Input $t_r$ , $t_f = 6 \text{ns}$ (Continued)

		TEST		25°C				С ТО °С	-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	2	-	-	160	-	200	-	240	ns
R to Q			4.5	-	-	32	=	40	-	48	ns
			6	-	-	27	=	34	-	41	ns
Propagation Delay,	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	180	-	225	-	270	ns
R to Q			4.5	-	-	36	-	45	-	54	ns
			6	-	-	31	-	38	-	46	ns
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C <sub>IN</sub>	-	-	-	-	10	-	10	-	10	pF
Pulse Width Match Between Circuits in the Same Package $C_X = 1000pF$ , $R_X = 10k\Omega$		-	4.5 to 5.5	-	±2	-	-	-	-	-	%
Power Dissipation Capacitance (Notes 4, 5)	CPD	-	5	-	166	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay, Trigger A, B, R to Q	t <sub>PLH</sub>	$C_L = 50pF$	4.5	-	_	42	-	-	-	63	ns
Trigger A, B, K to Q		C <sub>L</sub> = 15pF	5	-	18	-	-	-	-	-	ns
Propagation Delay,	t <sub>PHL</sub>	$C_L = 50pF$	4.5	-	-	34	-	43	-	51	ns
Trigger $\overline{A}$ , $B$ , $\overline{R}$ to $\overline{Q}$		C <sub>L</sub> = 15pF	5	ı	14	-	ı	i	·	-	ns
Propagation Delay, $\overline{R}$ to $Q$	<sup>t</sup> PLH	C <sub>L</sub> = 50pF	4.5	-	-	38	-	-	-	57	ns
Propagation Delay, $\overline{R}$ to $\overline{Q}$	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	37	-	-	-	56	ns
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C <sub>IN</sub>	-	-	-	-	10	-	10	-	10	pF
Pulse Width Match Between Circuits in the Same Package $C_X = 1000pF$ , $R_X = 10k\Omega$		-	4.5 to 5.5	-	±2	-	-	-	-	-	%
Power Dissipation Capacitance (Notes 4, 5)	CPD	-	5	-	166	-	-	-	-	-	pF

<sup>4.</sup>  $C_{\mbox{\scriptsize PD}}$  is used to determine the dynamic power consumption, per multivibrator.

<sup>5.</sup>  $P_D = (C_{PD} + C_L) V_{CC}^2 f_i + \Sigma$  where  $f_i$  = input frequency,  $f_0$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

### Test Circuits and Waveforms



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

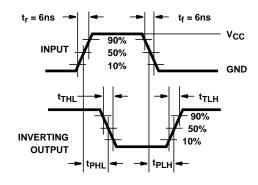
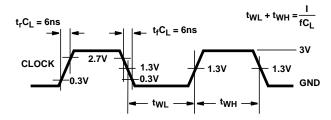


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



NOTE: Outputs should be switching from 10% V $_{CC}$  to 90% V $_{CC}$  in accordance with device truth table. For f $_{MAX}$ , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

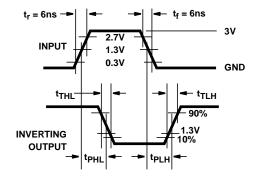


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

## **Typical Performance Curves**

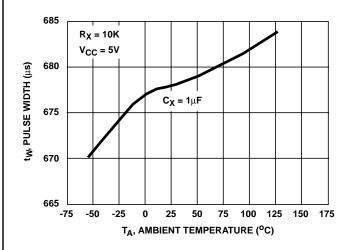


FIGURE 5. HC/HCT221 OUTPUT PULSE WIDTH vs TEMPERATURE

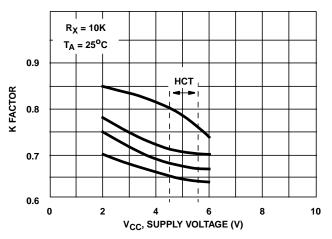


FIGURE 6. HC/HCT221 K FACTOR vs SUPPLY VOLTAGE

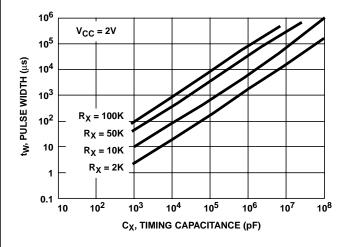


FIGURE 7. HC221 OUTPUT PULSE WIDTH vs  $C_\chi$ 

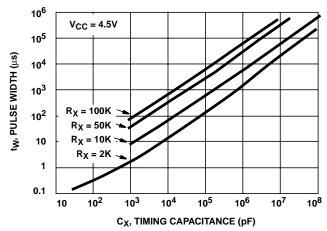
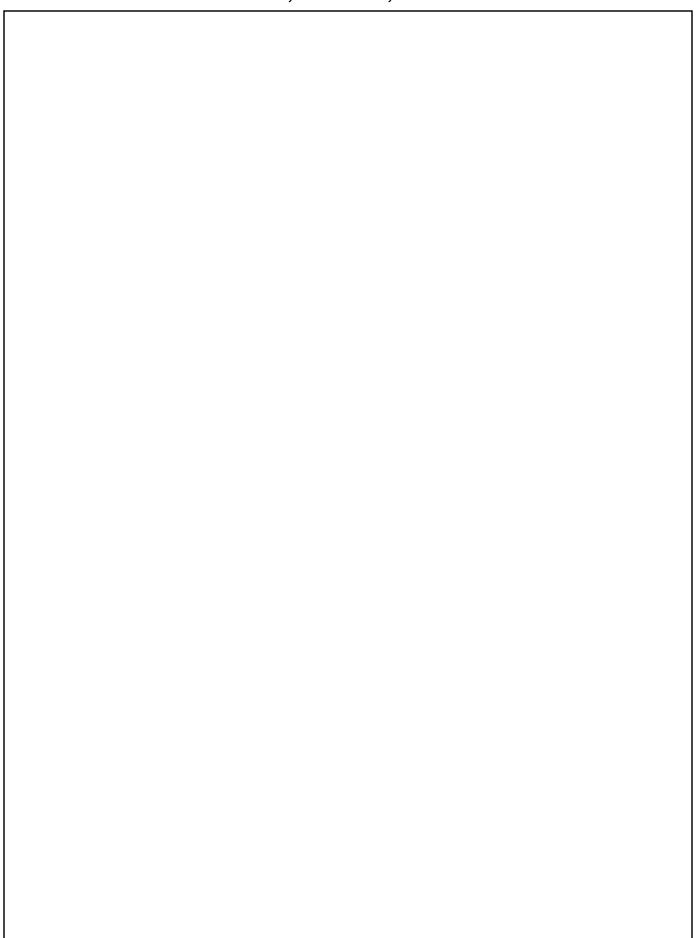


FIGURE 8. HC/HCT221 OUTPUT PULSE WIDTH vs  $C_\chi$ 



5-Sep-2011

### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-8780501EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
CD54HC221F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD54HC221F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD74HC221E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC221EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC221M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



5-Sep-2011

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CD74HC221PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC221PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT221E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT221EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT221M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT221M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT221M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT221M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT221ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT221MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT221MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT221MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT221MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:



### PACKAGE OPTION ADDENDUM

5-Sep-2011

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF CD54HC221, CD74HC221:

Catalog: CD74HC221

www.ti.com

Military: CD54HC221

NOTE: Qualified Version Definitions:

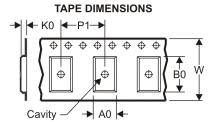
- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 6-Aug-2010

### TAPE AND REEL INFORMATION





Α	0	Dimension designed to accommodate the component width
В	0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
٧	٧	Overall width of the carrier tape
ГР	1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC221M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC221NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC221PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC221PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT221M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

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\*All dimensions are nominal

7 til dilliciololio die Horilita							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC221M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC221NSR	SO	NS	16	2000	346.0	346.0	33.0
CD74HC221PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
CD74HC221PWT	TSSOP	PW	16	250	346.0	346.0	29.0
CD74HCT221M96	SOIC	D	16	2500	333.2	345.9	28.6

### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



## D (R-PDS0-G16)

### PLASTIC SMALL OUTLINE

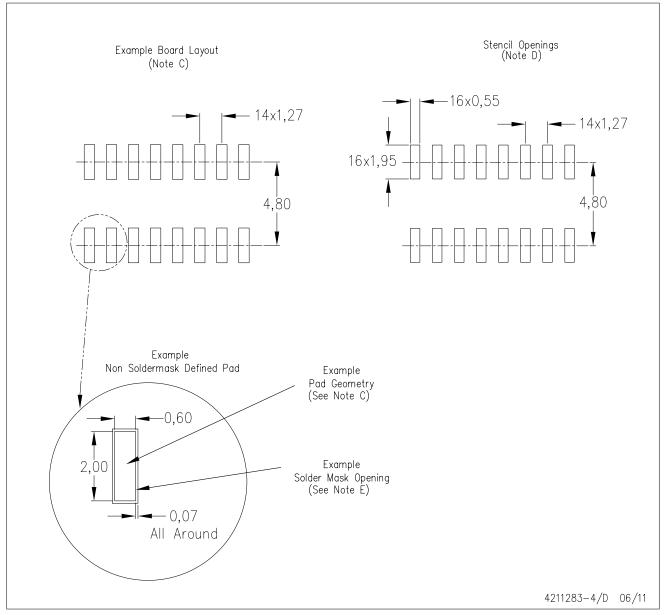


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# D (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

### PLASTIC SMALL OUTLINE

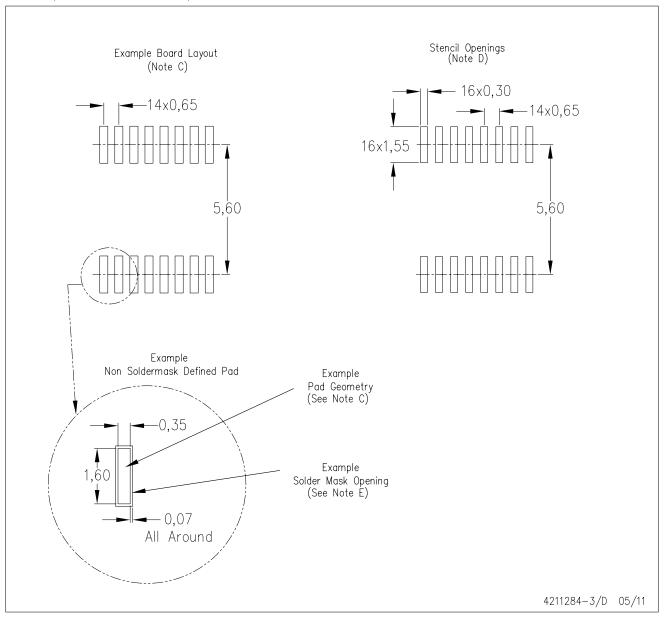


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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