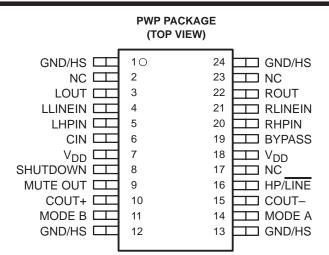
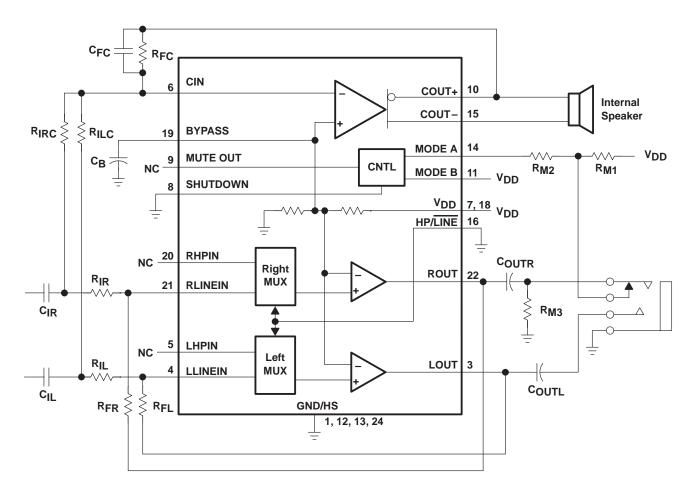
- **Desktop Computer Amplifier Solution** 
  - 1.75-W Bridge Tied Load (BTL) Center Channel
  - 500-mW L/R Single-Ended Channels
- **Low Distortion Output** 
  - < 0.05% THD+N at Full Power
- Full 3.3-V and 5-V Specifications
- **Surface-Mount Power Package** 24-Pin TSSOP
- L/R Input MUX Feature
- Shutdown Control . . .  $I_{DD} = 5 \mu A$







Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated



#### description

The TPA0103 is a 3-channel audio power amplifier in a 24-pin TSSOP thermal package primarily targeted at desktop PC or notebook applications. The left/right (L/R) channel outputs are single ended (SE) and capable of delivering 500 mW of continuous RMS power per channel into 4- $\Omega$  loads. The center channel output is a bridged tied load (BTL) configuration for delivering maximum output power from PC power supplies. Combining the SE line drivers and high power center channel amplifiers in a single TSSOP package simplifies design and frees up board space for other features. Full power distortion levels of less than 0.25% THD+N into 4- $\Omega$  loads from a 5-V supply voltage are typical. Low-voltage application are also well served by the TPA0103 providing 800 mW to the center channel into 4- $\Omega$  loads with a 3.3-V supply voltage.

Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10. A two channel input MUX circuit is integrated on the L/R channel inputs to allow two sets of stereo inputs to the amplifier. In the typical application, the center channel amplifier is driven from a mix of the L/R inputs to produce a monaural representation of the stereo signal. The center channel amplifier can be shut down independently of the L/R output for speaker muting in headphone applications. The TPA0103 also features a full shutdown function for power sensitive applications holding the bias current to 5  $\mu$ A.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of less than 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0103 to operate at full power at ambient temperature of up to 85°C.

#### **AVAILABLE OPTIONS**

	PACKAGE	
TA	TSSOP†	
	(PWP)	
-40°C to 85°C	TPA0103PWP	

<sup>†</sup>The PWP package is available in left-ended tape and reel only (e.g., TPA0103PWPLE).



### **Terminal Functions**

TERMINAL			DECODIDATION					
NAME	NO.	1/0	DESCRIPTION					
BYPASS	19		Bypass. BYPASS is a tap to the voltage divider for the internal mid-supply bias.					
CIN	6	Ι	Center channel	input				
COUT+	10	0				high-impedance s ODE B terminal (		device is in a mute state
COUT-	15	0				high-impedance s ODE B terminal (		device is in a mute state
GND/HS	1, 12, 13, 24		Ground. GND/H	S is the ground c	onnection for circ	cuitry, directly con	nected to therm	al pad.
MODE A,	14, 11	Ι	Mode select. Mo	DDE A and MODI	E B determine the	e output modes o	f the TPA0103.	
MODE B			TERMINAL	3 CHANNEL	MUTE	CENTER ONLY	L/R ONLY	
			MODE A	L	Н	L	Н	
			MODE B	L	L	Н	Н	
HP/LINE	16	I				PIN (5, 20), hold local connected to (L/R		LINEIN (4, 21). HP/LINE
LHPIN	5	Ι	Left channel hea	adphone input, se	elected when the	HP/LINE terminal	(16) is held hig	h
LLINEIN	4	I	Left channel line	input, selected v	vhen the HP/LINE	E terminal (16) is	held low	
LOUT	3	0	Left channel out don't care.	put. LOUT is acti	ve when the MOI	DE A terminal (14	) is low and the	MODE B terminal (11) is
MUTE OUT	9	0		A terminal (14) is e. Otherwise MU		DE B terminal (11)	is low, MUTE O	UT is high and the device
NC	2, 17, 23		No internal conr	ection				
RHPIN	20	Ι	Right channel h	eadphone input, s	selected when the	e HP/LINE termin	al (16) is held hi	gh
RLINEIN	21	I	Right channel lir	Right channel line input, selected when the HP/LINE terminal (16) is held low				
ROUT	22	0	Right channel output. ROUT is active when the MODE A terminal (14) is low and the MODE B terminal (11) is don't care.					
SHUTDOWN	8	I	Places entire IC	in shutdown mod	de when held higl	h, I <sub>DD</sub> = 5 μA		
$V_{DD}$	7, 18	I	Supply voltage i	nput. The V <sub>DD</sub> te	erminals must be	connected togeth	er.	

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>DD</sub>	
Continuous output current (COUT+, COUT-, LOUT, ROUT)	2 A
Continuous total power dissipation	internally limited
Operating virtual junction temperature range, T <sub>J</sub>	40°C to 150°C
Operating virtual case temperature range, T <sub>C</sub>	40°C to 125°C
Storage temperature range, T <sub>stq</sub>	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### **DISSIPATION RATING TABLE**

PACKAGE	$T_{\hbox{\scriptsize A}} \leq 25^{\circ}\hbox{\scriptsize C}$	DERATING FACTOR	T <sub>A</sub> = 70°C	T <sub>A</sub> = 85°C
PWP <sup>‡</sup>	2.7 W	21.8 mW/°C	1.7 W	1.4 W

<sup>‡</sup> Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

### recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage, V <sub>DD</sub>	3	5	5.5	V
Operating junction temperature, T <sub>J</sub>		125		°C

## dc electrical characteristics, $T_A = 25$ °C

PARAMETER		TEST CONDITIONS			NOM	TYP	MAX	UNIT
IDD		V== = = 5 V	3 Channel			19	25	mA
	Supply current	$V_{DD} = 5 V$	L and R or Center only			9	15	mA
	Supply current	V <sub>DD</sub> = 3.3 V	3 Channel			13	20	mA
			L and R or C	enter only		3	10	mA
V00	Output offset voltage (measured differentially)	$V_{DD} = 5 V$ ,	Gain = 2,	See Note 1		5	35	mV
I <sub>DD(MUTE)</sub>	Supply current in mute mode	V <sub>DD</sub> = 5 V				800		μΑ
I <sub>DD(SD)</sub>	I <sub>DD</sub> in shutdown	V <sub>DD</sub> = 5 V				5	15	μΑ

NOTE 1: At 3 V <  $V_{DD}$  < 5 V the dc output voltage is approximately  $V_{DD}/2$ .



# ac operating characteristics, $\rm V_{DD}$ = 5 V, $\rm T_A$ = 25°C, $\rm R_L$ = 4 $\Omega$

	PARAMETER		CONDITIONS	MIN TYP MAX	UNIT	
		THD = 0.2%,	BTL, Center channel	1.75	W	
 	Output news (such channel) (see Note 2)	THD = 1%,	BTL, Center channel	2.1	VV	
Po	Output power (each channel) (see Note 2)	THD = 0.2%,	SE, L/R channels	535	mW	
		THD = 1%,	SE, L/R channels	575	IIIVV	
THD+N	Total harmonic distortion plus noise	P <sub>O</sub> = 1.5 W,	f = 20 to 20 kHz	0.25%		
ВОМ	Maximum output power bandwidth	G = 10,	THD < 5 %	>20	kHz	
	Phase margin	Open loop		85	0	
	Supply ripple rejection ratio	f = 1 kHz	Center channel	80		
		=   K	L/R channels	58	dB	
		( 00 00111	Center channel	60	αB	
		f = 20 - 20  kHz	L/R channels	30		
	Mute attenuation			85	dB	
	Channel-to-channel output separation	f = 1 kHz		95	dB	
	Line/HP input separation			100	dB	
Z <sub>I</sub>	Input impedance			2	MΩ	
	Signal to poince rotio	\/ - 4 \//rma)	BTL, Center channel	94	dB	
	Signal-to-noise ratio	$V_O = 1 V(rms)$	SE, L/R channels	100	] ub	
.,	Outrat as is a salt and	BTL,	Center channel	20		
V <sub>n</sub>	Output noise voltage	SE,	L/R channels	9	μV(rms)	

NOTE 2: Output power is measured at the output terminals of the IC at 1 kHz.

# ac operating characteristics, V<sub>DD</sub> = 3.3 V, T<sub>A</sub> = 25°C, R<sub>L</sub> = 4 $\Omega$

	PARAMETER		TEST CONDITIONS		UNIT	
		THD = 0.2%	BTL, Center channel	800		
D <sub>a</sub>	Output pourse (oneh abancal) (one Nata O)	THD = 1%	BTL, Center channel	850	\4/	
PO	Output power (each channel) (see Note 2)	THD = 0.2%,	SE, L/R channels	215	mW	
		THD = 1%,	SE, L/R channels	235		
THD+N	Total harmonic distortion plus noise	$P_0 = 750 \text{ mW},$	f = 20 to 20 kHz	0.8%		
ВОМ	Maximum output power bandwidth	G = 10,	THD < 5 %	>20	kHz	
	Phase margin	Open loop		85	0	
		f = 1 kHz	Center channel	70		
	Supply ripple rejection ratio	T = T KHZ	L/R channels	62	dB	
	Supply ripple rejection ratio	f = 20 – 20 kHz	Center channel	55	uБ	
		1 = 20 - 20 KHZ	L/R channels	30	1	
	Mute attenuation			85	dB	
	Channel-to-channel output separation	f = 1 kHz		95	dB	
	Line/HP input separation			100	dB	
Z <sub>l</sub>	Input impedance			2	MΩ	
	Circulto naino retia	\/- 4\//maa	BTL, Center channel	93	I.D.	
	Signal-to-noise ratio	$V_O = 1 V(rms)$	SE, L/R channels	100	dB	
V	Outrot poissonalters	BTL,	Center channel	21	.,,	
V <sub>n</sub>	Output noise voltage	SE,	L/R channels	10	μV(rms)	

NOTE 2: Output power is measured at the output terminals of the IC at 1 kHz.



#### PARAMETER MEASUREMENT INFORMATION

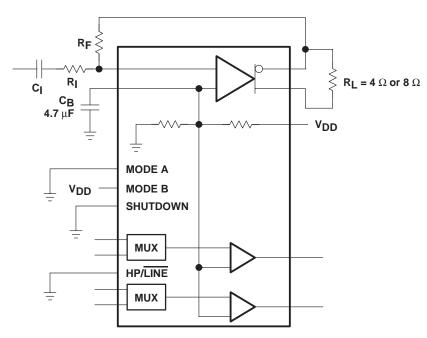


Figure 1. BTL Test Circuit

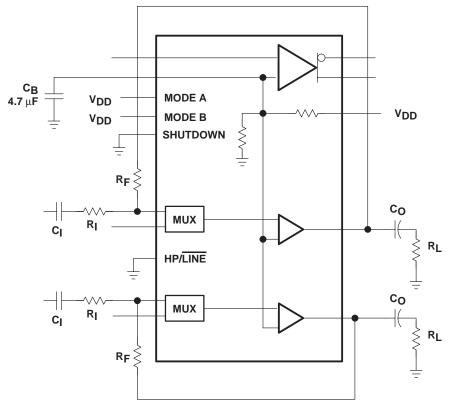


Figure 2. SE Test Circuit

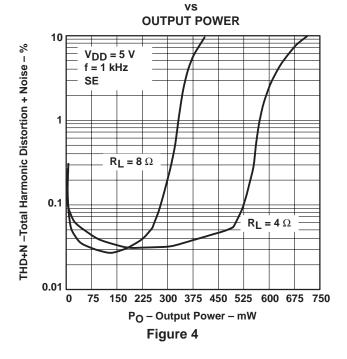


### **Table of Graphs**

			FIGURE
	Total harmonic distortion plus noise	vs Output power	3, 4, 7, 10–12, 15, 18, 21, 24, 27, 30, 33, 36
THD + N		vs Frequency	5, 6, 8, 9, 13, 14, 16, 17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34, 35
V <sub>n</sub>	Output noise voltage	vs Frequency	37,38
	Supply ripple rejection ratio	vs Frequency	39, 40
	Crosstalk	vs Frequency	41, 42
	Open loop response	vs Frequency	43, 44
	Closed loop response	vs Frequency	45 – 48
I <sub>DD</sub>	Supply current	vs Supply voltage	49
PO	Output power	vs Supply voltage vs Load resistance	50, 51 52, 53
PD	Power dissipation	vs Output power	54 – 57

# TOTAL HARMONIC DISTORTION PLUS NOISE

# **OUTPUT POWER** 10 THD+N -Total Harmonic Distortion + Noise - % $V_{DD} = 5 V$ f = 1 kHzBTL 1 $R_L = 4 \Omega$ $R_L = 8 \Omega$ 0.1 0.01 0.25 0.5 0.75 1.25 1.5 1.75 1 2.25 2.5 Po - Output Power - W Figure 3



THD+N -Total Harmonic Distortion + Noise - %

0.01 20

#### **TYPICAL CHARACTERISTICS**

# 



f - Frequency - Hz

100

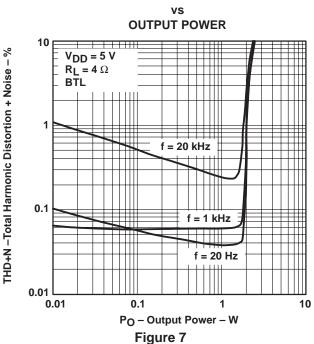
# **FREQUENCY** THD+N -Total Harmonic Distortion + Noise - % $V_{DD} = 5 V$ $R_L = 4 \Omega$ $A_V = -2 \text{ V/V}$ BTL $P_0 = 1.5 \text{ W}$ $P_0 = 0.75 W$ 0.1 $P_0 = 0.25 \text{ W}$ 20 100 1 k 10 k 20 k f - Frequency - Hz

TOTAL HARMONIC DISTORTION PLUS NOISE

TOTAL HARMONIC DISTORTION PLUS NOISE

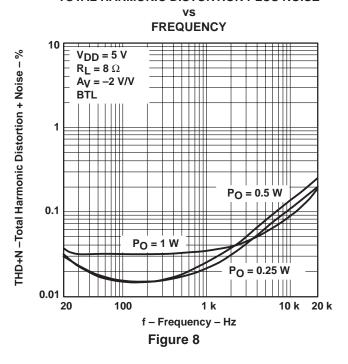
1 k

10 k 20 k



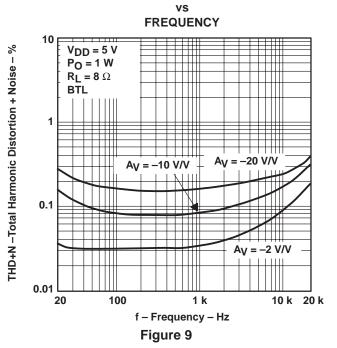
#### TOTAL HARMONIC DISTORTION PLUS NOISE

Figure 6

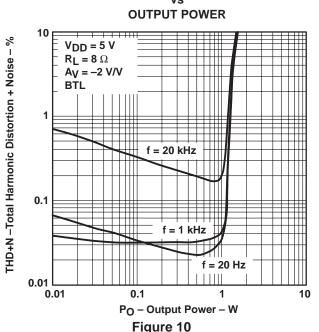




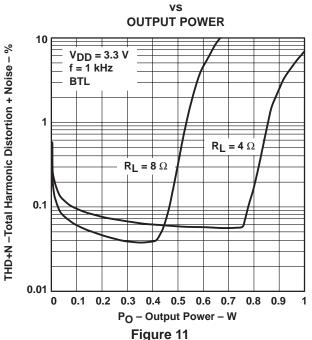
### TOTAL HARMONIC DISTORTION PLUS NOISE

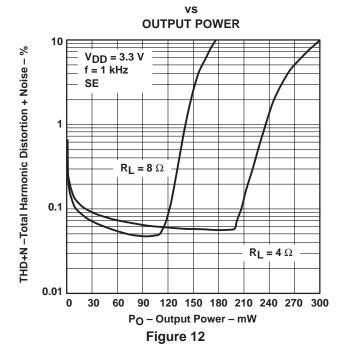


# TOTAL HARMONIC DISTORTION PLUS NOISE



## TOTAL HARMONIC DISTORTION PLUS NOISE



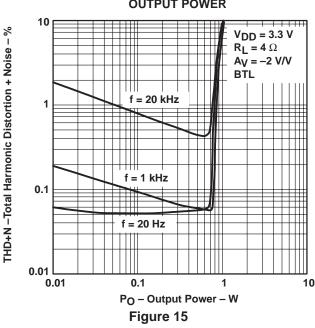


# TOTAL HARMONIC DISTORTION PLUS NOISE **FREQUENCY** THD+N -Total Harmonic Distortion + Noise - % $V_{DD} = 3.3 V$ $P_0 = 0.75 \text{ W}$ $R_L = 4 \Omega$ BTL $A_V = -20 \text{ V/V}$ 0.1 $A_V = -10 \text{ V/V}$ $A_V = -2 V/V$ 0.01 20 100 1 k 10 k 20 k f - Frequency - Hz

TOTAL HARMONIC DISTORTION PLUS NOISE **FREQUENCY** THD+N -Total Harmonic Distortion + Noise - %  $V_{DD} = 3.3 V$  $R_L = 4 \Omega$  $A_V^- = -2 \text{ V/V}$ BTL  $P_0 = 0.75 \text{ W}$ 0.1  $P_0 = 0.1 W$  $P_0 = 0.35 W$ 0.01 20 100 1 k 10 k 20 k f - Frequency - Hz

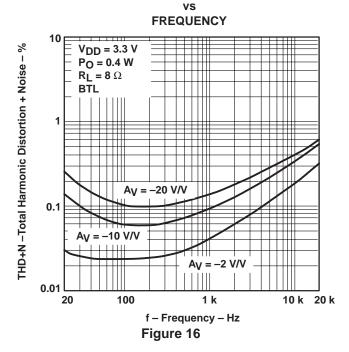
# TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

Figure 13

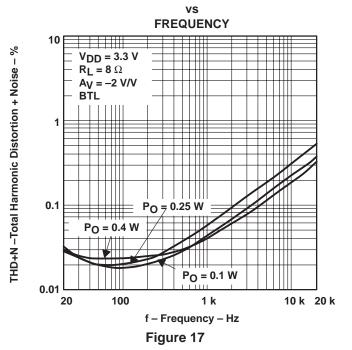


# TOTAL HARMONIC DISTORTION PLUS NOISE

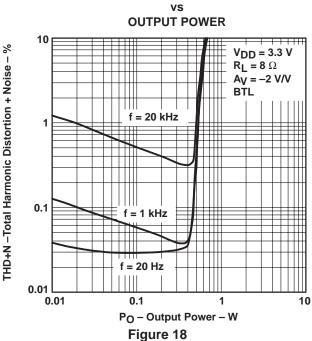
Figure 14



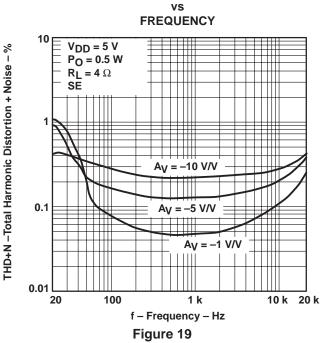
#### TOTAL HARMONIC DISTORTION PLUS NOISE

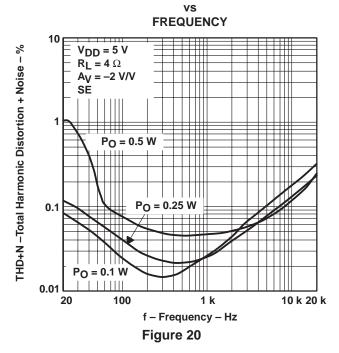


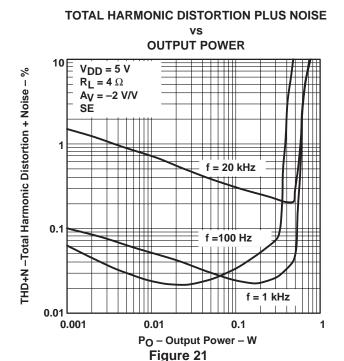
#### TOTAL HARMONIC DISTORTION PLUS NOISE

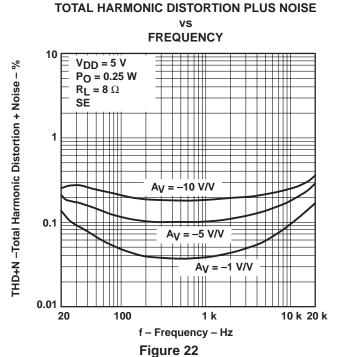


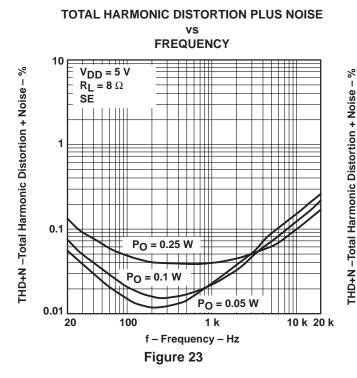
#### TOTAL HARMONIC DISTORTION PLUS NOISE

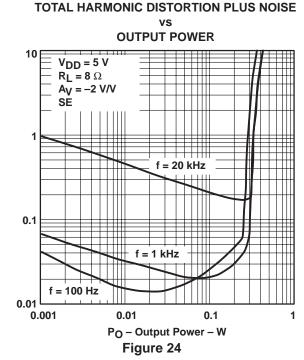












# 

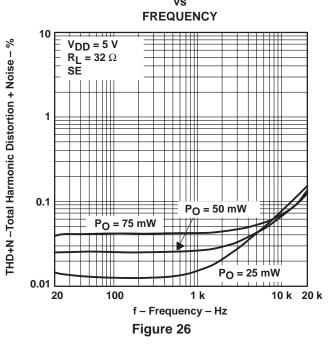
THD+N -Total Harmonic Distortion + Noise - %

0.01

20

100

TOTAL HARMONIC DISTORTION PLUS NOISE



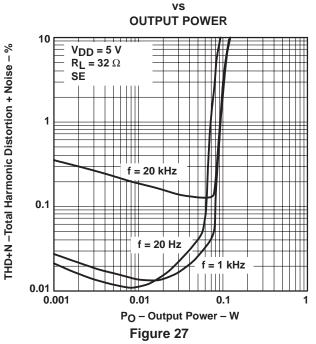
TOTAL HARMONIC DISTORTION PLUS NOISE

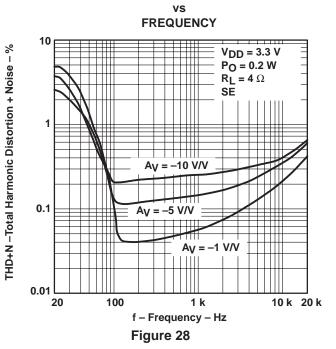
f - Frequency - Hz

Figure 25

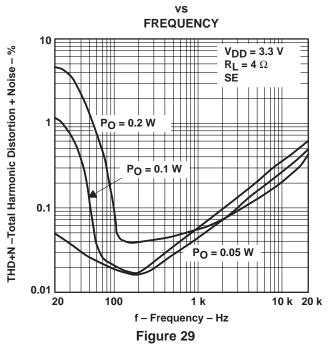
1 k

10 k 20 k

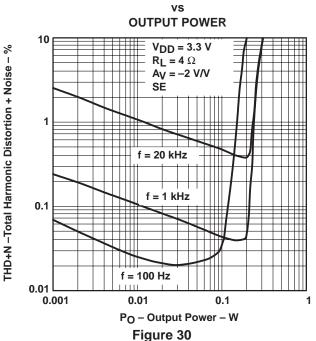




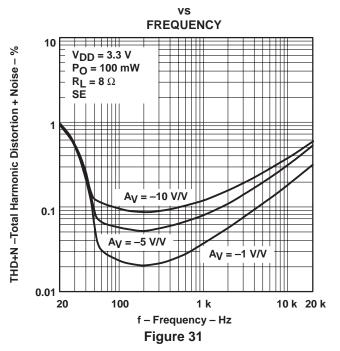
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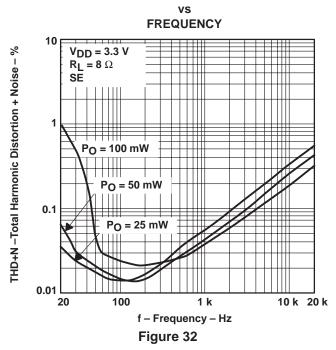


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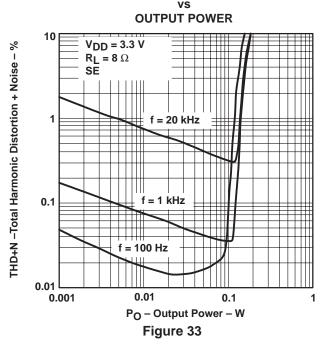


#### TOTAL HARMONIC DISTORTION PLUS NOISE

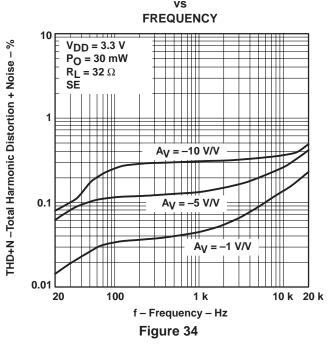




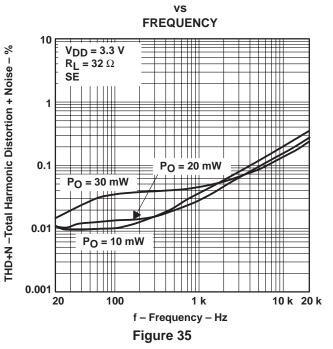
# TOTAL HARMONIC DISTORTION PLUS NOISE

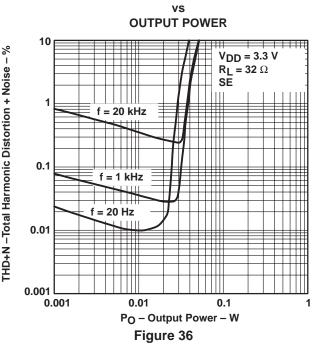


# TOTAL HARMONIC DISTORTION PLUS NOISE



#### TOTAL HARMONIC DISTORTION PLUS NOISE





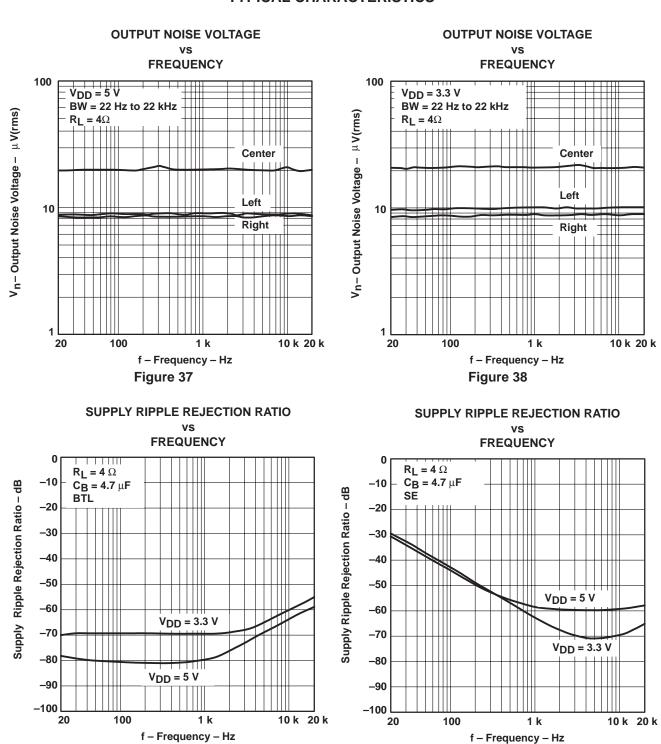
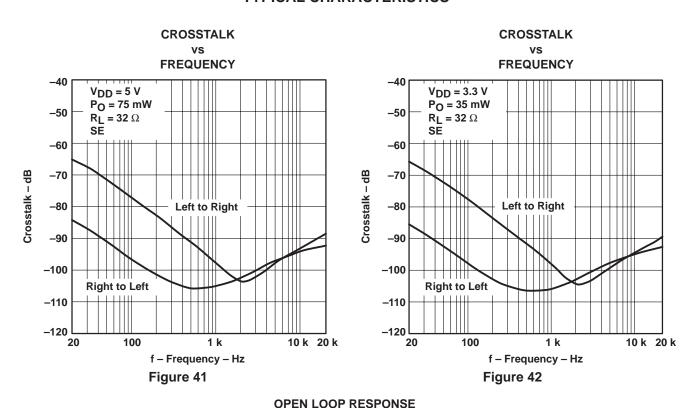
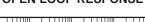




Figure 40

Figure 39





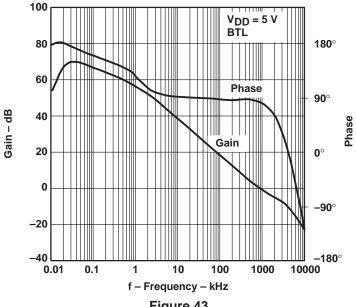
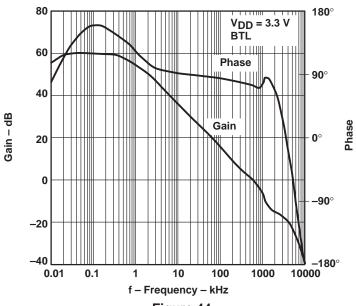


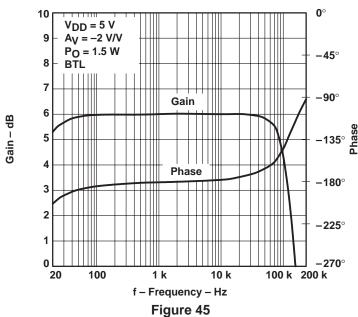
Figure 43

#### **OPEN LOOP RESPONSE**



# Figure 44

#### **CLOSED LOOP RESPONSE**



#### **CLOSED LOOP RESPONSE**

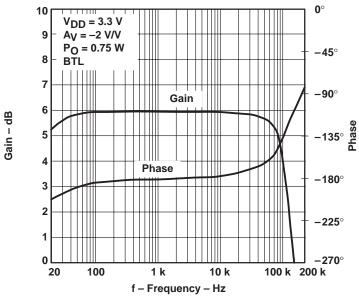


Figure 46

#### **CLOSED LOOP RESPONSE**

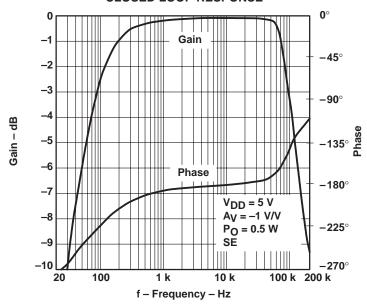
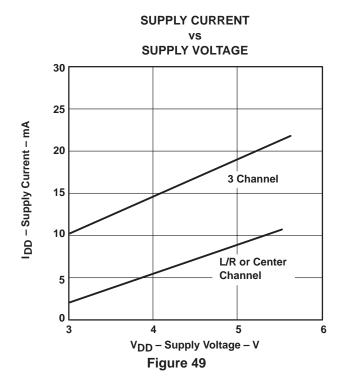
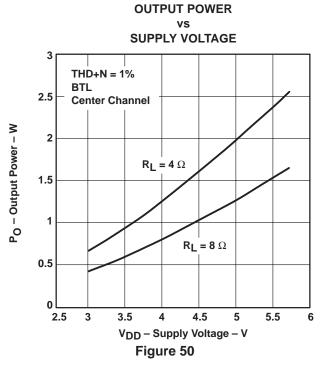


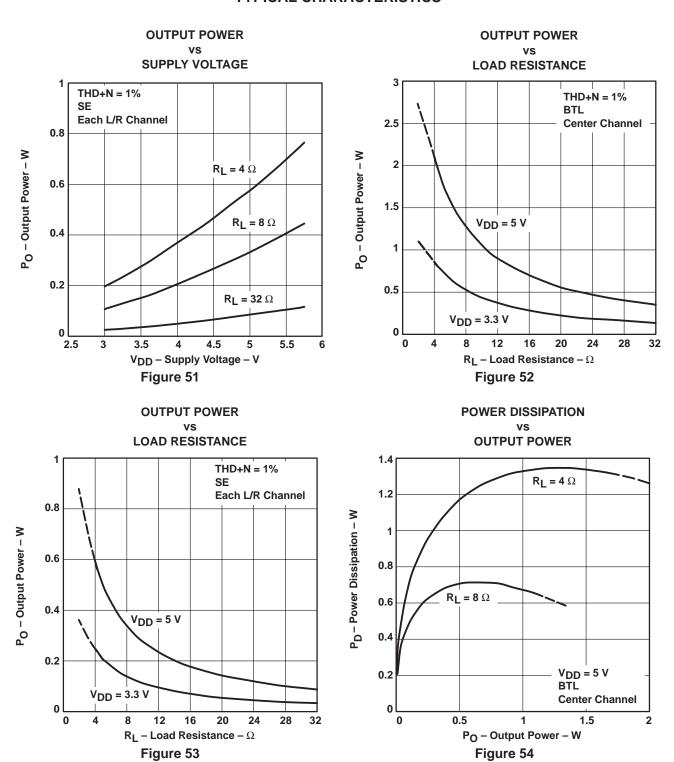
Figure 47

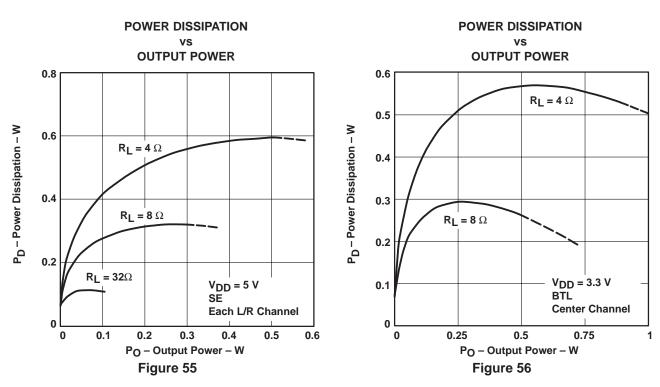
#### **CLOSED LOOP RESPONSE 0**° Gain -45° -2 -3 -90° -135° SEL− -5 -6 -180° -7 $V_{DD} = 3.3V$ $A_V = -1 \text{ V/V}$ -8 $P_0 = 0.25 \text{ W}$ **-225**° SĚ -9 **-270**° 20 100 1 k 10 k 100 k 200 k f - Frequency - Hz

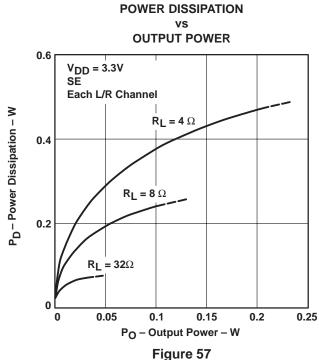
Figure 48











#### THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 58) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

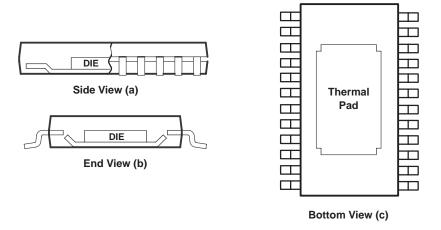


Figure 58. Views of Thermally Enhanced PWP Package

#### bridged-tied load versus single-ended mode

Figure 59 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA0103 center -channel BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up the other side is slewing down and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging  $2 \times V_{O(PP)}$  into the power equation, where voltage is squared, yields  $4\times$  the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$Power = \frac{V_{(rms)}^{2}}{R_{L}}$$
(1)

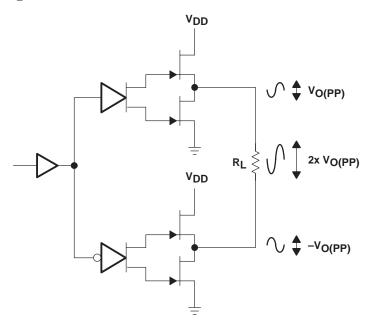


Figure 59. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an  $8-\Omega$  speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration of the L/R channels as shown in Figure 60. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33  $\mu$ F to 1000  $\mu$ F) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.



$$f_{C} = \frac{1}{2\pi R_{L} C_{C}} \tag{2}$$

For example, a  $68-\mu$ F capacitor with an  $8-\Omega$  speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

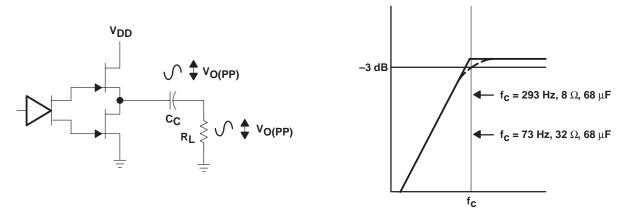


Figure 60. Single-Ended Configuration and Frequency Response

#### BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from  $V_{DD}$ . The internal voltage drop multiplied by the RMS value of the supply current,  $I_{DD}$ rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 61).

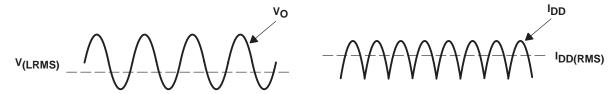


Figure 61. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

Efficiency = 
$$\frac{P_L}{P_{SUP}}$$
 (3)

Where:

$$P_{L(BTL)} = \frac{V_L rms^2}{R_L} = \frac{V_{PP}}{2R_L}, V_{PP} = \sqrt{P_L R_L 2}$$

$$V_L rms(BTL) = \frac{V_{PP}}{2\sqrt{2}} \times 2 = \frac{V_{PP}}{\sqrt{2}}$$

$$P_{SUP} = V_{DD} I_{DD} rms = \frac{V_{DD} V_{PP}}{\pi R_L}$$

$$I_{DD} rms = \frac{V_{PP}}{\pi R_L}$$

Efficiency of a BTE Configuration =  $\frac{P_L}{P_{SUP}} = \frac{V_{PP}^2}{2R_L} \times \frac{\pi R_L}{V_{DD} V_{PP}} = \frac{V_{PP} \pi}{2V_{DD}} = \frac{\pi \sqrt{2P_L R_L}}{2V_{DD}}$  (4)

Equation 4 can also be used for SE operations.

Table 1 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8- $\Omega$  loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 1. Efficiency Vs Output Power in 5-V 8- $\Omega$  BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-TO-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	1.25 70.2		0.53

<sup>†</sup> High peak voltages cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4,  $V_{DD}$  is in the denominator. This indicates that as  $V_{DD}$  goes down, efficiency goes up. As the numerator values of  $R_L$  and  $P_L$  decrease, efficiency decreases.



For example, if the 5-V supply is replaced with a 3.3-V supply (TPA0103 has a maximum recommended  $V_{DD}$  of 5.5 V) in the calculations of Table 1 then efficiency at 0.5 W would rise from 44% to 67% and internal power dissipation would fall from 0.62 W to 0.25 W at 5 V. Then for a stereo 0.5-W system from a 3.3-V supply, the maximum draw would only be 1.5 W as compared to 2.24 W from 5 V. In other words, use the efficiency analysis to chose the correct supply voltage and speaker impedance for the application.

#### selection of components

Figure 62 and Figure 63 are a schematic diagrams of typical computer application circuits.

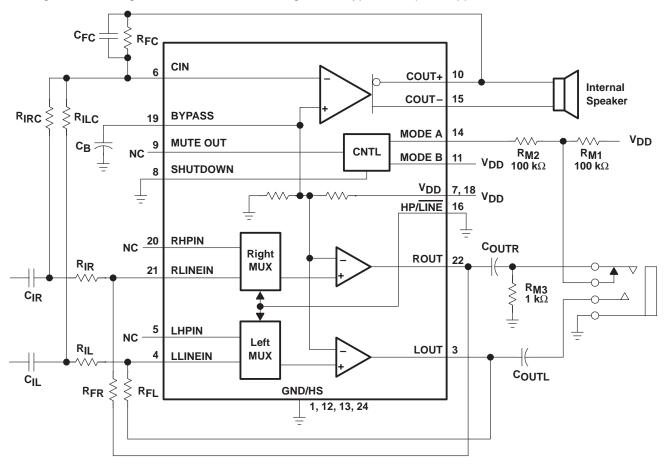
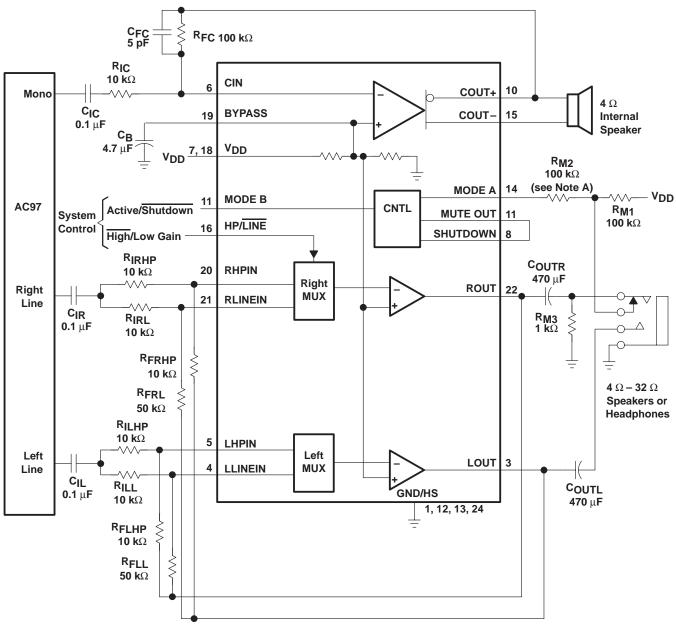


Figure 62. TPA0103 Minimum Configuration Application Circuit



NOTE A: This connection is for ultralow current in shutdown mode.

Figure 63. TPA0103 Full Configuration Application Circuit



#### gain setting resistors, RF and RI

The gain for each audio input of the TPA0103 is set by resistors  $R_F$  and  $R_I$  according to equation 5 for BTL mode.

BTL Gain = 
$$-2\left(\frac{R_F}{R_I}\right)$$
 (5)

In SE mode the gain is set by the R<sub>F</sub> and R<sub>I</sub> resistors and is shown in equation 6. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2, from equation 5, is not included.

SE Gain = 
$$-\left(\frac{R_F}{R_I}\right)$$
 (6)

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA0103 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of  $R_F$  increases. In addition, a certain range of  $R_F$  values are required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 k $\Omega$  and 20 k $\Omega$ . The effective impedance is calculated in equation 7.

Effective Impedance = 
$$\frac{R_F R_I}{R_F + R_I}$$
 (7)

As an example consider an input resistance of 10 k $\Omega$  and a feedback resistor of 50 k $\Omega$ . The BTL gain of the amplifier would be –10 and the effective impedance at the inverting terminal would be 8.3 k $\Omega$ , which is well within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of  $R_{\text{F}}$  above  $50~\text{k}\Omega$  the amplifier tends to become unstable due to a pole formed from  $R_{\text{F}}$  and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with  $R_{\text{F}}$  when  $R_{\text{F}}$  is greater than  $50~\text{k}\Omega$ . This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 8.

$$f_{c(lowpass)} = \frac{1}{2\pi R_F C_F}$$
 (8)

For example, if  $R_F$  is 100 k $\Omega$  and Cf is 5 pF then  $f_c$  is 318 kHz, which is well outside of the audio range.

#### input capacitor, CI

In the typical application an input capacitor,  $C_I$ , is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case,  $C_I$  and  $R_I$  form a high-pass filter with the corner frequency determined in equation 9.

$$f_{c(highpass)} = \frac{1}{2\pi R_{I}C_{I}}$$
 (9)

The value of  $C_I$  is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where  $R_I$  is 10 k $\Omega$  and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 10.

$$C_{I} = \frac{1}{2\pi R_{I} f_{C}} \tag{10}$$

In this example,  $C_I$  is  $0.40~\mu F$  so one would likely choose a value in the range of  $0.47~\mu F$  to  $1~\mu F$ . A further consideration for this capacitor is the leakage path from the input source through the input network  $(R_I, C_I)$  and the feedback resistor  $(R_F)$  to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at  $V_{DD}/2$ , which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

#### power supply decoupling, CS

The TPA0103 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1  $\mu\text{F}$  placed as close as possible to the device  $V_{DD}$  lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10  $\mu\text{F}$  or greater placed near the audio power amplifier is recommended.



#### midrail bypass capacitor, CB

The midrail bypass capacitor,  $C_B$ , serves several important functions. During startup or recovery from shutdown mode,  $C_B$  determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 25-k $\Omega$  source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 11 should be maintained.

$$\frac{1}{\left(\mathsf{C}_\mathsf{B} \times 25 \ \mathsf{k}\Omega\right)} \le \frac{1}{\left(\mathsf{C}_\mathsf{I}\mathsf{R}_\mathsf{I}\right)} \tag{11}$$

As an example, consider a circuit where  $C_B$  is 0.1  $\mu$ F,  $C_I$  is 0.22  $\mu$ F and  $R_I$  is 10  $k\Omega$ . Inserting these values into the equation 10 we get 400  $\leq$  454 which satisfies the rule. Bypass capacitor,  $C_B$ , values of 0.1  $\mu$ F to 1  $\mu$ F ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

#### output coupling capacitor, CC

In the typical single-supply SE configuration, an output coupling capacitor (C<sub>C</sub>) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 12.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C}$$
 (12)

The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of  $C_C$  are required to pass low frequencies into the load. Consider the example where a  $C_C$  of 330  $\mu$ F is chosen and loads vary from 4  $\Omega$ , 8  $\Omega$ , 32  $\Omega$ , to 47 k $\Omega$ . Table 2 summarizes the frequency response characteristics of each configuration.

### output coupling capacitor, C<sub>C (continued)</sub>

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

RL	c <sub>C</sub>	LOWEST FREQUENCY
4 Ω	330 μF	120 Hz
8 Ω 330 μF		60 Hz
32 Ω 330 μF		15 Hz
47,000 Ω 330 μF		0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4- $\Omega$  load, an 8- $\Omega$  load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the relationship shown in equation 13.

$$\frac{1}{\left(\mathsf{C}_{\mathsf{B}} \times 25 \ \mathsf{k}\Omega\right)} \le \frac{1}{\left(\mathsf{C}_{\mathsf{I}}\mathsf{R}_{\mathsf{I}}\right)} \ll \frac{1}{\mathsf{R}_{\mathsf{L}}\mathsf{C}_{\mathsf{C}}} \tag{13}$$

#### mode control resistor network, R<sub>M1</sub>, R<sub>M2</sub>, R<sub>M3</sub>

Using a readily available 1/8-in. (3.5-mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed, the 100-k $\Omega$ /1-k $\Omega$  divider (see Figure 64) pulls the MODE A input low. When a plug is inserted, the 1-k $\Omega$  resistor is disconnected and the MODE A input is pulled high. When the input goes high, the center BTL amplifier is shutdown causing the speaker to mute. The SE amplifiers then drive through the output capacitors (C<sub>O</sub>) into the headphone jack.

#### Input MUX operation

The HP/LINE MUX feature gives the audio designer the flexibility of a multichip design in a single IC (see Figure 64). The primary function of the MUX is to allow different gain settings for different types of audio loads. Speakers typically require approximately a factor of 10 more gain for similar volume listening levels as compared to headphones. To achieve headphone and speaker listening parity, the resistor values would need to be set as follows:

$$Gain_{(HP)} = -\left(\frac{R_{F(HP)}}{R_{I(HP)}}\right)$$
 (14)

If, for example  $R_{I(HP)} = 20 \text{ k}\Omega$  and  $R_{F(HP)} = 20 \text{ k}\Omega$  then SE  $Gain_{(HP)} = -1$ 

$$Gain_{(LINE)} = -\left(\frac{R_{F(LINE)}}{R_{I(LINE)}}\right)$$
 (15)

If, for example  $R_{I(LINE)} = 10 \text{ k}\Omega$  and  $R_{F(LINE)} = 100 \text{ k}\Omega$  then  $Gain_{(LINE)} = -10$ 



#### Input MUX operation (continued)

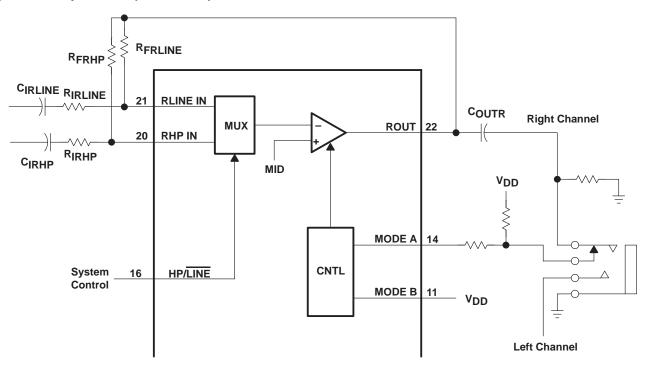


Figure 64. TPA0103 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important.

#### mute and shutdown modes

The TPA0103 employs both a mute and a shutdown mode of operation designed to reduce supply current,  $I_{DD}$ , to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state,  $I_{DD} = 5 \,\mu\text{A}$ . SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable. Mute mode alone reduces  $I_{DD} < 1 \,\text{mA}$ .

#### mute and shutdown modes (continued)

**Table 3. Shutdown and Mute Mode Functions** 

	INPL	тѕ†		OUTPUT	AMPLIFIER	STATE
MODE A	HP/LINE	MODE B	SHUTDOWN	MUTE OUT	INPUT	OUTPUT
Low	Low	Low	Low	Low	L/R Line	3 Channel
Х	Х		High	High	Х	Mute
X	Х	High	Low	High	Х	Mute
Low	High	Low	Low	Low	L/R HP	3 Channel
High	Low	Low	Low	High	L/R Line	Mute
High	High	Low	Low	High	L/R HP	Mute
Low	Low	High	Low	Low	L/R Line	Center BTL
Low	High	High	Low	Low	L/R HP	Center BTL
High	Low	High	Low	Low	L/R Line	L/R SE
High	High	High	Low	Low	L/R HP	L/R SE

<sup>†</sup> Inputs should never be left unconnected.

#### using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

#### 5-V versus 3.3-V operation

The TPA0103 operates over a supply range of 3 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V operation as far as supply bypassing, gain setting, or stability goes. For 3.3-V operation, supply current is reduced from 19 mA (typical) to 13 mA (typical). The most important consideration is that of output power. Each amplifier in TPA0103 can produce a maximum voltage swing of  $V_{DD}-1$  V. This means, for 3.3-V operation, clipping starts to occur when  $V_{O(PP)}=2.3$  V as opposed to  $V_{O(PP)}=4$  V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8- $\Omega$  load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power for a given output-power level than operation from 5-V supplies. When the application demands less than 500 mW, 3.3-V operation should be strongly considered, especially in battery-powered applications.



X = do not care

#### headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA0103 data sheet, one can see that when the TPA0103 is operating from a 5-V supply into a 4- $\Omega$  speaker that 2 W RMS levels are available. Converting watts to dB:

$$P_{dB} = 10 Log \left(\frac{P_W}{P_{ref}}\right)$$

$$= 10 Log \left(\frac{2}{1}\right)$$

$$= 3 dB$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

$$3 dB - 15 dB = -12 dB (15 dB headroom)$$

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref}$$
  
 $P_W = -12 dB = 63 mW (15 dB headroom)$ 

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 1.5 W of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 4- $\Omega$  system, the internal dissipation in the TPA0103 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0103 Power Rating, 5-V, 4-Ω, Three Channel

CONFIGURATION	HEADROOM <sup>†</sup>	POW	ER DISSIPA	ATION	T <sub>A</sub> (MAX)‡		
CONFIGURATION	HEADROOM	2 × L/R -	+ CENTER	= TOTAL	35°C/W	25°C/W	
Contar only Do - 2 W may	0 dB	0	1.25 W	1.25 W	81°C	93°C	
Center only, P <sub>O</sub> = 2 W max	15 dB	0	0.6 W	0.6 W	104°C	110°C	
1/D only D =	0 dB	0.6 W	0	1.2 W	83°C	95°C	
L/R only, $P_O = 500 \text{ mW max}$	15 dB	0.2 W	0	0.4 W	111°C	115°C	
Center, P <sub>O</sub> = 2 W max and	0 dB	0.6 W	1.25 W	2.45 W	39°C	63°C	
$L/R$ , $P_O = 500 \text{ mW max}$	15 dB	0.2 W	0.6 W	1 W	90°C	100°C	

<sup>†</sup> The 2 W max at 0 dB is a maximum level tone that is very loud. 15 dB is a typical headroom requirement for music.

<sup>&</sup>lt;sup>‡</sup>This parameter is based on a maximum junction temperature (T<sub>J</sub>) of 125°C.

#### headroom and thermal considerations (continued)

#### **DISSIPATION RATING TABLE**

PACKAGE	$T_{\mbox{A}} \le 25^{\circ} \mbox{C}$	DERATING FACTOR	T <sub>A</sub> = 70°C	T <sub>A</sub> = 85°C
PWP†	2.7 W	21.8 mW/°C	1.7 W	1.4 W
PWP <sup>‡</sup>	2.8 W	22.1 mW/°C	1.8 W	1.4 W

<sup>†</sup> This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 4 in<sup>2</sup> 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage.

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 LFM and 300 LFM data from the dissipation rating table, the derating factor for the PWP package with 6.9 in<sup>2</sup> of copper area on a multilayer PCB is 22.1 mW/°C and 53.7 mW/°C respectively. Converting this to  $\Theta_{1A}$ :

$$\Theta_{\text{JA}} = \frac{1}{\text{Derating}}$$
 For 0 LFM: 
$$= \frac{1}{22.1 \text{ mW/°C}}$$
 
$$= 45^{\circ}\text{C/W}$$
 For 300 LFM: 
$$= \frac{1}{53.7 \text{ mW/°C}}$$
 
$$= 18^{\circ}\text{C/W}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for the two SE channels and added to the center channel dissipation. Given  $\Theta_{JA}$ , the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0103 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D$$
  
= 125 - 45(0.2 × 2 + 0.6) = 80°C (15 dB headroom, 0 LFM)  
= 125 - 18(0.2 × 2 + 0.6) = 107°C (15 dB headroom, 300 LFM)

Internal dissipation of 1 W is estimated for a 3-channel system with 15 dB headroom per channel (see Table 4 for more information).

NOTE:

Table 4 shows that for most applications no airflow is required to keep junction temperatures in the specified range. The TPA0103 is designed with thermal protection that turns the device off when the junction temperature surpasses  $150^{\circ}$ C to prevent damage to the IC. However, sustained operation above  $125^{\circ}$ C is not recommended. Table 4 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using  $8-\Omega$  speakers dramatically increases the thermal performance by increasing amplifier efficiency.



<sup>&</sup>lt;sup>‡</sup> This parameter is measured with the recommended copper heat sink pattern on an 8-layer PCB, 6.9 in<sup>2</sup> 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in<sup>2</sup>) and layers 3 and 6 at 100% coverage (6 in<sup>2</sup>).





i.com 5-Oct-2007

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPA0103PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA0103PWPG4	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA0103PWPLE	OBSOLETE	HTSSOP	PWP	24		TBD	Call TI	Call TI
TPA0103PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA0103PWPRG4	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

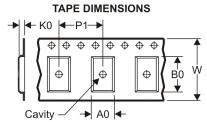
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#### TAPE AND REEL INFORMATION





I		Dimension designed to accommodate the component width
	B0	Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
		Overall width of the carrier tape
	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA0103PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1





#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA0103PWPR	HTSSOP	PWP	24	2000	346.0	346.0	33.0

PWP (R-PDSO-G24)

# PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <a href="http://www.ti.com">http://www.ti.com</a>.

  E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.



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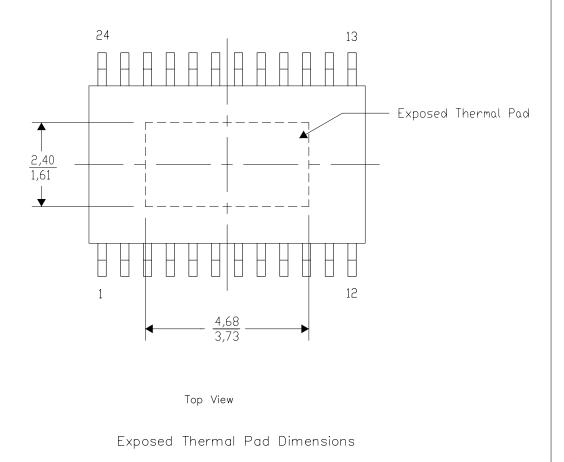
# PWP (R-PDSO-G24) PowerPAD™ SMALL PLASTIC OUTLINE

#### THERMAL INFORMATION

This PowerPAD $^{\text{TM}}$  package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



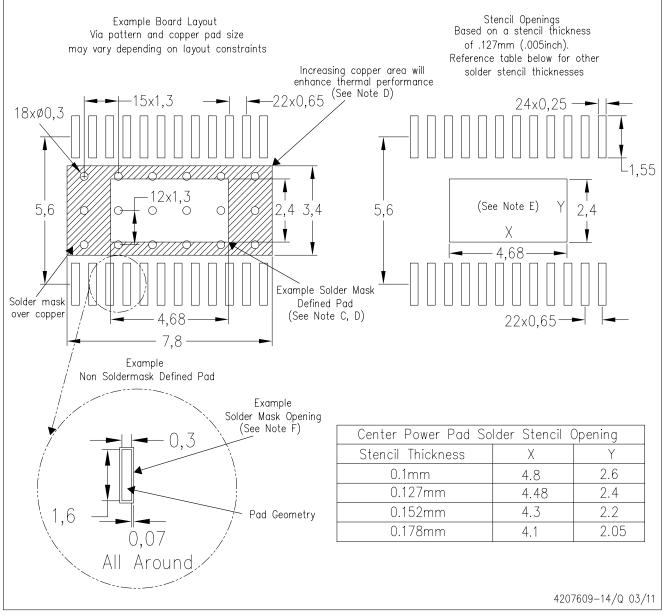
NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments



# PWP (R-PDSO-G24)

# PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="https://www.ti.com">http://www.ti.com</a>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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