# SN74CBT16390 16-BIT TO 32-BIT FET MULTIPLEXER/DEMULTIPLEXER BUS SWITCH

SCDS035E - OCTOBER 1997 - REVISED OCTOBER 2000

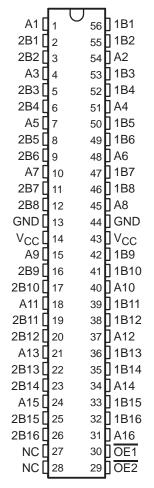
- Member of Texas Instruments' Widebus™
  Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## description

The SN74CBT16390 is a 16-bit to 32-bit switch used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, in which two different banks of memory must be addressed simultaneously. This device also can be used to connect or isolate the PCI bus to one or two slots simultaneously.

Two output enables ( $\overline{OE1}$  and  $\overline{OE2}$ ) control the data flow. When  $\overline{OE1}$  is low, A port is connected to 1B port. When  $\overline{OE2}$  is low, A port is connected to 2B port. When both  $\overline{OE1}$  and  $\overline{OE2}$  are low, the A port is connected to both 1B and 2B ports. The control inputs can be driven with a 5-V CMOS, 5-V TTL, or an LVTTL driver.

# DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

#### **ORDERING INFORMATION**

TA	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CBT16390DL	CBT16390
	330F - DL	Tape and reel	SN74CBT16390DLR	CB116390
	TSSOP – DGG	Tape and reel	SN74CBT16390DGGR	CBT16390
	TVSOP - DGV	Tape and reel	SN74CBT16390DGVR	CY390

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design quidelines are available at www.ti.com/sc/package.



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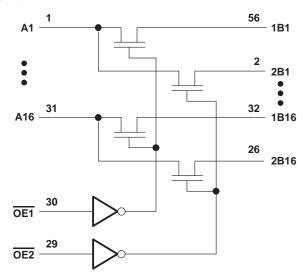
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#### **FUNCTION TABLE**

INP	UTS	FUNCTION
OE1	OE2	FUNCTION
L	L	A = 1B and A = 2B
L	Н	A = 1B
Н	L	A = 2B
Н	Н	Isolation

# logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)		0.5 V to V <sub>CC</sub> + 0.5 V
Continuous channel current		128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)		–50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2)	: DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T <sub>sta</sub>		–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - 2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	MIN	TYP <sup>†</sup>	MAX	UNIT			
VIK		$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$				-1.2	V
ļ.,		$V_{CC} = 0$ ,	V <sub>I</sub> = 5.5 V				10	
11		$V_{CC} = 5.5 \text{ V},$	$V_I = 5.5 \text{ V or GND}$				±1	μΑ
Icc		$V_{CC} = 5.5 \text{ V},$	I <sub>O</sub> = 0,	$V_I = V_{CC}$ or GND			3	μΑ
Δlcc <sup>‡</sup>	Control inputs	V <sub>CC</sub> = 5.5 V,	One input at 3.4 V,	Other input at V <sub>CC</sub> or GND			2.5	mA
Ci	Control inputs	V <sub>I</sub> = 3 V or 0				5		pF
C <sub>io(OFF</sub>	)	$V_O = 3 \text{ V or } 0$				5.5		pF
			V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA		5	7	
ron§		V <sub>CC</sub> = 4.5 V	V   = 0	I <sub>I</sub> = 30 mA		5	7	Ω
			V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA		7	12	

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>pd</sub> ¶	A or B	B or A		0.25	ns
t <sub>en</sub>	ŌĒ	A or B	1.3	5.9	ns
<sup>t</sup> dis	ŌE	A or B	1	5.3	ns

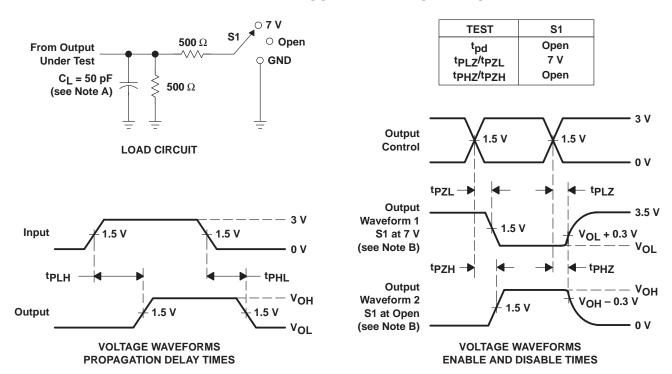
The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).



<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ . ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

<sup>§</sup> Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms



#### PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2009

#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74CBT16390DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT16390DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT16390DGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT16390DGVRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16390DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16390DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16390DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16390DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>&</sup>lt;sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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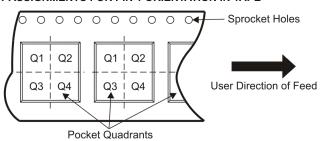
# TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16390DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CBT16390DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16390DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74CBT16390DGVR	TVSOP	DGV	56	2000	346.0	346.0	41.0

# DGG (R-PDSO-G\*\*)

# PLASTIC SMALL-OUTLINE PACKAGE

#### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

# DL (R-PDSO-G\*\*)

### **48 PINS SHOWN**

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

# DGV (R-PDSO-G\*\*)

### **24 PINS SHOWN**

### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

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