

CD54HC4538, CD74HC4538, CD54HCT4538

Data sheet acquired from Harris Semiconductor SCHS123E

High-Speed CMOS Logic Dual Retriggerable Precision Monostable Multivibrator

June 1998 - Revised October 2003

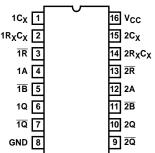
Features

- · Retriggerable/Resettable Capability
- Trigger and Reset Propagation Delays Independent of $R_X,\,C_X$
- · Triggering from the Leading or Trailing Edge
- Q and $\overline{\mathbf{Q}}$ Buffered Outputs Available
- Separate Resets
- . Wide Range of Output Pulse Widths
- Schmitt Trigger Input on A and B Inputs
- Retrigger Time is Independent of C_X
- Fanout (Over Temperature Range)

 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility,
 V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, $I_I \le 1\mu A$ at V_{OL} , V_{OH}

Pinout

CD54HC4538, CD54HCT4538 (CERDIP) CD74HC4538 (PDIP, SOIC, SOP, TSSOP) CD74HCT4538 (PDIP, SOIC) TOP VIEW



Description

The 'HC4538 and 'HCT4538 are dual retriggerable/resettable monostable precision multivibrators for fixed voltage timing applications. An external resistor (R_X) and an external capacitor (C_X) control the timing and the accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and \overline{Q} terminals. The propagation delay from trigger input-to-output transition and the propagation delay from reset input-to-output transition are independent of R_X and C_X.

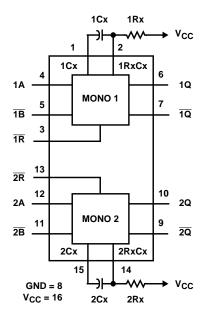
Leading-edge triggering (A) and trailing edge triggering (\overline{B}) inputs are provided for triggering from either edge of the input pulse. An unused "A" input should be tied to GND and an unused \overline{B} should be tied to V_{CC}. On power up the IC is reset. Unused resets and sections must be terminated. In normal operation the circuit retriggers on the application of each new trigger pulse. To operate in the non-triggerable mode \overline{Q} is connected to \overline{B} when leading edge triggering (A) is used or Q is connected to A when trailing edge triggering (\overline{B}) is used. The period (τ) can be calculated from τ = (0.7) R_X, C_X; R_{MIN} is 5k Ω . C_{MIN} is 0pF.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4538F3A	-55 to 125	16 Ld CERDIP
CD54HCT4538F3A	-55 to 125	16 Ld CERDIP
CD74HC4538E	-55 to 125	16 Ld PDIP
CD74HC4538M	-55 to 125	16 Ld SOIC
CD74HC4538MT	-55 to 125	16 Ld SOIC
CD74HC4538M96	-55 to 125	16 Ld SOIC
CD74HC4538NSR	-55 to 125	16 Ld SOP
CD74HC4538PW	-55 to 125	16 Ld TSSOP
CD74HC4538PWR	-55 to 125	16 Ld TSSOP
CD74HC4538PWT	-55 to 125	16 Ld TSSOP
CD74HCT4538E	-55 to 125	16 Ld PDIP
CD74HCT4538M	-55 to 125	16 Ld SOIC
CD74HCT4538MT	-55 to 125	16 Ld SOIC
CD74HCT4538M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

Functional Diagram



TRUTH TABLE

	INPUTS		оиті	PUTS
R	Α	B	Q	Q
L	Х	Х	L	Н
Х	Н	Х	L	Н
Х	Х	L	L	Н
Н	L	↓	7	Т
Н	1	Н	7	7

 $\label{eq:hamiltonian} \begin{array}{l} \mbox{H = High Level, $L = Low Level, \uparrow = Transition from Low to High,} \\ \mbox{\downarrow = Transition from High to Low,} & \mbox{\square} \mbox{\square} & \mbox{One High Level Pulse,} \end{array}$

☐ One Low Level Pulse, X = Irrelevant.

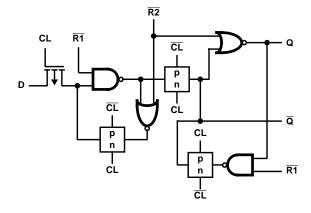


FIGURE 1. FF DETAIL

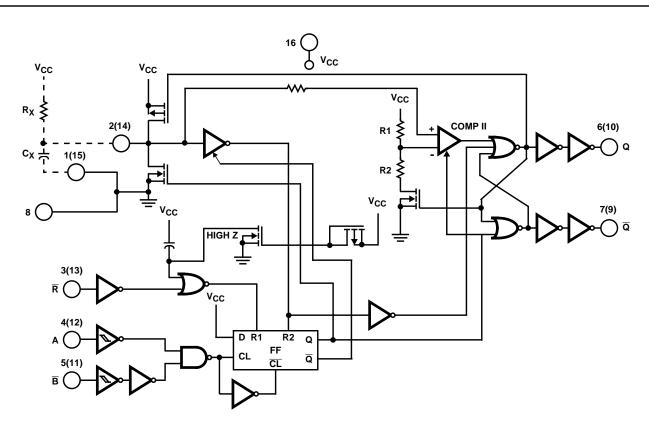


FIGURE 2. LOGIC DIAGRAM (1 MONO)

FUNCTIONAL TERMINAL CONNECTIONS

	V _{CC} TO TERMINAL NUMBER		I -	TO NUMBER	INPUT P	ULSE TO NUMBER	OTHER CONNECTIONS	
FUNCTION	MONO ₁	MONO ₂	MONO ₁	MONO ₂	MONO ₁	MONO ₂	MONO ₁	MONO ₂
Leading-Edge Trigger/Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/Non-Retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/Non-Retriggerable	3	13			5	11	4-6	12-10

NOTES:

- 1. A retriggerable one-shot multivibrator has an output pulse width which is extended one full time period (T) after application of the last trigger pulse.
- 2. A non-triggerable one-shot multivibrator has a time period (T) referenced from the application of the first trigger pulse.

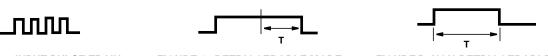


FIGURE 3. INPUT PULSE TRAIN

FIGURE 4. RETRIGGERABLE MODE PULSE WIDTH (A MODE) FIGURE 5. NON-RETRIGGERABLE MODE PULSE WIDTH (A MODE)

Operating Conditions

Temperature Range, T _A
Supply Voltage Range, V _{CC} (Note 3)
HC Types2V to 6V
HCT Types
DC Input or Output Voltage, V _I , V _O 0V to V _{CC}
Input Rise and Fall Times, t _r , t _f
Reset Input:
2V
4.5V 500ns (Max)
6V
Trigger Inputs A or B:
2V Unlimited (Max)
4.5VUnlimited (Max)
6V Unlimited (Max)
External Timing Resistor, R_X (Note 4)
External Timing Capacitor, C_X (Note 4) 0 (Min)

Thermal Information

Package Thermal Impedance, θ _{JA} (see Note 5):
E (PDIP) Package67°C/W
M (SOIC) Package73°C/W
NS (SOP) Package
PW (TSSOP) Package 108 ^o C/W
Maximum Junction Temperature
Maximum Storage Temperature Range65°C to 150°C
Maximum Lead Temperature (Soldering 10s)300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- 3. Unless otherwise specified, all voltages are referenced to ground.
- 4. The maximum allowable values of R_X and C_X are a function of leakage of capacitor C_X, the leakage of the 'HC4538, and leakage due to board layout and surface resistance. Values of R_X and C_X should be chosen so that the maximum current into pin 2 or pin 14 is 30mA. Susceptibility to externally induced noise signals may occur for R_X > 1MΩ.
- 5. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		TES CONDI		Vcc		25°C		-40°C T	O 85°C	-55°C TO 125°C		
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES								-	-		-	
High Level Input	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output	V _{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
Voltage CMOS Loads			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
OWIGO LOAGS			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output	1		-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V

DC Electrical Specifications (Continued)

		CONDI		v _{cc}		25°C		-40°C 1	го 85°С	-55°C T	O 125°C	
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Low Level Output	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
CIVIOS LOAUS			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output	1		-	-	-	-	-	-	-	-	-	V
Voltage			4	4.5	-	-	0.26	-	0.33	-	0.4	V
TTL Loads			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current A, B, R	lı	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μА
Input Leakage Current R _X C _X (Note 6)			-	6	-	-	±0.05	-	±0.5	-	±0.5	μА
Quiescent Device Current	Icc	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μА
Active Device Current Q = High & Pins 2, 14 at V _{CC} /4	Icc	V _{CC} or GND	0	6	-	-	0.6	-	0.8	-	1	mA
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{ОН}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V _{CC} and GND	-	5.5	-		±0.1	-	±1	-	±1	μА
Input Leakage Current R _X C _X (Note 6)			-	5.5	-	-	±0.05	-	±0.5	-	±0.5	μА
Quiescent Device Current	Icc	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μА
Active Device Current Q = High & Pins 2, 14 at V _{CC} /4	I _{CC}	V _{CC} or GND	0	5.5	-	-	0.6	-	0.8	-	1	mA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 7)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μА

- 6. When testing I_{IL} the Q output must be high. If Q is low (device not triggered) the pull-up P device will be ON and the low resistance path from V_{DD} to the test pin will cause a current far exceeding the specification.
- 7. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
All	0.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g. 360µA max at 25°C.

Prerequisite for Switching Specifications

				25°C		-40	°C TO 8	5°C	-55°C TO 125°C			
PARAMETER	SYMBOL	V _{CC} (V)	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
HC TYPES					-			-	-			-
Input Pulse Widths	t _{WH} , t _{WL}											
A, B		2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
R	t _{WL}	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
Reset Recovery Time	t _{REC}	2	5	-	-	5	-	-	5	-	-	ns
		4.5	5	-	-	5	-	-	5	-	-	ns
		6	5	-	-	5	-	-	5	-	-	ns
Retrigger Time (Figure 11)	t _{rT}	5	-	175	-	-	-	-	-	-	-	ns
HCT TYPES												
Input Pulse Widths A, \overline{B}	t _{WH} , t _{WL}	4.5	16	-	-	20	-	-	24	-	-	ns
R	t _{WL}	4.5	20	-	-	25	-	-	30	-	-	ns
Reset Recovery Time	t _{REC}	4.5	5	-	-	5	-	-	5	-	-	ns
Retrigger Time (Figure 11)	t _{rT}	5	-	175	-	-	-	-	-	-	-	ns

Switching Specifications $\text{C}_L = 50 \text{pF}, \text{ Input } t_f, \, t_f = 6 \text{ns}, \, R_X = 10 \text{K}\Omega, \, C_X = 0$

		TEST			25°C		-40 ⁰ (С ТО °С		C TO 5°C	
PARAMETER	SYMBOL	CONDITIONS	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	МАХ	UNITS
HC TYPES											
Propagation Delay	t _{PLH}	C _L = 50pF									
A, \overline{B} to Q			2	-	-	250	-	315	-	375	ns
			4.5	i	-	50	-	63	-	75	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	43	-	54	-	64	ns
A, \overline{B} to \overline{Q}	t _{PHL}	C _L = 50pF	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	43	-	54	-	64	ns
R to Q	t _{PHL}	C _L = 50pF	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	43	-	54	-	64	ns
$\overline{\mathbb{R}}$ to $\overline{\mathbb{Q}}$	t _{PLH}	C _L = 50pF	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	43	-	54	-	64	ns
Output Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Output Pulse Width	τ	C _L = 50pF	3	0.64	-	0.78	0.612	0.812	0.605	0.819	ms
$R_X = 10k, C_X = 0.1\mu F$			5	0.63	-	0.77	0.602	0.798	0.595	0.805	ms
Output Pulse Width Match, Same Package	-	-		-	±1	-	-	-	-	-	%
Power Dissipation Capacitance (Notes 8, 9)	C _{PD}	C _L = 15pF	5	-	136	-	-	-	-	-	pF
Input Capacitance	C _I	C _L = 50pF	-	10	-	10	-	10	-	10	pF
HCT TYPES									•		
Propagation Delay	t _{PLH}										
A, \overline{B} to Q		C _L = 50pF	4.5	-	-	55	-	69	-	83	ns
		C _L = 15pF	5	-	23	-	-	-	-	-	ns
A, \overline{B} to \overline{Q}	t _{PHL}	C _L = 50pF	4.5	-	-	55	-	69	-	83	ns
		C _L = 15pF	5	-	23	-	-	-	-	-	ns

Switching Specifications $C_L = 50 pF$, Input t_r , $t_f = 6 ns$, $R_X = 10 K\Omega$, $C_X = 0$ (Continued)

		TEST			25°C			С ТО °С		C TO 5°C	
PARAMETER	SYMBOL	CONDITIONS	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
R to Q	t _{PHL}	C _L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C _L = 15pF	5	-	17	-	-	-	-	-	ns
\overline{R} to \overline{Q}	t _{PLH}	C _L = 50pF	4.5	-	-	50	-	63	-	75	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
Output Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
Output Pulse Width $R_X = 10k, C_X = 0.1\mu F$	τ	C _L = 50pF	5	0.63	-	0.77	0.602	0.798	0.595	0.805	ms
Output Pulse Width Match, Same Package	-	-	-	-	±1	-	-	-	-	-	%
Power Dissipation Capacitance (Notes 8, 9)	C _{PD}	C _L = 15pF	5	-	134	-	-	-	-	-	pF
Input Capacitance	Cl	C _L = 50pF	-	10	-	10	-	10	-	10	pF

NOTES:

- 8. C_{PD} is used to determine the dynamic power consumption, per one shot.
- 9. $P_D = (C_{PD} + C_X) \ V_{CC}^2 \ f_i \ \Sigma (C_L \ V_{CC}^2 \ f_O)$ where f_i = input frequency, f_O = output frequency, C_L = output load capacitance, C_X = external capacitance V_{CC} = supply voltage assuming $f_i \ll \frac{1}{\tau}$

Test Circuits and Waveforms

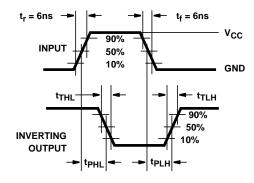


FIGURE 6. HC AND HCU TRANSITION TIMES AND PROPAGA-TION DELAY TIMES, COMBINATION LOGIC

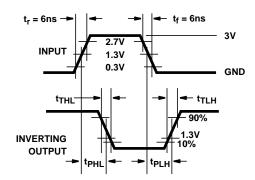


FIGURE 7. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Typical Performance Curves

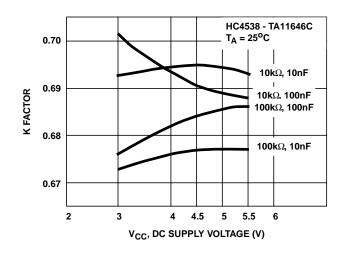


FIGURE 8. K FACTOR vs DC SUPPLY VOLTAGE (V_{CC}) - V

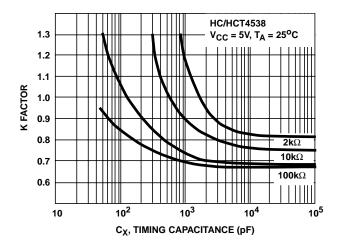


FIGURE 10. K FACTOR vs CX

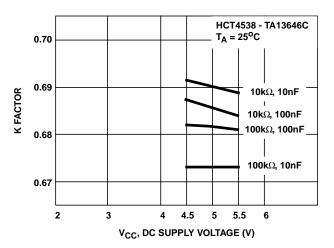


FIGURE 9. K FACTOR vs DC SUPPLY VOLTAGE (V_{CC}) - V

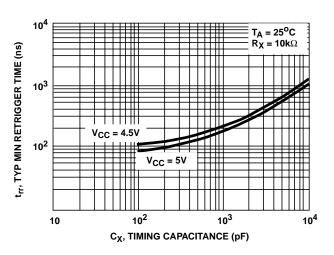
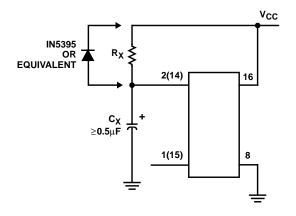


FIGURE 11. MINIMUM RETRIGGER TIME vs TIMING CAPACITANCE

Power-Down Mode

During a rapid power-down condition, as would occur with a power-supply short circuit with a poorly filtered power supply, the energy stored in C_X could discharge into Pin 2 or 14. To aviod possible device damage in this mode, when C_X is $\geq 0.5 \mu F$, a protection diode with a 1 ampere or higher rating (1N5395 or equivalent) and a separate ground return for C_X should be provided as shown in Figure 12.

An alternate protection method is shown in Figure 13, where a 51Ω current-limiting resistor is inserted in series with $C_X.$ Note that a small pulse width decrease will occur however, and R_X must be appropriately increased to obtain the originally desired pulse width.



V_{CC}

R_X

2(14)

51Ω

C_X
≥0.5μF

1(15)

8

FIGURE 12. RAPID POWER-DOWN PROTECTION CIRCUIT

FIGURE 13. ALTERNATE RAPID POWER-DOWN PROTECTION CIRCUIT



5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-8688601EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
CD54HC4538F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD54HC4538F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD54HCT4538F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD74HC4538E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC4538EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC4538M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CD74HC4538PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4538E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT4538EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT4538M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4538M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4538M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4538M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4538ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4538MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4538MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4538MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4538MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

PACKAGE OPTION ADDENDUM



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(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD54HC4538, CD54HCT4538, CD74HC4538, CD74HCT4538:

- Catalog: CD74HC4538, CD74HCT4538
- Automotive: CD74HC4538-Q1, CD74HC4538-Q1
- Military: CD54HC4538, CD54HCT4538

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects





5-Sep-2011

• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All differsions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4538M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4538NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC4538PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4538PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4538M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4538M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4538NSR	SO	NS	16	2000	346.0	346.0	33.0
CD74HC4538PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
CD74HC4538PWT	TSSOP	PW	16	250	346.0	346.0	29.0
CD74HCT4538M96	SOIC	D	16	2500	333.2	345.9	28.6

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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