34-Channel Symmetric Row Driver

Ordering Information

| | Package Options | | | | | | | | | |
|----------|--|------------|-----------------------|--|--|--|--|--|--|--|
| Device | 44 J-Lead Quad Ceramic Chip Carrier Plastic Chip Carrier | | Die in waffle pack | 44 J-Lead Quad Ceramic Chip Carrier (MIL-Std-883 Processed*) | | | | | | |
| HV7022-C | HV7022DJ-C | HV7022PJ-C | HV7022X-C | RBHV7022DJ-C | | | | | | |

^{*}For Hi-Rel process flows, refer to page 5-3 of the databook.

Features

- ☐ Processed with HVCMOS® technology
- Symmetric row drive (reduces latent imaging in ACTFEL displays)
- Output voltages up to 230V
- Low-power level shifting
- ☐ Source/Sink current 70mA (min.)
- Shift register speed 4MHz
- Pin-programmable shift direction
- 44-lead plastic & ceramic surface-mount packages
- Hi-Rel processing available

Absolute Maximum Ratings

| Supply voltage, V _{DD} ¹ | -0.3V to +15V | | | |
|---|--------------------------------|------------------|---------|----------------------|
| Supply voltage, V _{PP} ¹ | | | -0.3V | to +250V |
| Logic input levels ¹ | -0.3V to V _{DD} +0.3V | | | |
| Ground current ² | | | | 1.5A |
| Continuous total power dissipati | ion ³ : | Plastic Ceram | | 1200mW 1500mW |
| Operating temperature range | Plas Cera | stic amic | | to +85°C to 125°C |
| Storage temperature range | | | -65°C t | o +150°C |
| Lead temperature 1.6mm (1/16 from case for 10 seconds | inch) | | | 260°C |

Notes:

- 1. All voltages are referenced to GND.
- 2. Duty cycle is limited by the total power dissipated in the package.
- For operation above 25°C ambient derate linearly to maximum operating temperature at 25mW/°C for plastic and at 15mW/°C for ceramic.

General Description

The HV7022-C is a low-voltage serial to high-voltage parallel converter with push-pull outputs. It is especially suited for use as a symmetric row driver in AC thin-film electroluminescent (ACTFEL) displays. The HV70 offers 34 output lines, a direction (DIR) pin to give CW or CCW shift register loading, output enable (OE), and polarity (POL) control. After DATA INPUT is entered (on the falling edge of CLOCK), a logic high will cause the output to swing to V_{PP} if POL is high, or to GND if POL is low.

For Detailed circuit and application information, please refer to Application Note AN-H3.

02/96/022

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Electrical Characteristics

(over recommended operating conditions of $V_{DD} = 12V$, $T_A = 25$ °C and $V_{PP} = 230V$ unless otherwise noted)

DC Characteristics

| Symbol | Parameter | Min | Max | Units | Conditions | |
|------------------|-------------------------------------|-------------------|-----|-------|--|---|
| I _{DD} | V _{DD} supply current | | 10 | mA | f _{CLK} = 4MHz | |
| I _{PP} | High voltage supply cui | rrent | | 4 | mA | 1 Output high ¹ |
| | | | | 100 | μΑ | All Outputs low or High-Z |
| | | | | 750 | μА | All Outputs low or High-Z (125°C) |
| I _{DDQ} | Quiescent V _{DD} supply of | | 100 | μΑ | All V _{IN} = GND or V _{DD} | |
| V _{OH} | High-level output | HV _{OUT} | 195 | | V | I _O = -70mA (-50mA) ² |
| | | Data out | 11 | | V | I _O = -500μA |
| V _{OL} | Low-level output | HV _{OUT} | | 30 | V | I _O = 70mA (+50mA) ² |
| | | Data out | | 1 | V | I _O = 500μA |
| I _{IH} | High-level logic input cu | | 1 | μΑ | V _{IH} = 12V | |
| I _{IL} | Low-level logic input cu | irrent | | -1 | μΑ | V _{IL} = 0V |

Notes:

AC Characteristics $(V_{DD} = 12V, T_C = 25^{\circ}C)$

| Symbol | Parameter | Min | Max | Units | Conditions |
|-------------------|--|-----|------|-------|--|
| f _{CLK} | Clock frequency | | 4 | MHz | |
| t _W | Pulse duration clock high or low | 125 | | ns | |
| t _{SUD} | Data set-up time before falling clock | 100 | | ns | |
| t _{HD} | Data hold time after falling clock | 100 | | ns | |
| t _{SUC} | Setup time clock low before V _{PP} ↑ or GND↓ | 300 | | ns | |
| t _{SUE} | Setup time enable high before V _{PP} ↑ or GND↓ | 300 | | ns | |
| t _{SUP} | Setup time polarity high or low before V _{PP} ↑ or GND↓ | 300 | | ns | |
| t _{HC} | Hold time clock high after V _{PP} ↑ or GND↓ | 500 | | ns | |
| t _{HE} | Hold time enable high after V _{PP} ↑ or GND↓ | 300 | | ns | |
| t _{HP} | Hold time polarity high or low after V _{PP} ↑ or GND↓ | 300 | | ns | |
| t _{DHL} | Delay time high to low level output from clock | | 150 | ns | C _L = 10pF |
| t _{DLH} | Delay time low to high level output from clock | | 200 | ns | C _L = 10pF |
| t _{THL} | Transition time high to low level serial output | | 200 | ns | C _L = 15pF |
| t _{TLH} | Transition time low to high level serial output | | 100 | ns | C _L = 15pF |
| t _{ONH} | High level turn-on time Q outputs from enable | | 500 | ns | $I_{O} = -50 \text{ mA}, V_{OH} = 195 \text{V}$ $R_{L} = 2 \text{ k}\Omega \text{ to } 95 \text{V}$ |
| t _{ONL} | Low level turn-on time Q outputs from enable | | 500 | ns | $I_O = 50 \text{ mA}, V_{OH} = 130 \text{V}$ $R_L = 2 \text{ k}\Omega \text{ to } 30 \text{V}$ |
| t _{OFFH} | High level turn-off time Q outputs from enable | | 1000 | ns | $I_O = -50 \text{ mA}, V_{OH} = 195 \text{V}$ $R_L = 2 \text{ k}\Omega \text{ to } 95 \text{V}$ |
| t _{OFFL} | Low level turn-off time Q outputs from enable | | 500 | ns | $I_O = 50 \text{ mA}, V_{OH} = 130 \text{V}$ $R_L = 2 \text{ k}\Omega \text{ to } 30 \text{V}$ |
| | Slew rate, V _{PP} or GND | | 45 | V/μs | With one active output driving a 4.7 nF load to V_{PP} or GND |

^{1.} The total number of ON outputs times the duty cycle must not exceed the allowable package power disspation.

^{2.} Over military temperature range (-55°C to 125°C).

Recommended Operating Conditions

| Symbol | Paramete | Min | Max | Units | |
|------------------|-------------------------------------|---|------|-------|-----|
| V _{DD} | Logic supply voltage | | 10.8 | 13.2 | V |
| V _{PP} | High voltage supply | | | 230 | V |
| V _{IH} | High-level input voltage | V _{DD} = 10.8V | 8.1 | | V |
| | | V _{DD} = 13.2V | 9.9 | | |
| V _{IL} | Low-level input voltage | V _{DD} = 10.8V | | 2.7 | V |
| | | V _{DD} = 13.2V | | 3.3 | |
| f _{CLK} | Clock frequency | | | 4 | MHz |
| T _A | Operating free-air temperature | Plastic | -40 | +85 | °C |
| | | Ceramic | -55 | +125 | °C |
| I _{OD} | Allowable pulse current through out | Allowable pulse current through output diodes | | | |

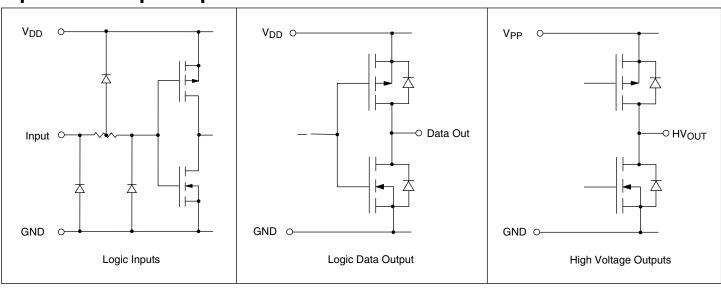
Note:

Power-up sequence should be the following:

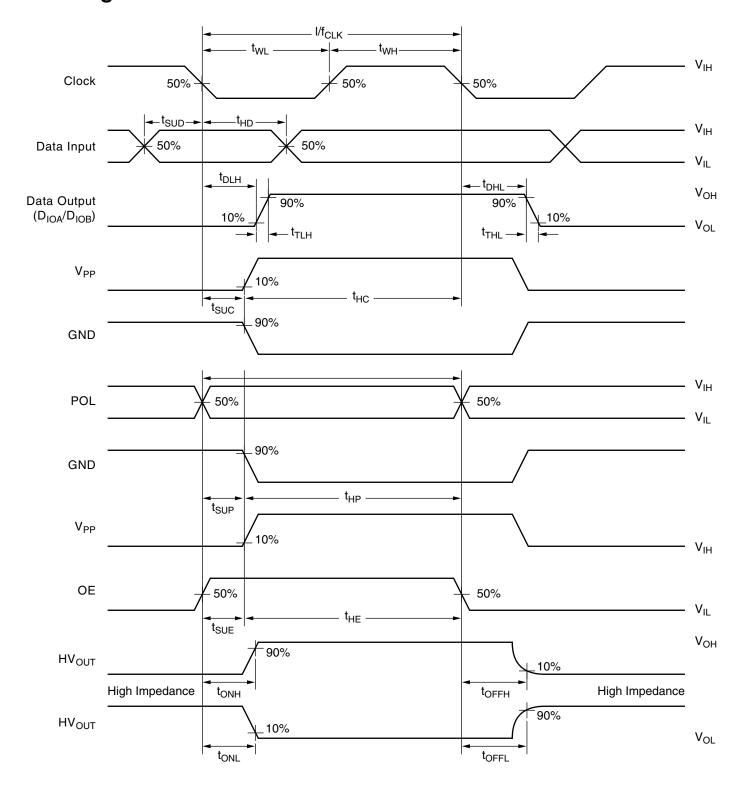
- 1. Connect ground.
- 2. Apply V_{DD} .
- 3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
- 4. Apply V_{PP}.
- 5. The V_{PP} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.

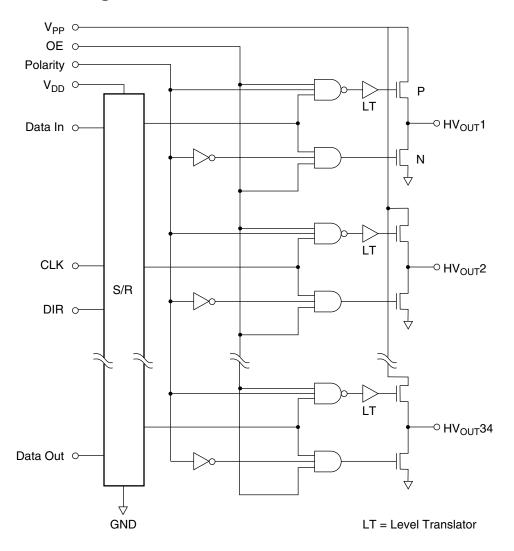
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

| | | | Inputs | | Outputs | | | | |
|------------------|----------|-----|--------|-----|---------|---------------------------|----------------|-----------------|--|
| I/O Relations | CLK | DIR | Data | POL | OE | Shift Reg | HV Outputs | Data Out | |
| O/P HIGH | Х | Х | Н | Н | Н | * | Н | | |
| O/P OFF | Х | Х | L | Н | Н | * | HIGH-Z | * | |
| O/P LOW | X | X | Н | L | Н | * | L | * | |
| O/P OFF | Х | Х | L | L | Н | * | HIGH-Z | * | |
| O/P OFF | Х | X | Х | Х | L | * | All O/P HIGH-Z | * | |
| Load S/R, | ↓ | L | Х | Х | Х | $Q_n \rightarrow Q_{n+1}$ | * | Q ₃₄ | |
| set DIR | ↓ | Н | Х | Х | Х | $Q_n \rightarrow Q_{n-1}$ | * | $Q_{_1}$ | |
| | No ↓ | Х | Х | Х | Х | * | No Change | No Change | |

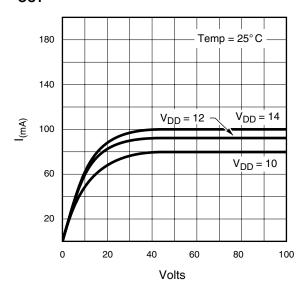
Notes:

 $H = logic \ high \ level, \ L = logic \ low \ level, \ X = irrelevant, \ \downarrow = high-to-low \ transition,$

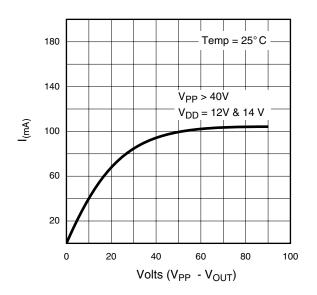
 $Q_1 = HV_{OUT} 1$, $Q_n = HV_{OUT}(n)$, etc.

^{* =} dependent on previous state and whether an O/P or S/R command occured.

HV_{OUT} Characteristics



Output N-Channel Characteristics through FET



Output P-Channel Characteristics through FET

Pin Configurations

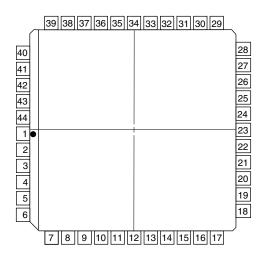
HV70 44 Pin J-Lead Package

| Pin | Function | Pin | Function |
|-----|-------------------------|-----|-------------------------|
| 1 | HV _{OUT} 18/17 | 23 | DIR |
| 2 | HV _{OUT} 17/18 | 24 | $V_{_{ m DD}}$ |
| 3 | HV _{OUT} 16/19 | 25 | Polarity |
| 4 | HV _{OUT} 15/20 | 26 | Data In |
| 5 | HV _{OUT} 14/21 | 27 | V_{pp} |
| 6 | HV _{OUT} 13/22 | 28 | N/C |
| 7 | HV _{OUT} 12/23 | 29 | HV _{OUT} 34/1 |
| 8 | HV _{OUT} 11/24 | 30 | HV _{OUT} 33/2 |
| 9 | HV _{OUT} 10/25 | 31 | HV _{OUT} 32/3 |
| 10 | HV _{OUT} 9/26 | 32 | HV _{OUT} 31/4 |
| 11 | HV _{out} 8/27 | 33 | HV _{оит} 30/5 |
| 12 | HV _{OUT} 7/28 | 34 | HV _{OUT} 29/6 |
| 13 | HV _{OUT} 6/29 | 35 | HV _{OUT} 28/7 |
| 14 | HV _{OUT} 5/30 | 36 | HV _{OUT} 27/8 |
| 15 | HV _{OUT} 4/31 | 37 | HV _{OUT} 26/9 |
| 16 | HV _{OUT} 3/32 | 38 | HV _{OUT} 25/10 |
| 17 | HV _{OUT} 2/33 | 39 | HV _{OUT} 24/11 |
| 18 | HV _{OUT} 1/34 | 40 | HV _{OUT} 23/12 |
| 19 | Data Out | 41 | HV _{OUT} 22/13 |
| 20 | Output Enable | 42 | HV _{OUT} 21/14 |
| 21 | Clock | 43 | HV _{OUT} 20/15 |
| 22 | GND | 44 | HV _{OUT} 19/16 |

Note:

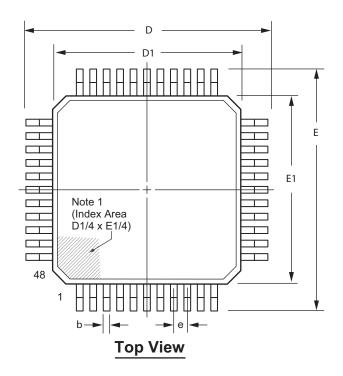
Pin designation for DIR L/H $Example: For DIR = L, pin 1 is HV_{OUT} 18$ $For DIR = H, pin 1 is HV_{OUT} 17$

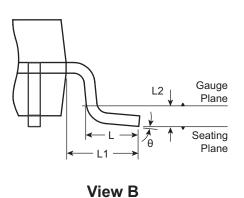
Package Outline

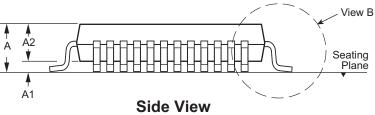


top view
44-pin J-Lead Package

44-Lead PQFP Package Outline (PG)







Side View

Note 1:A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

| Symbo | ol | Α | A1 | A2 | b | D | D1 | E | E1 | е | L | L1 | L2 | θ | θ1 |
|----------------|-----|------|------|------|------|-------|-------|-------|-------|-------------|------|-------------|-------------|------|-----|
| Dimension (mm) | MIN | - | 0.25 | 1.95 | 0.30 | 13.65 | 9.80 | 13.65 | 9.80 | 0.73 | | | 0.25 BSC | 3.5° | 5° |
| | NOM | - | - | 2.00 | - | 13.90 | 10.00 | 13.90 | 10.00 | 0.80 BSC | 0.88 | 1.95 REF | | - | - |
| | MAX | 2.45 | - | 2.10 | 0.45 | 14.15 | 10.20 | 14.15 | 10.20 | 200 | 1.03 | 1,721 | 200 | 7° | 16° |

JEDEC Registration M0-112, Variation AA-2, Issue B, Sep.1995.

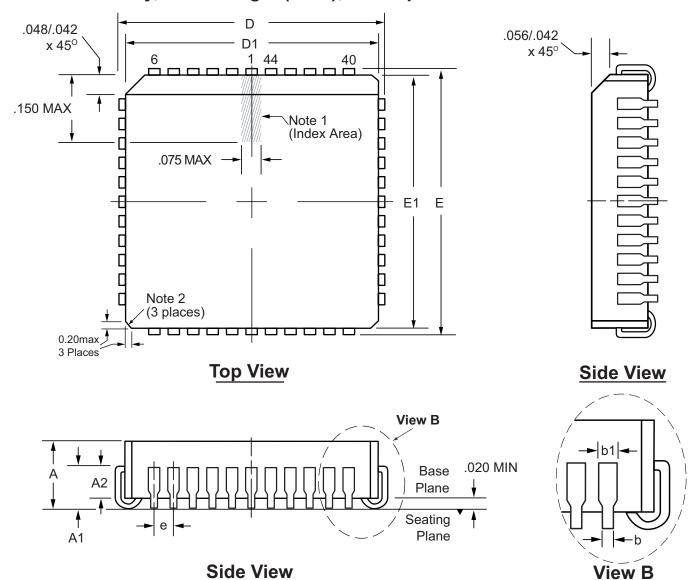
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Doc. #: DSPD-44PQFPPG

44-Lead PLCC Package Outline (PJ)

.653x.653in body, .180in height (max.), .050in pitch



Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature. 2. Exact shape of this feature is optional.

| Sym | bol | Α | A1 | A2 | b | b1 | D | D1 | E | E1 | е |
|--------------------|-----|------|------|------|------|------|------|------|------|------|-------------|
| Dimension (inches) | MIN | .165 | .090 | .062 | .013 | .026 | .685 | .650 | .685 | .650 | 0.50 |
| | NOM | .172 | .105 | - | - | - | .690 | .653 | .690 | .653 | .050 BSC |
| (mones) | MAX | .180 | .120 | .083 | .021 | .036 | .695 | .656 | .695 | .656 | ВОО |

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993. Drawings are not to scale.

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View B

Doc. #: DSPD-44PLCCPJ