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DLP[®] Digital Controller for the DLP5500 DMD

Check for Samples: DLPC200

FEATURES

- Operates the DLPA200 and DLP5500
- Two 24-Bit Input Ports (RGB888) With Pixel **Clock Support up to 80 MHz**
 - Port 1 Supports HDMI Input
 - Port 2 Supports Input via an Expansion Card
- Supports EDID via I²C
- Input Image Size 1024 × 768 (XGA)
- **Device Configuration Control Interface:** USB and SPI
- Video Input (via Port 1 or Port 2), 60 Hz:
 - Programmable Degamma
 - Spatial-Temporal Multiplexing (Dithering)
- Structured Light Pattern Mode
 - Download Pattern Data Directly to Device
 - Display Patterns up to 5000 Hz for Binary Patterns
 - Display Patterns up to 700 Hz for 8-Bitsper-Pixel Patterns
 - Programmable Reordering of Patterns

- 200-MHz LVDS 1.0 (DDR) DMD Interface
- Supports Three Outputs for Camera Syncing
- Supports Two Inputs for External Triggers
- Supports Eight General Purpose I/Os •
- External Memory Support: 133-MHz DDR-2 • SDRAM
- Serial FLASH Interface
- **Parallel FLASH Interface**
- **System Control:**
 - **Programmable LED Current Control** Adjustment of Red, Green, Blue, and Infrared LEDs
 - **Control of DMD Micromirror Driver** (DLPA200)
 - DMD Horizontal and Vertical Image Flip
 - **Built-In Test Pattern Generation**
 - In-Field Remote Download of Firmware Updates
- Packaged in 780-Pin Fineline Ball-Grid Array (FBGA)

DESCRIPTION

The DLPC200 performs image processing and control, along with DMD data formatting, for driving a 0.55 XGA DMD (DLP5500).

The DLPC200 is one of three components in the 0.55 XGA Chipset (see Figure 1). Proper function and operation of the DLP5500 requires that it be used in conjunction with the other components of the 0.55 XGA Chipset. See the 0.55 XGA Chipset Data Sheet for further details (TI literature number DLPZ004B).

In DLP electronics solutions, image data is 100% digital from the DLPC200 input port to the image projected on to the display screen. The image stays in digital form and is never converted into an analog signal. The DLPC200 processes the digital input image and converts the data into a format needed by the DMD. The DMD then reflects light to the screen using binary pulse-width modulation (PWM) for each pixel mirror.

The DLPC200 interfaces with an LED driver via an SPI interface. It sends strobes to indicate when each of the red, green, blue, or infrared LEDs should be enabled or disabled, and command packets are used to control the brightness of the LEDs.

Commands or programmable patterns can be input to the DLPC200 over either a SPI interface or a USB interface. When patterns are used, the DLPC200 can be synchronized to a camera or external source. This allows for the external interface to sync to the patterns displayed or for the patterns to be synchronized to the external source.

The DLCP200 allows the user to redefine the display order of the patterns that have been downloaded to memory. This allows any pattern stored in memory to be displayed in any order. Degamma and dithering are never applied to patterns, but can be applied to data processed through either of the two pixel ports.

See Table 1 for frame rates that can be supported by the DLPC200.



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DLPS014D - APRIL 2010 - REVISED MARCH 2012

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

	MODE	MIN	UNIT		
Structured light	1 bit per pixel	c	5000		
Structured light	8 bits per pixel	Ö	700	112	
Video		6	60	Hz	

The digital input interface levels for image data are nominally 1.8 V or 3.3 V. Port 1 input is 3.3 V and port 2 input is 1.8 V.

DLPR200F firmware is provided by Texas Instruments to support the operation of video and structured light mode. To locate DLPR200F, go to www.ti.com and search for the keyword *DLPR200*.

Related Documents

DOCUMENT	TI LITERATURE NUMBER
DLP 0.55 XGA Chipset data sheet	DLPZ004B
DLPA200 DMD Micromirror Driver	DLPS015B
DLP5500 0.55 XGA DMD data sheet	DLPS013B



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Figure 1. Typical Application

DLPC200

DLPS014D-APRIL 2010-REVISED MARCH 2012



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Device Marking

Device marking should be as shown below.



Marking Key:

- Line 1: TI Reference Number
- Line 2: Device Name
- Line 3: DLP® logo
- Line 4: Date Code
- Line 5: Country of Origin
- Line 6: Assembly Lot Number
- Line 7: Trace Code



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PROJECTOR IMAGE AND CONTROL PORT SIGNALS

The DLPC200 provides two input ports for graphics and motion video inputs. The signals listed below support the two input interface modes.

Following are the two input image interface modes, signal descriptions, and pins needed on the DLPC200.

- PORT 1, 28 pins (HDMI connector)
 - PORT1_D(23-0) Projector data
 - PORT1_VSYNC Vertical sync
 - PORT1_HSYNC Horizontal sync
 - PORT1_IVALID Data enable
 - PORT1_CLK Projector clock (rising edge or falling edge, to capture input data)
- PORT 2, 28 pins (Expansion connector)
 - PORT2_D(23-0) Projector data
 - PORT2_VSYNC Vertical sync
 - PORT2_HSYNC Horizontal sync
 - PORT2_IVALID Data enable
 - PORT2_CLK Projector clock (rising edge or falling edge, to capture input data)

Two control interfaces, USB and SPI, are provided to configure the DLPC200, as well as to transmit pattern data to memory for structured light mode. Following are the pins needed for the SPI and USB control interfaces.

- USB, 48 MHz
 - USB_CLK USB clock
 - USB_CTRL1 FIFO full flag
 - USB_CTRL2 FIFO empty flag
 - USB_FD(15-0) USB data
 - USB_PA02 FIFO output enable for reads
 - USB_PA04 FIFO address bit
 - USB_PA05 FIFO address bit
 - USB_RDY1 Write enable
 - USB_RDY0 Read enable
- SPI, 5 MHz
 - SLAVE_SPI_CLK SPI clock
 - SLAVE_SPI_ACK Busy signal that holds off additional transactions until the slave has completed processing data
 - SLAVE_SPI_MISO Output from slave
 - SLAVE_SPI_MOSI Output from master
 - SLAVE_SPI_CS Slave select

Images are displayed via control of the DMD and DLPA200. The DLPC200 DMD interface consists of a 200-MHz (nominal) half-bus DDR output-only interface with LVDS signaling. The serial communications port (SCP), 125-kHz nominal, is used to read or write control data to both the DMD and the DLPA200. The following listed signals support data transfer to the DMD and DLPA200.

- DMD, 200 MHz
 - DMD_CLK_AP, DMD_CLK_AN DMD clock for A
 - DMD_CLK_BP, DMD_CLK_BN DMD clock for B
 - DMD_DAT_AP, DMD_DAT_AN(1, 3, 5, 7, 9, 11, 13, 15) Data bus A (odd-numbered pins are used for half-bus)
 - DMD_DAT_BP, DMD_DAT_BN(1, 3, 5, 7, 9, 11, 13, 15) Data bus B (odd-numbered pins are used for half-bus)
 - DMD_SCRTL_AP, DMD_SCRTL_AN S-control for A
 - DMD_SCRTL_BP, DMD_SCRTL_BN S-control for B

DLPC200

DLPS014D - APRIL 2010-REVISED MARCH 2012



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- DLPA200, 125 kHz
 - SCP_DMD_RST_CLK SCP clock
 - SCP_DMD_EN Enable DMD communication
 - SCP_RST_EN Enable DLPA200 communication
 - SCP_DMD_RST_DI Input data
 - SCP_DMD_RST_DO Output data



DLPS014D - APRIL 2010 - REVISED MARCH 2012

DEVICE INFORMATION

The Terminal Functions table describes the input/output characteristics of signals that interface to the DLPC200 by functional groups.

TERMINAL		I/O	CLOCK	DESCRIPTION					
NAME	NO.	TYPE ⁽¹⁾	SYSTEM						
Port 1 Video Data and Control ⁽²⁾									
PORT1_CLK	J2			Pixel clock					
PORT1_VSYNC	N3		PORT1_CLK	Vertical sync; weak pullup applied					
PORT1_HSYNC	P1		PORT1_CLK	Horizontal sync; weak pullup applied					
PORT1_IVALID	P2		PORT1_CLK	Data valid					
PORT1_D0	D2		PORT1_CLK	Pixel data - Blue 0					
PORT1_D1	D3		PORT1_CLK	Pixel data - Blue 1					
PORT1_D2	F5		PORT1_CLK	Pixel data - Blue 2					
PORT1_D3	D1		PORT1_CLK	Pixel data - Blue 3					
PORT1_D4	F3		PORT1_CLK	Pixel data - Blue 4					
PORT1_D5	G4		PORT1_CLK	Pixel data - Blue 5					
PORT1_D6	F1		PORT1_CLK	Pixel data - Blue 6					
PORT1_D7	G3		PORT1_CLK	Pixel data - Blue 7					
PORT1_D8	H5		PORT1_CLK	Pixel data – Green 0					
PORT1_D9	H4		PORT1_CLK	Pixel data – Green 1					
PORT1_D10	G2	13	PORT1_CLK	Pixel data – Green 2					
PORT1_D11	J4		PORT1_CLK	Pixel data – Green 3					
PORT1_D12	H3		PORT1_CLK	Pixel data – Green 4					
PORT1_D13	J3		PORT1_CLK	Pixel data – Green 5					
PORT1_D14	K3		PORT1_CLK	Pixel data – Green 6					
PORT1_D15	L1		PORT1_CLK	Pixel data – Green 7					
PORT1_D16	L3		PORT1_CLK	Pixel data - Red 0					
PORT1_D17	L4		PORT1_CLK	Pixel data - Red 1					
PORT1_D18	M4		PORT1_CLK	Pixel data - Red 2					
PORT1_D19	K1		PORT1_CLK	Pixel data - Red 3					
PORT1_D20	M1		PORT1_CLK	Pixel data - Red 4					
PORT1_D21	K2		PORT1_CLK	Pixel data - Red 5					
PORT1_D22	M2		PORT1_CLK	Pixel data - Red 6					
PORT1_D23	M3		PORT1_CLK	Pixel data - Red 7					
PORT1_HPD	E15	B ₂		HDMI hotplug detect					
PORT1_SYNCDET	J22			HDMI input sync detect					

TERMINAL FUNCTIONS

(1)

See I/O Characteristics for more detail. 24-bit data is mapped according to RGB888 pixel format. See Figure 2. (2)

DLPS014D-APRIL 2010-REVISED MARCH 2012



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TERMINAL FUNCTIONS (continued)

TERMINAL	TERMINAL		CLOCK	DESCRIPTION
NAME	NO.	TYPE ⁽¹⁾	SYSTEM	DESCRIPTION
Port 2 Video Data and	Control ⁽³⁾	1		
PORT2_CLK	Y2			Pixel clock
PORT2_VSYNC	AF2		PORT2_CLK	Vertical sync; weak pullup applied
PORT2_HSYNC	AB6		PORT2_CLK	Horizontal sync; weak pullup applied
PORT2_IVALID	W1		PORT2_CLK	Data valid
PORT2_D0	Y1		PORT2_CLK	Pixel data - Blue 0
PORT2_D1	AE1		PORT2_CLK	Pixel data - Blue 1
PORT2_D2	U2		PORT2_CLK	Pixel data - Blue 2
PORT2_D3	AD12		PORT2_CLK	Pixel data - Blue 3
PORT2_D4	AB1		PORT2_CLK	Pixel data - Blue 4
PORT2_D5	V3		PORT2_CLK	Pixel data - Blue 5
PORT2_D6	U5		PORT2_CLK	Pixel data - Blue 6
PORT2_D7	Т3		PORT2_CLK	Pixel data - Blue 7
PORT2_D8	AD1		PORT2_CLK	Pixel data – Green 0
PORT2_D9	AA3		PORT2_CLK	Pixel data – Green 1
PORT2_D10	R6	11	PORT2_CLK	Pixel data – Green 2
PORT2_D11	W3		PORT2_CLK	Pixel data – Green 3
PORT2_D12	AB5		PORT2_CLK	Pixel data – Green 4
PORT2_D13	AD3		PORT2_CLK	Pixel data – Green 5
PORT2_D14	AD5		PORT2_CLK	Pixel data – Green 6
PORT2_D15	AD4		PORT2_CLK	Pixel data – Green 7
PORT2_D16	AE5		PORT2_CLK	Pixel data - Red 0
PORT2_D17	AC11		PORT2_CLK	Pixel data - Red 1
PORT2_D18	AB8		PORT2_CLK	Pixel data - Red 2
PORT2_D19	AC7		PORT2_CLK	Pixel data - Red 3
PORT2_D20	AG4		PORT2_CLK	Pixel data - Red 4
PORT2_D21	AE4		PORT2_CLK	Pixel data - Red 5
PORT2_D22	AF5	-	PORT2_CLK	Pixel data - Red 6
PORT2_D23	AF3		PORT2_CLK	Pixel data - Red 7
Sync In/Sync Out				·
PORT1_Trig_in	F2	l ₃	PORT1_CLK	Alternate sync for port 1. Treated as Vsync; weak pullup applied
PORT1_Sync_out	H6	O ₃	Async	Reserved for future use
PORT2_Trig_in	AB7	l ₁	PORT2_CLK	Alternate sync for port 2. Treated as vsync; weak pullup applied
PORT2_Sync_out	Y3	O ₁	Async	Reserved for future use

(3) 24-bit data is mapped according to RGB888 pixel format. See Figure 2.



DLPS014D - APRIL 2010-REVISED MARCH 2012

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TERMINAL	TERMINAL		CLOCK	DECODIDITION			
NAME	NO.	TYPE ⁽¹⁾	SYSTEM	DESCRIPTION			
Control Interfaces (I ² C, USB, SPI)							
USB_CLK	B15	l ₃		USB clock input (48 MHz), feeds a PLL			
USB_CTRL0	B17	l ₃	USB_CLK	USB I/F FIFO programmable level			
USB_CTRL1	A26	l ₃	USB_CLK	USB I/F FIFO-full flag			
USB_CTRL2	D22	I ₃	USB_CLK	USB I/F FIFO-empty flag			
USB_CTRL3	C19	I ₃	USB_CLK	Reserved for future use			
USB_CTRL4	D16	l ₃	USB_CLK	Reserved for future use			
USB_CTRL5	G17	I ₃	USB_CLK	Reserved for future use			
USB_FD0	G16						
USB_FD1	C26						
USB_FD2	F17						
USB_FD3	C22						
USB_FD4	E18						
USB_FD5	B18						
USB_FD6	F18						
USB_FD7	E19	B.		LISP interface data hus			
USB_FD8	B23	D ₂	USB_OLK				
USB_FD9	D25						
USB_FD10	C21						
USB_FD11	D24						
USB_FD12	B19						
USB_FD13	E25						
USB_FD14	G18						
USB_FD15	C15						
USB_PA02	D23	O ₃	USB_CLK	USB I/F FIFO output enable for reads			
USB_PA04	G15	O ₃	USB_CLK	USB I/F FIFO address(0)			
USB_PA05	A22	O ₃	USB_CLK	USB I/F FIFO address(1)			
USB_PA06	A25	O ₃	USB_CLK	USB I/F FIFO packet end trigger			
USB_RDY0	C16	O ₃	USB_CLK	USB I/F FIFO read enable			
USB_RDY1	C17	O ₃	USB_CLK	USB I/F FIFO write enable			
USB_RDY2	B26	O ₃	USB_CLK	Reserved for future use			
USB_RSVD_14	A15	l ₃	USB_CLK	Reserved for future use			
I2C_SCL	C25	B ₂		Master I ² C clock - 400-kHz. Requires external pullup			
I2C_SDA	D18	B ₂	I2C_SCL	Master I ² C data - 400-kHz. Requires external pullup			
EDID_I2C_SCL	F8	B ₂		HDMI EDID I ² C clock. 400-kHz. Requires external pullup			
EDID_I2C_SDA	D6	B ₂	EDID_I2C_SCL	HDMI EDID I ² C data. 400-kHz. Requires external pullup			
SLAVE_SPI_CLK	B14	l ₃		Slave SPI clock			
SLAVE_SPI_CS	C14	l ₃	SLAVE_SPI_CLK	Slave SPI chip select; weak pullup applied			
SLAVE_SPI_MISO	D14	O ₃	SLAVE_SPI_CLK	Slave SPI data OUT			
SLAVE_SPI_MOSI	E14	l ₃	SLAVE_SPI_CLK	Slave SPI data IN; weak pullup applied			
SLAVE_SPI_SOP	F21	l ₃	SLAVE_SPI_CLK	Reserved for future use			
SLAVE_SPI_ACK	D20	O ₃	SLAVE_SPI_CLK	Slave SPI data busy			



TERMINAL		I/O CLOCK	DESCRIPTION					
NAME	NO.	TYPE ⁽¹⁾	SYSTEM	DESCRIPTION				
DMD Interface								
DMD_DAT_AP1	AB27	O ₄						
DMD_DAT_AN1	AB28	O ₄						
DMD_DAT_AP3	Y25	O ₄						
DMD_DAT_AN3	Y26	O ₄						
DMD_DAT_AP5	W25	O ₄						
DMD_DAT_AN5	W26	O ₄						
DMD_DAT_AP7	W28	O ₄						
DMD_DAT_AN7	W27	O ₄	DMD DCLK AP.					
DMD_DAT_AP9	V27	O ₄	DMD_DCLK_AN	DMD data pins. LVDS pins for data bus A				
DMD_DAT_AN9	V28	O ₄						
DMD DAT AP11	V25	O ₄						
DMD DAT AN11	V26	O ₄						
DMD DAT AP13	V23	O ₄						
DMD DAT AN13	V24	O ₄						
DMD DAT AP15	T26	04						
DMD_DAT_AN15	U27	04						
	T25	04		DMD data clock. I VDS clk for data bus A				
DMD_DCLK_AN	U28	04		DMD data clock. I VDS clk for data bus A				
DMD SCTRL AP	R25	04						
DMD SCTRL AN	R26	0	DMD_DCLK_AN	DMD data serial-control signal bus A (LVDS)				
DMD DAT BP1	AC24	O ₄						
DMD DAT BN1	AC25	04						
DMD DAT BP3	AC26	O ₄						
DMD DAT BN3	AD26	O ₄						
DMD_DAT_BP5	AE27	O ₄						
DMD_DAT_BN5	AE28	0 ₄						
DMD_DAT_BP7	AD27	O ₄						
DMD_DAT_BN7	AD28	O ₄						
DMD_DAT_BP9	Y23	O ₄	DMD_DCLK_BN	DMD data pins. LVDS pins for data bus B				
DMD_DAT_BN9	Y24	0 ₄						
DMD_DAT_BP11	AC27	O ₄						
DMD_DAT_BN11	AC28	0 ₄						
DMD_DAT_BP13	AB25	O ₄						
DMD_DAT_BN13	AB26	O ₄						
DMD_DAT_BP15	AA25	O ₄						
DMD_DAT_BN15	AA26	O ₄						
DMD_DCLK_BP	U25	O ₄						
DMD_DCLK_BN	U26	O ₄		DMD data clock. LVDS clk for data bus B				
DMD_SCTRL_BP	T21	O ₄						
DMD_SCTRL_BN	T22	O ₄	DMD_DCLK_AN	DMD data serial-control signal bus B (LVDS)				
DMD_PWRDN	P26	0 ₃	ASYNC	DMD power down (active-low)				
RST_IRQ	M25	l ₃	ASYNC	DLPA200 interrupt (active-low)				
RST_OE	M28	O ₃	ASYNC	DLPA200 output enable				
RST_RST	H24	O ₃	ASYNC	DLPA200 reset				
RST_STROBE	G28	O ₃		DLPA200 strobe				



DLPS014D - APRIL 2010-REVISED MARCH 2012

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TERMINAL		I/O	CLOCK	DECODIDITION
NAME	NO.	TYPE ⁽¹⁾	SYSTEM	DESCRIPTION
DMD Interface (Continu	ued)			
RST_SEL0	G27	0	DET STROPE	DL DA 200 voltage coloct
RST_SEL1	G26	O_3	KOT_OTROBE	DEFA200 Voltage select
RST_MODE0	L24	0	DET ETDODE	DL DA 200 mode coloct
RST_MODE1	L23	O_3	KSI_SIKUBE	DEPA200 mode select
RST_A0	K25			
RST_A1	J26	0		DL DA 200 oddroso
RST_A2	J25	03	KOT_OTROBE	DEFA200 address
RST_A3	K26			
SCP_DMD_RST_DO	G25	O ₃	SCP_DMD_RST_CLK	SCP data out (write data)
SCP_DMD_RST_DI	H26	l ₃	SCP_DMD_RST_CLK	SCP data in (read data)
SCP_DMD_EN	L25	O ₃	SCP_DMD_RST_CLK	DMD SCP chip select
SCP_RST_EN	H23	O ₃	SCP_DMD_RST_CLK	DLPA200 SCP chip select
SCP_DMD_RST_CLK	H25	O ₃		DMD/DLPA200 SCP clock, 125 kHz
Static RAM Interface				
FLASH_CE	D12	O ₃	ASYNC	Flash chip enable
FLASH_SRAM_A0	D13			
FLASH_SRAM_A1	A11			
FLASH_SRAM_A2	C11			
FLASH_SRAM_A3	D11			
FLASH_SRAM_A4	A12			
FLASH_SRAM_A5	B12			
FLASH_SRAM_A6	D10			
FLASH_SRAM_A7	A10			
FLASH_SRAM_A8	B10			
FLASH_SRAM_A9	B8			
FLASH_SRAM_A10	C8			
FLASH_SRAM_A11	A7			
FLASH_SRAM_A12	B7			
FLASH_SRAM_A13	A4	O ₃	FLASH_SRAM_WE	Flash/SRAM address
FLASH_SRAM_A14	D7			
FLASH_SRAM_A15	C6			
FLASH_SRAM_A16	D8			
FLASH_SRAM_A17	B6			
FLASH_SRAM_A18	C7			
FLASH_SRAM_A19	A8			
FLASH_SRAM_A20	C4	1		
FLASH_SRAM_A21	B3			
FLASH_SRAM_A22	A3	1		
FLASH_SRAM_A23	C5	1		
FLASH_SRAM_A24	D5	1		
FLASH_SRAM_A25	B4	1		
FLASH_SRAM_A26	D4			

DLPS014D-APRIL 2010-REVISED MARCH 2012



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TERMINAL		I/O TYPE ⁽¹⁾	CLOCK	DESCRIPTION				
NAME	NO.		SYSTEM	DESCRIPTION				
Static RAM Interface (Continued)								
FLASH_SRAM_D0	E11							
FLASH_SRAM_D1	F10							
FLASH_SRAM_D2	E10							
FLASH_SRAM_D3	G9							
FLASH_SRAM_D4	E8							
FLASH_SRAM_D5	E7							
FLASH_SRAM_D6	E5							
FLASH_SRAM_D7	E4	Р		Elech/CRAM doto				
FLASH_SRAM_D8	F11	D ₂	FLASH_SKAW_WE	Flash/SRAW Uala				
FLASH_SRAM_D9	E12							
FLASH_SRAM_D10	F12							
FLASH_SRAM_D11	G12							
FLASH_SRAM_D12	G13							
FLASH_SRAM_D13	H13							
FLASH_SRAM_D14	F14							
FLASH_SRAM_D15	G14							
FLASH_SRAM_OE	C10	O ₃		Flash output enable				
FLASH_SRAM_RDY	C13	l ₃		Flash wait				
FLASH_SRAM_RST	C12	O ₃		Flash reset				
FLASH_SRAM_WE	A6	O ₃		Flash write enable				
SRAM_CE	B11	O ₃		SRAM chip enable				
SRAM_LB	D9	O ₃		SRAM lower byte enable				
SRAM_UB	C9	O ₃		SRAM upper byte enable				
SDRAM Interface								
MEM_CLK_P0	R2	O ₅		DDR2 memory, differential memory clock				
MEM_CLK_N0	R1	O ₅		DDR2 memory, differential memory clock				
MEM_CLK_P1	U3	O ₅		DDR2 memory, differential memory clock				
MEM_CLK_N1	U4	O ₅		DDR2 memory, differential memory clock				
MEM_CLK_P2	AC5	O ₅		DDR2 memory, differential memory clock				
MEM_CLK_N2	AC4	O ₅		DDR2 memory, differential memory clock				
MEM_CLK_P3	AE14	O ₅		DDR2 memory, differential memory clock				
MEM_CLK_N3	AF14	O ₅		DDR2 memory, differential memory clock				
MEM_CKE0	AF12	O ₅						
MEM_BA0	Y19	O ₅	MEM_CLK					
MEM_BA1	AD21	O ₅	MEM_CLK					
MEM_BA2	AE7	O ₅	MEM_CLK					



DLPS014D - APRIL 2010 - REVISED MARCH 2012

TERMINAL		I/O	CLOCK	DESCRIPTION					
NAME	NO.	TYPE ⁽¹⁾	SYSTEM	DESCRIPTION					
SDRAM Interface (Cont	SDRAM Interface (Continued)								
MEM_A0	AD24	_							
MEM_A1	AF21								
MEM_A2	AG23								
MEM_A3	AE8								
MEM_A4	AG12								
MEM_A5	AF23								
MEM_A6	AC17			DDP2 momenty multiplexed row and column address. The momenty					
MEM_A7	AA16	0		in the kit is 512 Mbit in ×16 mode, 8 Meg × 16 bits × 4 banks. Only					
MEM_A8	AE23	O_5		A(12:0) and BA(1:0) are currently used. A(15:13) and BA(2) are					
MEM_A9	AE22			reserved for future use (RFO).					
MEM_A10	AE16								
MEM_A11	AD25								
MEM_A12	AF19								
MEM_A13	AH10								
MEM_A14	AA8	1							
MEM_A15	AD11								
MEM_CAS	AG19	O ₅	MEM_CLK	Column address strobe. Active-low					
MEM_RAS	AE20	O ₅	MEM_CLK	Row address strobe. Active-low					
MEM_CS0	AF13	O ₅	MEM_CLK	Chip select. Active-low					
MEM_WE	AG25	O ₅	MEM_CLK	Write enable. Active-low					
MEM_ODT	AH12	O ₅	MEM_CLK						
MEM_DM0	W2	O ₅	MEM_CLK						
MEM_DM1	AE2	O ₅	MEM_CLK						
MEM_DM2	AH6	O ₅	MEM_CLK						
MEM_DM3	AF7	O ₅	MEM_CLK						
MEM_DM4	AE13	O ₅	MEM_CLK						
MEM_DM5	AH18	O ₅	MEM_CLK						
MEM_DM6	AF24	O ₅	MEM_CLK						
MEM_DM7	AG26	O ₅	MEM_CLK						
MEM_DS0	AB2	B ₁	MEM_CLK_P0						
MEM_DS1	AE3	B ₁	MEM_CLK_N0						
MEM_DS2	AD7	B ₁	MEM_CLK_P1						
MEM_DS3	AE10	B ₁	MEM_CLK_N1						
MEM_DS4	AF11	B ₁	MEM_CLK_P2						
MEM_DS5	AF17	B ₁	MEM_CLK_N2						
MEM_DS6	AE18	B ₁	MEM_CLK_P3						
MEM_DS7	AF26	B ₁	MEM_CLK_N3						



TERMINAL		I/O	CLOCK	DESCRIPTION
NAME	NO.	TYPE ⁽¹⁾	SYSTEM	DESCRIPTION
SDRAM Interface (Cont	tinued)			
MEM_D0	R3	B ₁		
MEM_D1	R4	B ₁		
MEM_D2	T4	B ₁		
MEM_D3	R5	B ₁		
MEM_D4	U1	B ₁		
MEM_D5	V4	B ₁		
MEM_D6	V2	B ₁		
MEM_D7	V1	B ₁		
MEM_D8	U6	B ₁	MEM_DS0, MEM_DS1	
MEM_D9	Y4	B ₁		
MEM_D10	AC2	B ₁		
MEM_D11	AC1	B ₁		
MEM_D12	AC3	B ₁		
MEM_D13	AD2	B ₁		
MEM_D14	AB3	B ₁		
MEM_D15	AA4	B ₁		
MEM_D16	AE6	B ₁		
MEM_D17	AF4	B ₁		
MEM_D18	AG3	B ₁		
MEM_D19	AH3	B ₁		
MEM_D20	AF6	B ₁		
MEM_D21	AH4	B ₁		
MEM_D22	AD8	B ₁		
MEM_D23	AG6	B ₁		
MEM_D24	AB9	B ₁	MEM_DS2, MEM_DS3	
MEM_D25	AD10	B ₁		
MEM_D26	AG7	B ₁		
MEM_D27	AH7	B ₁		
MEM_D28	AC8	B ₁		
MEM_D29	AA10	B ₁		
MEM_D30	AG8	B ₁		
MEM_D31	AH8	B ₁		



DLPS014D - APRIL 2010 - REVISED MARCH 2012

TERMINAL		I/O	CLOCK	DESCRIPTION
NAME	NO.	TYPE ⁽¹⁾	SYSTEM	DESCRIPTION
SDRAM Interface (Cont	inued)			
MEM_D32	AF8	B ₁		
MEM_D33	AE9	B ₁		
MEM_D34	AF10	B ₁		
MEM_D35	AG10	B ₁		
MEM_D36	AE12	B ₁		
MEM_D37	AE11	B ₁		
MEM_D38	AG11	B ₁		
MEM_D39	AH11	B ₁		
MEM_D40	AC15	B ₁	MEM_DS4, MEM_DS5	
MEM D41	AF15	B₁	-	
MEM D42	AG17	B ₁	-	
 MEM_D43	AH17	B₁		
MEM D44	AF16	B₁		
MEM_D45	AB16	I B₁		
MEM_D46	AF17	B₄		
MFM_D47	AG18	B ₄		
MEM_D48	AH19	B ₁		
MEM_D49	AD17	B		
MEM_D50	AG21	B		
MEM_D01	AH21	B ₄		
MEM_D52	AG22	B ₄		
MEM_D02	AH22	B ₄		
MEM_D64	AH23	B ₄		
MEM_D55	AF19	B		
MEM_D56	AE25	B	MEM_DS6, MEM_DS7	
MEM_D57	AF20	 B₁		
MEM_D58	AD18	B1		
MEM D59	AE21	B ₁		
MEM D60	AE25	B₁		
MEM D61	AH25	B₁		
MEM D62	AF22	B1		
MEM D63	AE24	 B₁		
LED Driver Interface				
PWM0	C27	03	Async	PWM signal used to control the LED current
PWM1	D28	03	Async	PWM signal used to control the LED current
PWM2	D27	03	Async	PWM signal used to control the LED current
PWM3	D26	0 ₃	Async	PWM signal used to control the LED current
LED_IR_EN	E28	O ₃	Async	IR LED enable strobe. Controlled by programmable DMD sequence timing (active-high)
LED_RED_EN	F28	O ₃	Async	RED LED enable strobe. Controlled by programmable DMD sequence timing (active-high)
LED_GRN_EN	E27	O ₃	Async	Green LED enable strobe. Controlled by programmable DMD sequence timing (active-high)
LED_BLU_EN	F27	O ₃	Async	Blue LED enable strobe. Controlled by programmable DMD sequence timing (active-high)
LED_SUBFRAME	E26	O ₃	Async	Subframe signal used by LED driver. Controlled by programmable DMD sequence timing (active-high)

TEXAS INSTRUMENTS

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TERMINAL		I/O	CLOCK	DECODIDITION				
NAME	NO.	TYPE ⁽¹⁾	SYSTEM	DESCRIPTION				
LED Driver Interface (C	ontinued)						
SYNC_0	F26	O ₃	Async	Extra strobe. Controlled by programmable DMD sequence timing (active-high)				
SYNC_1	F25	O ₃	Async	Extra strobe. Controlled by programmable DMD sequence timing (active-high)				
SYNC_2	F24	O ₃	Async	Extra strobe. Controlled by programmable DMD sequence timing (active-high)				
LED_EN	L28	O ₃	Async	LED driver enable. Active-low output control to external LED drive logic				
LED_SYNC	M21	O ₃	Async	Reserved for future use; weak pullup applied				
LED_SYNCEN	C24	O ₃	Async	Inverted LED_LIT signal				
LED_LIT	J28	l ₃	Async	LED driver status				
LED_SENS	K27	l ₃	Async	Reserved for future use				
LED_SPI_CLK	N26	O ₃	Async	LED SPI master clock				
LED_SPI_CS	M26	O ₃	LED_SPI_CLK	LED SPI master chip select				
LED_SPI_DIR	P25	O ₃	LED_SPI_CLK	LED SPI master driver direction				
LED_SPI_MISO	L27	I ₃	LED_SPI_CLK	LED SPI master data IN				
LED_SPI_MOSI	L26	O ₃	LED_SPI_CLK	LED SPI master data OUT; weak pullup applied				
System Interfaces								
CFG_CSO	E2	O ₃	CFG_DCLK	Chip-select output for an external serial configuration device. Active-low				
CFG_CLK	P3	O ₃	CFG_DCLK	Configuration serial EPROM data clock				
CFG_ASDI	N7	l ₃	CFG_DCLK	Data input from an external serial configuration device. Provides configuration data for the device				
CFG_ASDO	F4	O ₃	CFG_DCLK	Serial data output. This pin sends address and control information to the external PROM during configuration.				
CFG_STATUS	M6	O ₃	CFG_DCLK	Configuration status pin				
CFG_DONE	P24	O ₃	CFG_DCLK	Configuration-done status pin. Signal goes high at the end of configuration.				
CFG_MSEL0	N22							
CFG_MSEL1	P23		A					
CFG_MSEL2	M22	13	Async	Configuration-mode selection signals				
CFG_MSEL3	P22							
CFG_CE	R8	l ₃	Async	Chip enable. Active-low				
CFG_EN	P4	l ₃	Async	Configuration control. Configuration starts when a low-to-high transition is detected at this pin.				
CFG_CEO	P28	O ₃	Async					
REF_CLK	J27	I ₃		50-MHz reference clock, 3.3 V				
RESET	A14	I ₃	Async	Device reset (active-low)				
PWR_GOOD	A23	I ₃	Async	System power-good indicator				
Reserved								
RSVD_H10	N4	B ₂		GPIO				
RSVD_H11	L2	B ₂		GPIO				
RSVD_H12	K4	B ₂		GPIO				
RSVD_H6	G1	B ₂		GPIO				
RSVD_H5	G5	B ₂		GPIO				
RSVD_H4	G6	B ₂		GPIO				
RSVD_H2	E1	B ₂		GPIO				
RSVD_H1	C2	B ₂		GPIO				



DLPS014D - APRIL 2010 - REVISED MARCH 2012

NAME NO. TYPE ⁽¹⁾ SYSTEM DESCRIPTION Reserved (Continued) E22 RSVD_171 D21 A21 RSVD_173 C16 C RSVD_173 C16 C RSVD_174 B22 L RSVD_175 D17 L	TERMINAL		I/O	CLOCK	DESCRIPTION					
Reserved (Continued) E22 Image: Continued of the context of the conte	NAME	NO.	TYPE ⁽¹⁾	SYSTEM	DESCRIPTION					
RSVD_T0 E22 Image: Constraint of the constraint of theconstraint of the constraint of theconstraint of theconstraint	Reserved (Continued)	1								
RSVD_T1 D21 RSVD_T2 A21 RSVD_T3 C18 RSVD_T4 B22 RSVD_T5 B21 RSVD_T6 D17 RSVD_T6 D17 RSVD_T6 D17 RSVD_T6 D17 RSVD_T0 K21 RSVD_T0 M24 RSVD_D1 D15 O3 Reserved for future use, do not connect RSVD_D3 F15 O3 Reserved for future use, do not connect RSVD_H4 E3 F3 Reserved for future use, can be left open, recommend grounding. RSVD_H3 E3 F3 Reserved for future use, can be left open, recommend grounding. RSVD_H4 L5 F3 Reserved for future use, can be left open, recommend grounding. RSVD_H3 J1 F3 Reserved for future use, can be left open, recommend grounding. RSVD_P1 P6 O2 Reserved for future use, do not connect RSVD_P3 RSVD_P3 P5 I4	RSVD_T0	E22								
RSVD_T2 A21 A21 RSVD_T3 C18 C18 RSVD_T5 B21 C18 RSVD_T5 B21 C18 RSVD_T6 D17 C18 RSVD_T6 D17 C18 RSVD_T6 D17 C18 RSVD_T0 M24 C RSVD_T0 M24 C RSVD_T1 D15 O.3 Reserved for future use, do not connect RSVD_D2 E17 Is Reserved for future use, do not connect RSVD_D3 F15 O.3 Reserved for future use, do not connect RSVD_H8 E3 Is Reserved for future use, can be left open, recommend grounding. RSVD_H8 L5 Is Reserved for future use, can be left open, recommend grounding. RSVD_P14 M5 Is Reserved for future use, can be left open, recommend grounding. RSVD_P2 P8 Is Reserved for future use, can be left open, recommend grounding. RSVD_P3 P6 O_2 Reserved for future use, can be left open, recommend grounding. <t< td=""><td>RSVD_T1</td><td>D21</td><td></td><td></td><td></td></t<>	RSVD_T1	D21								
RSVD_T3 C18 C18 RSVD_T4 B22 Image: Construction of the construction of theconstruction of the construction of theconstruction of theconstru	RSVD T2	A21								
RSVD_T4 B22 Image: Control of the contr	RSVD T3	C18								
RSVD_T5 B21 Image: Constraint of the second	RSVD T4	B22			These I/Os can be left open/ unconnected for normal operation.					
RSVD_T6 D17 L RSVD_T7 E21 L RSVD_TC M24 L RSVD_D1 D15 O ₃ Reserved for future use, do not connect RSVD_D2 E17 I ₃ Reserved for future use, do not connect RSVD_D3 F15 O ₃ Reserved for future use, do not connect RSVD_H3 E3 I ₃ Reserved for future use, can be left open, recommend grounding. RSVD_H4 E3 I ₃ Reserved for future use, can be left open, recommend grounding. RSVD_H4 L5 I ₃ Reserved for future use, can be left open, recommend grounding. RSVD_H4 L5 I ₃ Reserved for future use, can be left open, recommend grounding. RSVD_P13 J1 I ₅ Reserved for future use, do not connect RSVD_P2 P8 I ₄ Reserved for future use, do not connect RSVD_P3 P5 I ₄ Reserved for future use, do not connect RSVD_G1 F19 O ₃ Reserved for future use, do not connect RSVD_G2 M27 O ₃ Reserved for future use, do n	RSVD T5	B21								
RSVD_TC P21 P21 RSVD_TC M24 P21 RSVD_DC M24 P21 RSVD_DD A17 Is Reserved for future use, do not connect RSVD_DD D15 Os Reserved for future use, do not connect RSVD_D2 E17 Is Reserved for future use, do not connect RSVD_D3 F15 Os Reserved for future use, do not connect RSVD_H4 E3 Is Reserved for future use, can be left open, recommend grounding. RSVD_H8 L5 Is Reserved for future use, can be left open, recommend grounding. RSVD_H13 J1 Is Reserved for future use, can be left open, recommend grounding. RSVD_P1 P6 Os Reserved for future use, do not connect RSVD_P2 P8 Is Reserved for future use, do not connect RSVD_P3 P5 Is Reserved for future use, do not connect RSVD_G3 N21 Os Reserved for future use, do not connect RSVD_G4 F19 Os Reserved for future use, do not connect	RSVD_T6	D17								
InstructInstructRSVD_TCM24RSVD_D0A17IsRSVD_D1D16O3Reserved for future use, do not connectRSVD_D2F17IsReserved for future use, do not connectRSVD_D3F15O3Reserved for future use, do not connectRSVD_H3E3IsReserved for future use, can be left open, recommend grounding.RSVD_H4L5IsReserved for future use, can be left open, recommend grounding.RSVD_H9M5IsReserved for future use, can be left open, recommend grounding.RSVD_P14P7IsReserved for future use, can be left open, recommend grounding.RSVD_P19M5IsReserved for future use, can be left open, recommend grounding.RSVD_P11P6O2Reserved for future use, do not connectRSVD_P2P7IsReserved for future use, do not connectRSVD_P3P5IsReserved for future use, do not connectRSVD_C4P27O3Reserved for future use, do not connectRSVD_G3N21O3Reserved for future use, do not connectRSVD_G4P27O4Reserved for future use, do not connectRSVD_C5A18O3Reserved for future use, do not connectRSVD_G5A18O3Reserved for future use, do not connectRSVD_G5A18O3Reserved for future use, do not connectRSVD_G5A18O3Reserved for future use, do not connectRSVD_S2A614Unused input only, can be left	RSVD T7	F21								
NULL_12InterNullRSVD_D0A171gReserved for future use, do not connectRSVD_D1D15O_3Reserved for future use, do not connectRSVD_D2E171gReserved for future use, do not connectRSVD_D3F15O_3Reserved for future use, do not connectRSVD_H3E31gReserved for future use, do not connectRSVD_H4E31gReserved for future use, can be left open, recommend grounding.RSVD_H7H71gReserved for future use, can be left open, recommend grounding.RSVD_H9M51gReserved for future use, can be left open, recommend grounding.RSVD_H9M51gReserved for future use, can be left open, recommend grounding.RSVD_P1P6O_2Reserved for future use, do not connectRSVD_P2P81gReserved for future use, do not connectRSVD_P3P51gReserved for future use, do not connectRSVD_G3N21O_3Reserved for future use, do not connectRSVD_G4F19O_3Reserved for future use, do not connectRSVD_G5A18O_3Reserved for future use, do not connectRSVD_G6A19O_3Reserved for future use, do not connectRSVD_G5A18O_3Reserved for future use, do not connectRSVD_G6A19O_3Reserved for future use, do not connectRSVD_S1AG15Unused input only, can be left open, recommend grounding.RSVD_S2AG15Unused input only, c	RSVD TC	M24								
RSVD_D1 D15 O ₃ Reserved for future use, do not connect RSVD_D2 E17 I ₃ Reserved for future use, do not connect RSVD_D3 F15 O ₃ Reserved for future use, do not connect RSVD_H3 E33 I ₃ Reserved for future use, can be left open, recommend grounding. RSVD_H4 E3 I ₃ Reserved for future use, can be left open, recommend grounding. RSVD_H4 L5 I ₃ Reserved for future use, can be left open, recommend grounding. RSVD_H4 L5 I ₃ Reserved for future use, can be left open, recommend grounding. RSVD_H9 M5 I ₃ Reserved for future use, can be left open, recommend grounding. RSVD_P1 P6 O ₂ Reserved for future use, do not connect RSVD_P3 P5 I ₄ Reserved for future use, do not connect RSVD_C60 C23 O ₃ Reserved for future use, do not connect RSVD_C3 M27 O ₃ Reserved for future use, do not connect RSVD_G3 N21 O ₃ Reserved for future use, do not connect RSVD_G4 P27 O ₃ Reserved for future use, do not connect	RSVD_D0	A17	la la		Reserved for future use do not connect					
INDEL_D1D13D33Indervoid on future use, do not connectRSVD_D2E17IIReserved for future use, do not connectRSVD_D3F15O3Reserved for future use, do not connectRSVD_H3E3IIReserved for future use, can be left open, recommend grounding.RSVD_H4L5IReserved for future use, can be left open, recommend grounding.RSVD_H4L5IReserved for future use, can be left open, recommend grounding.RSVD_H9M5IReserved for future use, can be left open, recommend grounding.RSVD_P1P7IReserved for future use, do not connectRSVD_P2P8IReserved for future use, do not connectRSVD_P2P8IReserved for future use, do not connectRSVD_C3C23O3Reserved for future use, do not connectRSVD_C4P27P3IReserved for future use, do not connectRSVD_C5M27O3Reserved for future use, do not connectRSVD_C64P27O3Reserved for future use, do not connectRSVD_C65A18O3Reserved for future use, do not connectRSVD_C66A19O3Reserved for future use, do not connectRSVD_C65A18O3Reserved for future use, do not connectRSVD_C66A19O3Reserved for future use, do not connectRSVD_C66A18O3Reserved for future use, do not connectRSVD_S1AG16Unused input only, can be left open, recommend grounding.<	RSVD_D1	D15	-13 Oc		Reserved for future use, do not connect					
RSVD_D3F15O3Reserved for future use, do not connectRSVD_D4E3I3Reserved for future use, can be left open, recommend grounding.RSVD_H7H7I4I3Reserved for future use, can be left open, recommend grounding.RSVD_H8L5I3Reserved for future use, can be left open, recommend grounding.RSVD_H9M5I3Reserved for future use, can be left open, recommend grounding.RSVD_P10P7I4Reserved for future use, can be left open, recommend grounding.RSVD_P20P7I4Reserved for future use, do not connectRSVD_P2P8I4Reserved for future use, do not connectRSVD_P3P5I4Reserved for future use, do not connectRSVD_00C23O3Reserved for future use, do not connectRSVD_01F19O3Reserved for future use, do not connectRSVD_02M27O3Reserved for future use, do not connectRSVD_G4P27O3Reserved for future use, do not connectRSVD_64P27O3Reserved for future use, do not connectRSVD_S2A615Unused input only, can be left open, recommend grounding.RSVD_S2A616Unused input only, can be left open, recommend grounding.RSVD_S2A615Unused input only, can be left open, recommend grounding.RSVD_S2A616Unused input only, can be left open, recommend grounding.RSVD_S2A615Unused input only, can be left open, recommend grounding.RSVD_S2A614Unused input		E17	U3		Reserved for future use, do not connect					
RSVD_D3P13O3Reserved for future use, can be left open, recommend grounding.RSVD_H3E3I3Reserved for future use, can be left open, recommend grounding.RSVD_H8L5I3Reserved for future use, can be left open, recommend grounding.RSVD_H13J1I3Reserved for future use, can be left open, recommend grounding.RSVD_H13J1I4Reserved for future use, can be left open, recommend grounding.RSVD_P10P7I4Reserved for future use, can be left open, recommend grounding.RSVD_P11P6O2Reserved for future use, do not connectRSVD_P12P8I4Reserved for future use, do not connectRSVD_P3P5I4Reserved for future use, do not connectRSVD_G0C23O3Reserved for future use, do not connectRSVD_G1F19O3Reserved for future use, do not connectRSVD_G2M27O3Reserved for future use, do not connectRSVD_G4P27O3Reserved for future use, do not connectRSVD_G5A18O3Reserved for future use, do not connectRSVD_S2A614Unused input only, can be left open, recommend grounding.RSVD_S2A615Unused input only, can be left open, recommend grounding.RSVD_S2A615Unused input only, can be left open, recommend grounding.RSVD_S2Y27Unused input only, can be left open, recommend grounding.RSVD_S2Y27Unused input only, can be left open, recommend grounding.RSVD_S2Y28 <td< td=""><td></td><td>E17</td><td>13</td><td></td><td>Reserved for future use, do not connect</td></td<>		E17	13		Reserved for future use, do not connect					
RSVD_H7H7H3Reserved for future use, can be left open, recommend grounding.RSVD_H8L5H3Reserved for future use, can be left open, recommend grounding.RSVD_H9M5H3Reserved for future use, can be left open, recommend grounding.RSVD_H9M5H3Reserved for future use, can be left open, recommend grounding.RSVD_H13J1H3Reserved for future use, can be left open, recommend grounding.RSVD_P1P6O2Reserved for future use, dan be to connectRSVD_P2P8H4Reserved for future use, do not connectRSVD_P3P5H4Reserved for future use, do not connectRSVD_G0C23O3Reserved for future use, do not connectRSVD_G1F19O3Reserved for future use, do not connectRSVD_G2M27O3Reserved for future use, do not connectRSVD_G3N21O3Reserved for future use, do not connectRSVD_G5A18O3Reserved for future use, do not connectRSVD_S1AG14Unused input only, can be left open, recommend grounding.RSVD_S2AG15Unused input only, can be left open, recommend grounding.RSVD_S2Y27Unused input only, can be left open, recommend grounding.RSVD_S2Y27Unused input only, can be left open, recommend grounding.RSVD_S2Y27Unused input only, can be left open, recommend grounding.RSVD_S2Y28Unused input only, can be left open, recommend grounding.RSVD_S2Y28Unused input only,		F10 F2	03		Reserved for future use, do not connect					
RSVD_H8L5IsReserved for future use, can be left open, recommend grounding.RSVD_H9M5IsReserved for future use, can be left open, recommend grounding.RSVD_H13J1IsReserved for future use, can be left open, recommend grounding.RSVD_P0P7IsReserved for future use, can be left open, recommend grounding.RSVD_P1P6O2Reserved for future use, do not connectRSVD_P2P8IsReserved for future use, do not connectRSVD_P3P5IsReserved for future use, do not connectRSVD_G6C23O3Reserved for future use, do not connectRSVD_G2M27O3Reserved for future use, do not connectRSVD_G2M27O3Reserved for future use, do not connectRSVD_G4P27O3Reserved for future use, do not connectRSVD_G5A18O3Reserved for future use, do not connectRSVD_G6A19O3Reserved for future use, do not connectRSVD_S2AG14Unused input only, can be left open, recommend grounding.RSVD_S2AG15Unused input only, can be left open, recommend grounding.RSVD_S2AG15Unused input only, can be left open, recommend grounding.RSVD_S2Y27Unused input only, can be left open, recommend grounding.RSVD_S0AA24Reserved for future use, do not connectRSVD_S0AA24Reserved for future use, do not connectRSVD_S0AA24Reserved for future use, do not connectRSVD_S1Af1		ES	13		Reserved for future use, can be left open, recommend grounding.					
RSVD_HB L5 I3 Reserved for future use, can be left open, recommend grounding. RSVD_H13 J1 I3 Reserved for future use, can be left open, recommend grounding. RSVD_P10 P7 I4 Reserved for future use, do not connect RSVD_P11 P6 O2 Reserved for future use, do not connect RSVD_P2 P8 I4 Reserved for future use, do not connect RSVD_G0 C23 O3 Reserved for future use, do not connect RSVD_G1 F19 O3 Reserved for future use, do not connect RSVD_G2 M27 O3 Reserved for future use, do not connect RSVD_G2 M27 O3 Reserved for future use, do not connect RSVD_G4 P27 O3 Reserved for future use, do not connect RSVD_G5 A18 O3 Reserved for future use, do not connect RSVD_G6 A19 O3 Reserved for future use, do not connect RSVD_S1 AG14 Unused input only, can be left open, recommend grounding. RSVD_S2 AG15 Unused input only, can be left open, recommend grounding. RSVD_S3 AH14 Unused input only, can be left open, recommend g	RSVD_H7	H/	I ₃		Reserved for future use, can be left open, recommend grounding.					
RSVD_H9 Mb Is Reserved for future use, can be left open, recommend grounding. RSVD_P0 P7 I4 Reserved for future use, can be left open, recommend grounding. RSVD_P0 P7 I4 Reserved for future use, do not connect RSVD_P2 P8 I4 Reserved for future use, do not connect RSVD_P3 P5 I4 Reserved for future use, do not connect RSVD_G0 C23 O3 Reserved for future use, do not connect RSVD_G1 F19 O3 Reserved for future use, do not connect RSVD_G2 M27 O3 Reserved for future use, do not connect RSVD_G4 P27 O3 Reserved for future use, do not connect RSVD_G4 P27 O3 Reserved for future use, do not connect RSVD_G5 A18 O3 Reserved for future use, do not connect RSVD_G6 A19 O3 Reserved for future use, do not connect RSVD_S1 A614 Unused input only, can be left open, recommend grounding. RSVD_S2 A615 Unused input only, can be left open, recommend grounding. RSVD_S2 A215 Unused input only, can be left open, recommend grou	RSVD_H8	L5	I ₃		Reserved for future use, can be left open, recommend grounding.					
RSVD_P13 J1 I3 Reserved for future use, can be left open, recommend grounding. RSVD_P0 P7 I4 Reserved for future use, do not connect RSVD_P1 P6 O2 Reserved for future use, do not connect RSVD_P2 P8 I4 Reserved for future use, do not connect RSVD_G0 C23 O3 Reserved for future use, do not connect RSVD_G1 F19 O3 Reserved for future use, do not connect RSVD_G2 M27 O3 Reserved for future use, do not connect RSVD_G3 N21 O3 Reserved for future use, do not connect RSVD_G4 P27 O3 Reserved for future use, do not connect RSVD_G5 A18 O3 Reserved for future use, do not connect RSVD_G6 A19 O3 Reserved for future use, do not connect RSVD_S1 AG14 Unused input only, can be left open, recommend grounding. RSVD_S2 AG15 Unused input only, can be left open, recommend grounding. RSVD_S2 Y27 Unused input only, can be left open, recommend grounding. RSVD_S21 Y28 Unused input only, can be left open, recommend grounding.	RSVD_H9	M5	l ₃		Reserved for future use, can be left open, recommend grounding.					
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RSVD_X12 U8 Reserved for future use, do not connect RSVD_X2 AE15 Reserved for future use, do not connect	RSVD X13	U7			Reserved for future use, do not connect					
RSVD X2 AF15 Reserved for future use, do not connect	RSVD X12	U8			Reserved for future use, do not connect					
	RSVD X2	AF15			Reserved for future use, do not connect					

DLPS014D-APRIL 2010-REVISED MARCH 2012

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TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	CLOCK	DECODIDION			
NAME	NO.	TYPE ⁽¹⁾	SYSTEM	DESCRIPTION			
Reserved (Continued)							
RSVD_X0	AF18			Reserved for future use, do not connect			
RSVD_X1	AD15			Reserved for future use, do not connect			
RSVD_X8	AF27			Reserved for future use, do not connect			
RSVD_X4	AF9			Reserved for future use, do not connect			
RSVD_S4	AH26			Reserved for future use, do not connect			
RSVD_S5	B25			Reserved for future use, do not connect			
RSVD_S6	C20			Reserved for future use, do not connect			
RSVD_S8	D19			Reserved for future use, do not connect			
RSVD_X5	E24			Reserved for future use, do not connect			
RSVD_S10	F22			Reserved for future use, do not connect			
RSVD_S11	K28			Reserved for future use, do not connect			
RSVD_S14	N25			Reserved for future use, do not connect			
RSVD_X7	R24			Reserved for future use, do not connect			
RSVD_S16	R27			Reserved for future use, do not connect			
RSVD_S17	R28			Reserved for future use, do not connect			
RSVD_S18	U23			Reserved for future use, do not connect			
RSVD_S19	U24			Reserved for future use, do not connect			
Power and Ground ⁽⁴⁾							
P1P2V		PWR	N/A	1.2-V core power			
P2P5V_DPLL		PWR	N/A	2.5-V filtered power for internal PLL			
P1P8V		PWR	N/A	1.8-V I/O power			
P2P5V		PWR	N/A	2.5-V I/O power			
P3P3V		PWR	N/A	3.3-V I/O power			
GND		PWR	N/A	Common digital ground			
GNDA		PWR	N/A	Common PLL ground			

(4) Unused inputs should be pulled down to ground through an external resistor.

I/O CHARACTERISTICS⁽¹⁾

all inputs/outputs are LVCMOS

		CONDITIONS	V	/ _{IL} (V)	V _{IH} (V)	V _{OH} (V)	V _{oL} (V)	
	WOTTPE	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
I ₁	Input LVCMOS	V _{CCIO} = 1.8 V	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	2.25			V
I_2	Input LVCMOS	$V_{CCIO} = 2.5 V$	-0.3	0.7	1.7	V_{CCIO} + 0.3			V
l ₃	Input LVCMOS	$V_{CCIO} = 3.3 V$	-0.3	0.8	1.7	3.6			V
I_4	Input LVTTL	$V_{CCIO} = 3.3 V$	-0.3	0.8	1.7	3.6			V
O ₁	Output LVCMOS	V _{CCIO} = 1.8 V					$V_{CCIO} - 0.45$	0.45	V
O ₂	Output LVTTL	$V_{CCIO} = 3.3 V$					2.4	0.45	V
O ₃	Output LVCMOS	$V_{CCIO} = 3.3 V$					$V_{CCIO} - 0.2$	0.2	V
O ₄	Output LVDS	$V_{CCIO} = 3.3 V$					$V_{CCIO} - 0.3$	0.3	V
O ₅	Output SSTL-18 Class I	V _{CCIO} = 1.8 V					1.484	0.398	V
B ₁	Bidirectional SSTL- 18 Class I	V _{CCIO} = 1.8 V		0.844	1.094		1.484	0.398	V
B ₂	Bi-directional LVCMOS	V _{CCIO} = 3.3 V	-0.3	0.8	1.7	3.6	V _{CCIO} -0.2	0.2	V

(1) Cross reference to I/O assignments

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DLPS014D - APRIL 2010 - REVISED MARCH 2012

POWER	AND	GROUND	PINS

NAME	DESCRIPTION	PIN NUMBER(S)
Input Power and (Ground Pins	
VCC_1P2V	1.2-V power supply for core logic	K9, K11, K13, K15, K17, K19, L10, L12, L14, L16, L18, L20, M9, M11, M13, M15, M17, M19, N10, N12, N14, N16, N18, N20, P9, P11, P13, P15, P17, P19, R10, R12, R14, R16, R18, R20, T9, T11, T13, T15, T17, T19, U10, U12, U14, U16, U18, U20, V9, V11, V13, V15, V17, V19, W10, W12, W14, W16, W18, W20
VCC_2P5V	2.5-V power supply for I/Os on bank 5	AA28, AG28, T24, T28, W24
VCC_1P8V	1.8-V power supply for I/Os on banks 2, 3, 4	AA1, AG1, T1, T5, W5, AA11, AD6, AD9, AD13, AH2, AH5, AH9, AH13, AA18, AD16, AD20, AD23, AH16, AH20, AH24, AH27
VCC_3P3V	3.3-V power supply for I/Os on banks 1, 6, 7, 8	B1, H1, K5, N1, N5, B28, H28, K24, N24, N28 A16, A20, A24, A27, E16, E20, E23, H18, A2, A5, A9, A13, E6, E9, E13, H11
VCCA	2.5-V power supply for the internal PLL analog supply	Y8, J21, J8, Y21
VCCD_PLL	1.2-V power supply for the internal PLL digital supply	Y9, J20, J9, Y20
VREF_B2	DDR2 VREF 0.9 V. The SDRAM spec has guidelines on how these references should be connected. It is not just any 0.9-V source on the board.	T7, T8, AB4
VREF_B3	DDR2 VREF 0.9 V. The SDRAM spec has guidelines on how these references should be connected. It is not just any 0.9-V source on the board.	AB13, AB11, Y10
VREF_B4	DDR2 VREF 0.9 V. The SDRAM spec has guidelines on how these references should be connected. It is not just any 0.9-V source on the board.	AB20, AC18, AA15
DGND	Common ground	 K10, K12, K14, K16, K18, K20, L9, L11, L13, L15, L17, L19, M10, M12, M14, M16, M18, M20, N9, N11, N13, N15, N17, N19, P10, P12, P14, P16, P18, P20, R9, R11, R13, R15, R17, R19, T10, T12, T14, T16, T18, T20, U9, U11, U13, U15, U17, U19, V10, V12, V14, V16, V18, V20, W9, W11, W13, W15, W17, W19, AA2, AA27, AC6, AC9, AC13, AC16, AC20, AC23, AF1, AF28, AG2, AG5, AG9, AG13, AG16, AG20, AG24, AG27, B2, B5, B9, B13, B16, B20, B24, B27, C1, C28, F6, F9, F13, F16, F20, F23, H2, H27, J11, J18, K6, K23, N2, N6, N23, N27, T2, T6, T23, T27, W6, W23, Y11, Y18
DGND2	Analog ground return for the PLL (This should not be connected to the common ground GND.)	H9, H20, AA9, AA20
NC	No-connect pins	C3, F7, G7, G8, G10, G11, G19, G20, G21, G22, G23, G24, H8, H10, H12, H14, H15, H16, H17, H19, H21, H22, J5, J6, J7, J10, J12, J13, J14, J15, J16, J17, J19, J23, J24, K7, K8, K21, K22, L6, L7, L8, L21, L22, M7, M8, M23, N8, P21, R7, R21, R22, R23, U21, U22, V5, V6, V7, V8, V21, V22, W4, W7, W8, W21, W22, Y5, Y6, Y7, Y12, Y13, Y14, Y15, Y16, Y17, Y22, AA5, AA6, AA7, AA12, AA13, AA14, AA19, AA21, AA23, AB10, AB12, AB14, AB15, AB18, AB19, AB21, AB22, AC10, AC12, AC14, AC19, AC22, AD14, AD19, AD22, AE26

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CC12}			–0.5 V to 1.8	
V _{CCIO18}	Supply voltage range (2)		–0.5 V to 3.9	V
V _{CCA25_DPLL}	Supply voltage range V		-0.5 V to 3.75	v
V _{CCD_PLL1-4}				
VI	Input voltage range ⁽³⁾	1.8 V, 2.5 V, 3.3 V	-0.5 V to 3.95	V
TJ	Operating junction temperature range		-40°C to 125	°C
T _{stg}	Storage temperature range		–65°C to 150	°C
НВМ	Electrostatic discharge voltage using the human- body model		±2000	V
CD	Electrostatic discharge voltage using the charged- device model		±500	V

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND, and at the device, not at the power supply.

(3) Applies to external input and bidirectional buffers.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
V _{CC12}	1.2-V supply voltage, core logic		1.15	1.2	1.25	V
V _{CC18}	1.8-V supply voltage, HSTL output buffers		1.71	1.8	1.89	V
V _{CCA25_DPLL}	2.5-V analog voltage for PLL regulator		2.375	2.5	2.625	V
V _{CCD_PLL1-4}	1.2-V supply voltage, for PLL		1.15	1.2	1.25	V
V _{CC33}	3.3-V supply voltage		3.135	3.3	3.465	V
V _{REF_B2-4}	0.9-V reference voltage, for DDR2 SDRAM		0.833	0.9	0.969	V
VI	Input voltage		-0.5		3.6	V
Vo	Output voltage		0		V _{CCIO}	V
t _{Ramp}	Power supply ramp time		50 µs		3 ms	-
TJ	Operating junction temperature ⁽¹⁾		-20		85	°C
R _C	Case-to-ambient thermal resistance	T_A = ambient temperature P = Power		[(T _J –	T _A) / P] - 3.3	°C/W

(1) Heat sink not required for 0 to 55, but for 55 to 85, low-profile (15-mm) heat sink recommended



DLPS014D - APRIL 2010 - REVISED MARCH 2012

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Video Input Pixel Interface

Figure 2 illustrates how pixels should be mapped to the input data bus for both Port 1 and Port 2.

24-Bit Input Bus, RGB888

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POF
																								Defa
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	В3	B2	B1	B0	RGE

PORTx_D(23:0) of the Input Pixel Data Bus Default Bus Assignment Mapping RGB888 Format

Figure 2. Pixel Mapping

IMAGE SYNC AND BLANKING REQUIREMENTS

	PARAMETER	MIN	MAX	UNIT
t _{p_vsw}	Vertical sync duration	1		clocks
t _{p_vbp}	Vertical back porch	14		lines
t _{p_vfp}	Vertical front porch	2		lines
t _{p_hsw}	Horizontal sync duration	1		clocks
t _{p_hbp}	Horizontal back porch	64		clocks
t _{p_hfp}	Horizontal front porch	75		clocks

TIMING REQUIREMENTS

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
f _{pclock}	Clock frequency, PORTx_CLK			80	MHz
t _{p_wh}	Pulse duration, high	45% to 55% reference points (signal)	5.6		ns
t _{p_wl}	Pulse duration, low	45% to 55% reference points (signal)	5.6		ns
t _{p_su}	Setup time, PORTx_D(23-0) valid before PORTx_CLK	See (1)	1.5		ns
t _{p_h}	Hold time, PORTx_D(23–0) valid after PORTx_CLK	See (1)	1.5		ns
t _{p_su}	Setup time, PORTx_VSYNC valid before PORTx_CLK	See (1)	1.5		ns
t _{p_h}	Hold time, PORTx_VSYNC valid after PORTx_CLK	See (1)	1.5		ns
t _{p_su}	Setup time, PORTx_HSYNC valid before PORTx_CLK	See (1)	1.5		ns
t _{p_h}	Hold time, PORTx_HSYNC valid after PORTx_CLK	See (1)	1.5		ns
t _{p_su}	Setup time, PORTx_IVALID valid before PORTx_CLK	See (1)	1.5		ns
t _{p_h}	Hold time, PORTx_IVALID valid after PORTx_CLK	See (1)	1.5		ns

(1) PCLK may be inverted from that shown in Figure 3. In that case, the same specifications in the table are valid except now referenced to the falling edge of the clock. If the falling edge of PCLK is to be used, a USB or SPI command is needed to tell the DLPC200 to use the falling edge of PCLK. DLPS014D - APRIL 2010-REVISED MARCH 2012

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DLPC200 Master, I²C Interface, for Extended Display Identification Data (EDID) Programming

The DLPC200 controller I²C interface is used only to program the HDMI EDID. Upon plugging in an HDMI source, the DMD resolution is compared to the HDMI output resolution programmed in the HDMI EDID PROM. If the two do not match, then the HDMI EDID is adjusted to match the DMD resolution.

The bidirectional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.



DLPC200 Master, I²C Interface, for Extended Display Identification Data (EDID) Programming (continued)

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high. After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop). A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master.

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period. Setup and hold times must be met to ensure proper operation.

I²C INTERFACE TIMING REQUIREMENTS

	PARAMET	ER	MIN	MAX	UNIT
f _{scl}	I ² C clock frequency		0	400	kHz
t _{sch}	I ² C clock high time		1		ms
t _{scl}	I ² C clock low time		1		ms
t _{sp}	I ² C spike time			20	ns
t _{sds}	I ² C serial-data setup time		100		ns
t _{sdh}	I ² C serial-data hold time		100		ns
t _{icr}	I ² C input rise time		100		ns
t _{ocf}	I ² C output fall time	50 pF	30	200	ns
t _{buf}	I ² C bus free time between stop and start co	onditions	1.3		ms
t _{sts}	I ² C start or repeat start condition setup		1		ms
t _{sth}	I ² C start or repeat start condition hold		1		ms
t _{sph}	I ² C stop condition setup		1		ms
	Valid-data time	SCL low to SDA output valid		1	ms
۱ _{vd}	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low		1	ms
t _{sch}	I ² C bus capacitive load		0	100	pF



DLPS014D-APRIL 2010-REVISED MARCH 2012

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SDA LOAD CONFIGURATION



BYTE	DESCRIPTION
1	I ² C address
2, 3	P-port data

Figure 4. I²C Interface Load Circuit and Voltage Waveforms

Recommended EDID PROM Devices

PART NUMBER	MANUFACTURER
24LC02B	Microchip Technology



USB Interface

The USB interface consists of a single-chip integrated USB 2.0 transceiver, smart SIE, and enhanced 8051 microprocessor running at 48 MHz (nominal) that supports USB 2.0.

Bus Protocol

USB is a polled bus. The host controller (typically at PC) initiates all data transfers. Each transaction begins when the PC sends a packet. Communications are always through the bulk transfer mode, and 512 bytes of data are always written/read at a time. The packet consists of the following:

- Header (6 bytes)
- Data (505 bytes)
- Checksum (1 byte)

The USB device that is addressed selects itself by decoding the appropriate address fields. The direction of data transfer, either read or write, is specified in the packet header. The source of the transaction then sends a data packet or indicates it has no data to transfer. At the end of either a single packet transfer or a multi-packet transfer, the destination responds with a handshake packet indicating whether the transfer was successful.

The packet header consists of

- CMD1 Indicates if packet is write/write response or read/read response
- CMD2 Groups major functions together
- CMD3 Provides more information about packet grouping defined in CMD2
- · CMD4 Used to indicate location of data in a multi-packet transfer
- Len_MSB:Len_LSB Valid number of bytes of data transferred in packet data

Header				Data	Checksum		
CMD1 1 byte	CMD2 1 byte	CMD3 1 byte	CMD4 1 byte	Len_LSB 1 byte	Len_MSB 1 byte	0-505 bytes	1 byte

Figure 5. USB Data Packet

As discussed previously, the header describes whether the data transaction is to be a read or write and designates the data endpoint. The data portion of the packet carries the payload and is followed by a handshaking mechanism, checksum, that reports if the data was received successfully, or if the endpoint is stalled or not available to accept data.

USB READ INTERFACE TIMING REQUIREMENTS

	PARAMETER	MIN	Тур	MAX	UNIT
t _{CL}	1/CLKOUT frequency		20.8		ns
t _{AV}	Delay from clock to valid address			10.7	ns
t _{STBL}	Clock to USB_RDY0 LOW			11	ns
t _{STBH}	Clock to USB_RDY0 HIGH			11	ns
t _{SCSL}	Clock to USB_PA02 LOW			13	ns
t _{DSU}	Data setup to clock	9.6			ns
t _{DH}	Data hold time	0			ns
t _{ACC1}	Valid USB_PA04 to valid USB_FDC	43			ns

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Figure 6. USB Read Timing

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USB WRITE INTERFACE TIMING REQUIREMENTS

	PARAMETER	MIN	MAX	UNIT
t _{AV}	Delay from clock to valid address	0	10.7	ns
t _{STBL}	Clock to USB_RDY1 pulse LOW	0	11.2	ns
t _{STBH}	Clock to USB_RDY1 pulse HIGH	0	11.2	ns
t _{SCSL}	Clock to USB_PA02 pulse LOW		13	ns
t _{ON1}	Clock to data turnon	0	13.1	ns
t _{OFF1}	Clock to data hold time	0	13.1	ns



Figure 7. USB Write Timing

Recommended USB Devices

PART NUMBER	MANUFACTURER
CY7C68013A	Cypress
24LC128I/SN	Microchip Technology

SPI Slave Interface

The DLPC200 controller SPI interface consists of a 5-MHz input.

The SPI bus specifies five logic signals.

- SLAVE_SPI_CLK Serial clock (output from master)
- SLAVE_SPI_MOSI Master output, slave input (output from master)
- SLAVE_SPI_MISO Master input, slave output (output from slave)
- SLAVE_SPI_CS Slave select (active-low; output from master)

DLPS014D-APRIL 2010-REVISED MARCH 2012



SPI Slave Interface (continued)

 SLAVE_SPI_ACK — Holdoff signal to indicate that the slave is processing commands and cannot accept new input (output from slave)

The master pulls the slave-select low. During each SPI clock cycle, a full-duplex data transmission occurs:

- The master sends a bit on the MOSI line; the slave reads it from that same line.
- The slave sends a bit on the MISO line; the master reads it from that same line.

Transmissions involve two shift registers, one in the master and one in the slave; they are connected in a ring. Data is shifted out with the most-significant bit first, while shifting a new least-significant bit into the same register.

After that register has been shifted out, the master and slave have exchanged register values. If there is more data to exchange, the shift registers are loaded with new data and the process repeats. Transmissions may involve any number of clock cycles.

When there is no more data to be transmitted, the master stops toggling its clock. Transmissions consist of packet commands/responses similar to the protocol defined for the USB interface. The SPI slave supports variable-length command and response packets, and a master can initiate multiple such transmissions as needed.

SPI SLAVE INTERFACE TIMING REQUIREMENTS

	PARAMETER	MIN	MAX	UNIT
f _{clock}	Clock frequency, SLAVE_SPI_CLK		5	MHz
t _{p_clkper}	Clock period, SLAVE_SPI_CLK	200		ns
t _{p_wh}	Pulse duration high, SLAVE_SPI_CLK	10		ns
t _{p_wl}	Pulse duration low, SLAVE_SPI_CLK	10		ns
t _{c_su}	Setup time, SLAVE_SPI_CS	6		ns
t _{c_h}	Hold time, SLAVE_SPI_CS	3		ns
t _{i_su}	Setup time, SLAVE_SPI_MOSI	10		ns
t _{i_h}	Hold time, SLAVE_SPI_MOSI	10		ns
t _{o_su}	Setup time, SLAVE_SPI_MISO	10		ns
t _{o_h}	Hold time, SLAVE_SPI_MISO	10		ns
t _{a_su}	Setup time, SLAVE_SPI_ACK	7		ns
t _{a_h}	Hold time, SLAVE_SPI_ACK	7		ns



DLPS014D - APRIL 2010 - REVISED MARCH 2012

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Parallel Flash Memory Interface

The controller parallel flash memory interface supports a high-speed NOR device with a 16-bit data bus and up to 1GB of memory.

To perform an asynchronous read, an address is driven onto the address bus, and \overline{CE} is asserted. WE and \overline{RST} must already have been deasserted. WAIT is configured to be active low and is set to a deasserted state. ADV must be held low throughout the read cycle. CLK is not used for asynchronous reads, and is ignored. After \overline{OE} is asserted, the data is driven onto DQ[15:0] after an initial access time t_{AVQV} or t_{GLQV} delay.

The WAIT signal indicates data valid when the device is operating in asynchronous mode (RCR.15 = 0). The WAIT signal is only deasserted when data is valid on the bus. When the device is operating in asynchronous non-array read mode, such as read status, read ID, or read query, the WAIT signal is also deasserted when data is valid on the bus. WAIT behavior during asynchronous non-array reads at the end of word line works correctly only on the first data access.

To perform a write operation, both \overline{CE} and \overline{WE} are asserted while \overline{RST} and \overline{OE} are deasserted. During a write operation, address and data are latched on the rising edge of \overline{WE} or \overline{CE} , whichever occurs first. When the device is operating in write operations, WAIT is set to a deasserted state as determined by RCR.10.

PARALLEL FLASH INTERFACE TIMING REQUIREMENTS

	PARAMETER	MIN	MAX	UNIT
t _{AVAV}	Read cycle time		110	ns
t _{AVQV}	Address to output valid		110	ns
t _{ELQV}	CE low to output valid		110	ns
t _{GLQV}	OE low to output valid		25	ns
t _{PHQV}	RST high to output valid		150	ns
t _{GLTV}	OE low to WAIT valid		17	ns
t _{PHWL}	RST high recovery to WE low	150		ns
t _{ELWL}	CE setup to WE low	0		ns
t _{WLWH}	WE write pulse width low	50		ns
t _{DVWH}	Data setup to WE high	50		ns
t _{AVWH}	Address setup to WE high	50		ns
t _{WHEH}	CE hold from WE high	0		ns
t _{PWDHX}	Data hold from \overline{WE} high	0		ns
t _{WHAX}	Address hold from WE high	0		ns

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DLPS014D - APRIL 2010-REVISED MARCH 2012

Figure 9. Parallel Flash Read Timing

Figure 10. Parallel Flash Write Timing

Recommended Parallel Flash Devices

PART NUMBER	MANUFACTURER	SIZE
JS28F00AP30BF	Numonyx	128 Mbit

Serial Flash Memory Interface

The DLPC200 controller flash memory interface consists of a SPI flash serial interface at 33.3 MHz (nominal).

SERIAL FLASH INTERFACE TIMING REQUIREMENTS

	PARAMETER	MIN	MAX	UNIT
f _{clock}	Clock frequency, CFG_CLK	DC	33	MHz
t _{p_clkper}	Clock period, CFG_CLK		30.03	ns
t _{p_wh}	Pulse duration low, CFG_CLK	6		ns
t _{p_wl}	Pulse duration high, CFG_CLK	6		ns
t _{p_su}	Setup time – CFG_ASDI/CFG_ASDO valid before CFG_CLK rising edge	2		ns
t _{p_h}	Hold time – CFG_ASDI/CFG_ASDO valid after CFG_CLK rising edge	5		ns

DLPS014D - APRIL 2010-REVISED MARCH 2012

Figure 11. Flash Memory Interface Timing

Table 2 shows the serial flash parts that were tested by TI and found to work properly with the DLPC200.

PART NUMBER	MANUFACTURER	SIZE
M25P64	Numonyx	64 Mbit
W25X64	Winbond	64 Mbit

Table 2. Recommended Serial Flash Devices

STATIC RAM Interface

The DLPC200 controller Static RAM (SRAM) interface consists of a high performance CMOS Static RAM organized as 128K words by 16 bits (2 Mbit).

STATIC RAM INTERFACE TIMING REQUIREMENTS

	PARAMETER	MIN	MAX	UNIT
t _{RC}	Read cycle time	10		ns
t _{AA}	Address to data valid		10	ns
t _{OHA}	Data hold from address change	3		ns
t _{WC}	Write cycle time	10		ns
t _{SCE}	CE low to write end	7		ns
t _{AW}	Address setup to write end	7		ns
t _{HA}	Address hold from write end	0		ns
t _{SA}	Address setup to write start	0		
t _{PWE}	WE pulse width	7		
t _{SD}	Data setup to write end	5		
t _{HD}	Data hold from write end	0		

Table 3 shows the serial flash parts that were tested by TI and found to work properly with the DLPC200. See the recommended Static RAM data sheet for read and write cycle timing information.

Table 3. Recommended Static RAM Devices

PART NUMBER	MANUFACTURER	SIZE
CY7C1011DV33	Cypress	2 Mbit

DMD Interface

The DLPC200-DMD interface consists of a 200 MHz (nominal) DDR output-only interface with LVDS signaling.

DMD INTERFACE TIMING REQUIREMENTS

	PARAMETER	MIN	ТҮР	MAX	UNIT
f _{clock}	Clock frequency, DCLK_A and DCLK_B		200		MHz
t _{p_clkper}	Clock period, DCLK_A and DCLK_B		5		ns
t _{p_wh}	Pulse duration low, DCLK_A and DCLK_B		1.25		ns
t _{p_wl}	Pulse duration high, DCLK_A and DCLK_B		1.25		ns
t _{skew}	Channel B relative to channel A	-1.25		1.25	ns
t _{p_su}	Output setup time – D_A(0:15) and D_B(0:15) relative to both rising and falling edges of DCLK_A and DCLK_B, respectively	0.35			ns
t _{p_h}	Output hold time – D_A(0:15) and D_B(0:15) relative to both rising and falling edges of DCLK_A and DCLK_B, respectively	0.35			ns

Figure 12. DMD I/F Timing

DLPA200 Interface

The DLPC200 interface to the DLPA200 consists of a 125 kHz (nominal) serial communications port (SCP).

DLPA200 INTERFACE TIMING REQUIREMENTS

	PARAMETER	MIN	TYP	MAX	UNIT
f _{clock}	Clock frequency		125	125	kHz
t _{p_clkper}	Clock period			8	us
t _{p_wh}	Pulse duration low			4	us
t _{p_wl}	Pulse duration high			4	us
t _{p_su}	SCPDI setup time	7.3			ns
t _{p_h}	SCPDI hold time	5.7			ns

Figure 13. DLPA200 I/F Timing

DDR2 SDR Memory Interface

The DDR2 SDRAM is a high-speed CMOS, dynamic random-access memory. It is internally configured as a multibank DRAM. The controller DDR-2 memory interface consists of four 32-Mbit by 16-bit wide, DDR-2 interfaces with double-data-rate signaling, operating at 133.33 MHz (nominal). A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READ commands and by the memory controller during WRITE commands. DQS is edge-aligned with data for READ commands and center-aligned with data for WRITE commands.

The DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK. Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

	PARAMETER	MIN	MAX	UNIT
t _{CYCLE}	Cycle time reference	5	8	ns
t _{CH}	CK high pulse duration ⁽¹⁾	2.4	4.16	ns
t _{CL}	CK low pulse duration ⁽¹⁾	2.4	4.16	ns
t _{CMS}	Command setup	200		ps
t _{CMH}	Command hold	275		ps
t _{AS}	Address setup	400		ps
t _{AH}	Address hold	400		ps
t _{DS}	Write data setup	1.5		ns
t _{DH}	Write data hold	1.5		ns
t _{AC}	Read data access time	-450	450	ps
t _{OH}	Read data hold time		340	ps
t _{LZ}	Read data low-impedance time	-900	450	ps
t _{H7}	Read data high-impedance time		450	ps

DDR2 SDR MEMORY INTERFACE TIMING REQUIREMENTS

(1) Output setup/hold numbers already account for controller clock jitter. Only routing skew and memory setup/hold need be considered in system timing analysis.

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INSTRUMENTS

DLPS014D - APRIL 2010-REVISED MARCH 2012

Figure 14. SDR Memory I/F Write Timing

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DLPS014D - APRIL 2010 - REVISED MARCH 2012

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Figure 15. SDR Memory I/F Read Timing

SDRAM Memory

The DLPC200 requires an external DDR2 SDR SDRAM. The DLPC200 supports the use of four 512-Mbit SDRAMs. The requirements for the SDRAMs are:

- SDRAM type: DDR2
- Speed: 133 MHz minimum
- 16-bit interface size: 32 Mbit
- Supply voltage: 1.8 V

Table 4 lists the Recommended SDRAM Devices that have been tested by TI and found to work properly with the DLPC200.

Table 4. Recommended	SDRAM	Devices
----------------------	-------	---------

PART NUMBER	MANUFACTURER	SIZE
MT47H32M16R	Micron	512 Mbit

POWER-UP REQUIREMENTS

Details about the chip power-up requirements are included in the DLPZ004 Chipset data sheet. For the DLPC200, there is a 50-MHz reference clock that must meet the specifications listed in the table 5 below. Additionally, at power up, the 3.3-V supply must be stable for two seconds before the global reset (RESET) occurs, and then PWR_GOOD occurs within 20 ms.

PART NUMBER	FREQUENCY STABILITY	FREQUENCY	SUPPLY VOLTAGE
ASV-50.000MHZ-E-J-T	±20 ppm (0.002% or ±0.001 MHz)	50 MHz	3.3 V

POWER-DOWN REQUIREMENTS

Details about the chip power-down requirements are included in the DLPZ004 Chipset data sheet. For the DLPC200, there is a minimum 1-ms delay from the time when PWR_GOOD goes low until any of the supplied voltages can drop below their minimum valid values; see Table 6. This is required so that the DMD can be parked. See the following figure for more detail.

Table 6. Supply Voltages and Minimum Values

V _{cc}	V _{cc_min}	UNIT
1.2	1.14	
1.8	1.71	V
2.5	2.375	V
3.3	3.135	

Thermal Considerations

The underlying thermal limitation for the DLPC200 is that the maximum operating junction temperature (T_J) not be exceeded (see Recommended Operating Conditions). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC200 and power dissipation of surrounding components. The DLPC200 package is designed primarily to extract heat through the power and ground planes of the PCB; thus, copper content and airflow over the PCB are important factors. DLPC200

DLPS014D – APRIL 2010–REVISED MARCH 2012

REVISION HISTORY

Changes from Original (April 2010) to Revision A Page • Changed TI Lit Number from DLPS012 to DLPZ004 in Related Documents table 2 • Added / changed pin names, updated descriptions in TERMINAL FUNCTIONS table 7 • Deleted unused types, updated values in I/O CHARACTERISTICS table 18 • Changed junction temperature and notated need for heat sink 20 • Changed parameter names to match figure 21 • Added new section for POWER-UP REQUIREMENTS 37

Changes from Revision A (May 2010) to Revision B

•	Changed typo on pin number for MEM_D43 Terminal	15
•	Changed typo on pin number for MEM_D62 Terminal	15
•	Added part number used for EEPROM	27
•	Changed part number for Winbond part	32
•	Added new section for POWER-DOWN REQUIREMENTS	37

Changes from Revision B (December 2010) to Revision C

•	Changed Typical Application diagram	3
•	Changed location of Device Marking in document	4
•	Replaced "DAD" with "DLPA200"	5
•	Changed typo on pin number for PORT1_D10 Terminal	7
•	Changed typo on pin number for USB_CLK Terminal	9
•	Changed I/O type to B ₂ for USB interface data bus Terminals	9
•	Added pin number A15 to TERMINAL FUNCTIONS table	9
•	Changed I/O type to B ₂ for Flash/SRAM data Terminals	12
•	Corrected the I/O type to O_3 on $\overline{CFG_CSO}$ terminal pin	16
•	Added pin number AB17 to TERMINAL FUNCTIONS table	17
•	Added pin number U7 to TERMINAL FUNCTIONS table	17
•	Added pin number U8 to TERMINAL FUNCTIONS table	17
•	Added pin number AD15 to TERMINAL FUNCTIONS table	18
•	Changed location of Absolute Maximum Ratings and Recommended Operating Conditions Tables in document	20
•	Changed MIN and MAX T_J values in RECOMMENDED OPERATING CONDITIONS	20
•	Added V _{CC33} and V _{REF_B2-4} pins to 'RECOMMENDED OPERATING CONDITIONS'	20
•	Changed Input Port Interface figure	22
•	Changed SPI SLAVE INTERFACE TIMING REQUIREMENTS table	28
•	Added SPI Timing diagram	28
•	Changed paragraph about read mode in Parallel Flash Memory Interface	29
•	Changed RST signal timing in Parallel Flash Write Timing diagram	31
•	Changed signal notations in SERIAL FLASH INTERFACE TIMING REQUIREMENTS table	31
•	Changed signal notations in Flash Memory Interface Timing diagram	32
•	Deleted SRAM Interface Timing diagram and provided reference to the OEM datasheet	32
•	Changed signal notations in DLPA200 I/F Timing diagram	34

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www.ti.com

Page

DLPS014D - APRIL 2010-REVISED MARCH 2012

Cł	nanges from Revision C (February 2012) to Revision D	Page
•	Changed the ADV time line in Figure 9	30

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾ F	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
DLPC200ZEW	ACTIVE	BGA	ZEW	780	5	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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ZEW (S-PBGA-N780)

PLASTIC BALL GRID ARRAY

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-034, Variation: AAM-1.
- D. This package is Pb-free.

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