DLP® Configuration PROM for DLPC100

Check for Samples: DLPR100

FEATURES

- **Programmed for Use With the DLPC100 and DLP1700 (0.17 HVGA Chipset)**
- **Data Transfer up to 150 M-Bits/Second**
- **Single 2.7 to 3.6 V Supply**
- **5 mA Active-Current, 1-µA Powerdown (Typ)**
- **–40°C to 85°C Operating Temperature Range**

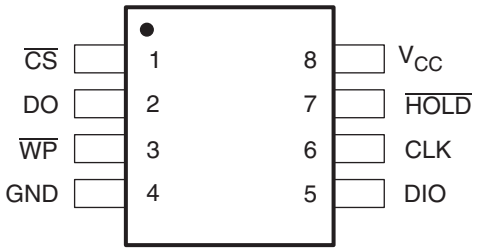
DESCRIPTION

The DLPR100 is one of three components in the 0.17 HVGA chipset (see Block Diagram). Proper function and operation of the DLPR100 requires that it be used in conjunction with the other components of the 0.17 HVGA chipset. Refer to the 0.17 HVGA Chip-Set data sheet for further details (TI Literature Number DLPS017).

The serial flash device provides a storage solution for the DLPC100 device in the 0.17 HVGA chipset. The device operates on a single 2.7 V to 3.6 V power supply with current consumption as low as 5 mA active and 1 µA for power-down. The DLPR100 supports the standard Serial Peripheral Interface (SPI). SPI clock frequencies of up to 75 MHz are supported.

ORDERING INFORMATION

T_A	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	DLPR100DWC	By Pin 1



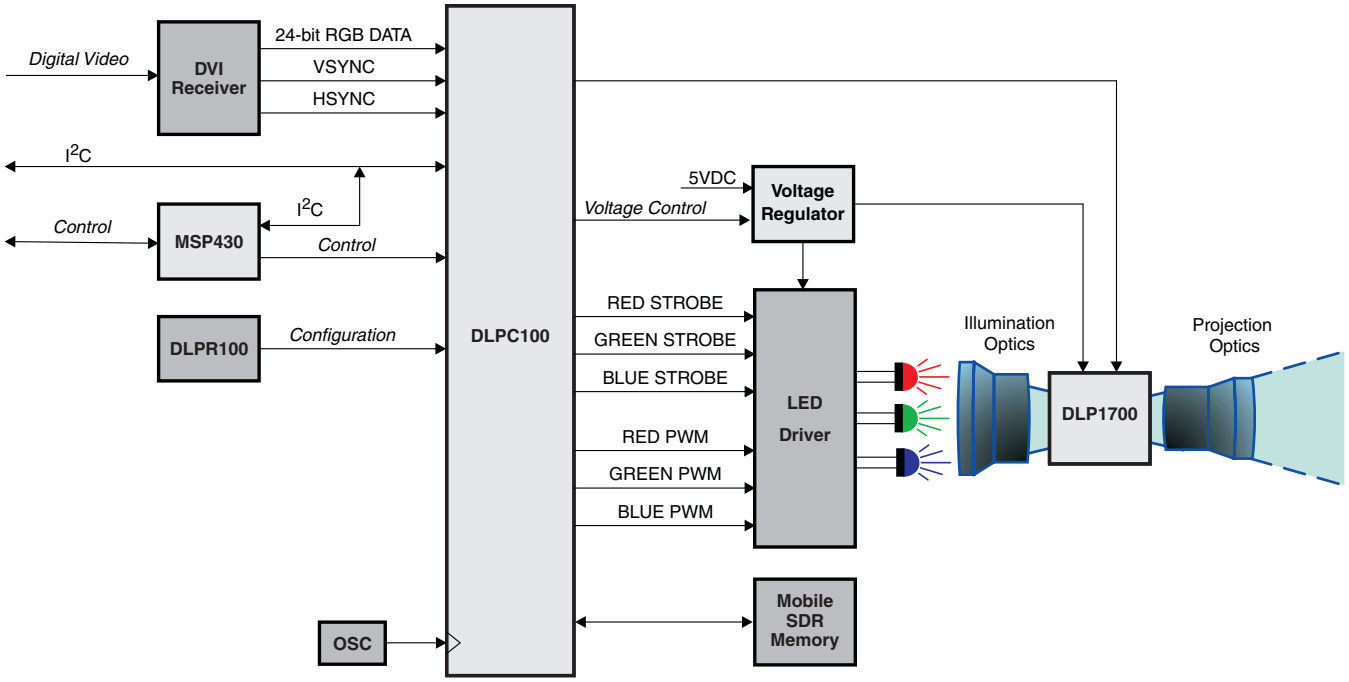
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{CS}$	I	Chip select, active low. When $\overline{CS}$ is high, the device is deselected and DO pin is high impedance.
2	DO	O	Data output. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin.
3	$\overline{WP}$	I	Write protect input, active low. Disables writes to the status register when the Status Register Protect (SRP) bit is set to a 1 state.
4	GND	–	Ground
5	DIO	I/O	Data input/output. Data is latched on the rising edge of the CLK input pin.
6	CLK	I	Serial clock. Provides the timing clock for the serial input and output operation.
7	$\overline{HOLD}$	I	Hold input, active low. Allows the device to be paused. When $\overline{HOLD}$ is brought low, while $\overline{CS}$ is low, the DO pin will be at high impedance and signals on the DIO and CLK pins will be ignored. Device operation will resume when $\overline{HOLD}$ is brought high.
8	V_{CC}	–	Power supply

Related Documents

DOCUMENT	TI LITERATURE NUMBER
DLP 0.17 HVGA Chip-Set data sheet	DLPS017
DLPC100 Digital Controller data sheet	DLPS019
DLP1700 0.17 HVGA DMD data sheet	DLPS018

Block Diagram



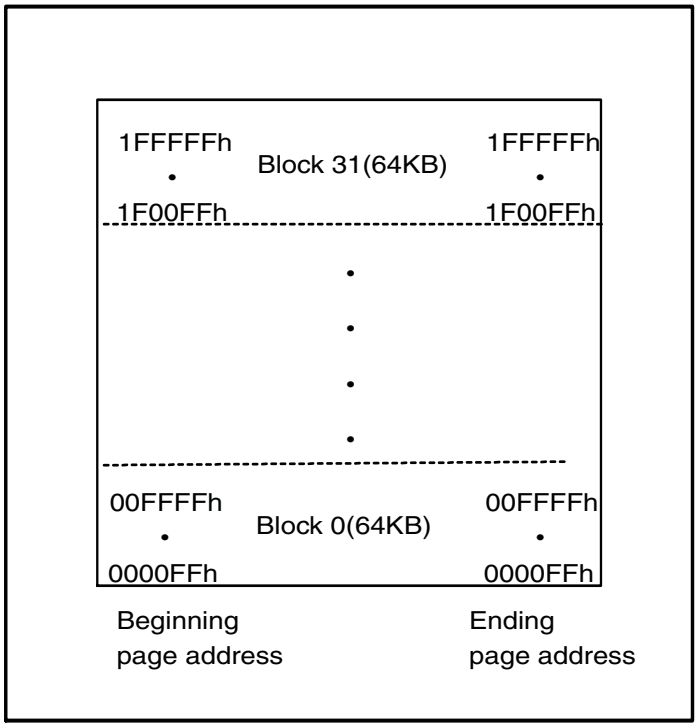


Figure 1. Memory Blocks of the DLPR100

Functional Description

The memory blocks of the DLPR100 are shown in Figure 1.

SPI Operation

The DLPR100 is accessed through an SPI compatible bus. Data input on the DIO pin is sampled on the rising edge of the CLK. Data on the DO and DIO pins are clocked out on the falling edge of the CLK.

Write Protection

Upon power-up or at power-down the DLPR100 will maintain a reset condition while VCC is below the threshold value of VWI. While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds VWI, all program and erase related instructions are further disabled for a time of tPUW. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin ($\overline{CS}$) must track the VCC supply level at power-up until the VCC-min level and tVSL time delay is reached. If needed a pull-up resistor on $\overline{CS}$can be used to accomplish this. After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a write operation will be accepted. After completing a write operation the Write Enable Latch (WEL) is automatically cleared to a write-disabled status of 0. Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP) and Block Protect (TB, BP2, BP1, and BP0) bits. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Released Power-down instruction.

Control and Status Registers

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled/disabled, and the state of write protect. The Write Status Resister instruction can be used to configure the device's write protection feature.

Status Register

Busy

Busy is a read only status register (S0) that is set to 1 state when the device is executing a write operation. When write operation is completed the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled. A write disable state occurs upon power-up.

Block Protect Bits (BP2, BP1, BP0)

Block Protect Bits are non-volatile read/write bits in the status register (S4,S3,S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register instruction. The factory default setting for the Block Protect bits is 0, none of the array protected. The Block Protect bits cannot be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (/WP) pin is low.

Top/Bottom Block Protect (TB)

The Top/Bottom bit (TB) controls if the block protect bits (BP2,BP1,BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array. Factory default setting is TB=0. The TB bit cannot be written to if the Status Register Protect (SRP) bit is set to 1 and Write Protect (/WP) pin is low.

Reserved Bits

Status register bit location S6 is reserved for the future use. Device will read 0 for this bit.

Status Register Protect (SRP)

The Status Register Protect (SRP) bit is a read/write bit in status register (S7) that can be used in conjunction with the Write Protect ($\overline{WP}$) pin to disable writes to the status register. When the SRP bit is set to 0 state (factory default) the $\overline{WP}$ pin has no control over Status Register. When the SRP bit is set to a 1 state, the Write Status Register is locked out while the $\overline{WP}$ pin is low. When the $\overline{WP}$ pin is high the Write Status Register instruction is allowed.

Table 1. Status Register Bit Locations

S7	S6	S5	S4	S3	S2	S1	S0
SRP	(R)	TB	BP2	BP1	BP0	WEL	BUSY

Table 2. Status Register Memory Protection

STATUS REGISTER				MEMORY PROTECTION			
TB(1)	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	1	31	1F0000h-1FFFFFh	64KB	Upper 1/32
0	0	1	0	30 thru 31	1E0000h-1FFFFFh	128KB	Upper 1/16
0	0	1	1	28 thru 31	1C0000h-1FFFFFh	256KB	Upper 1/8
0	1	0	0	24 thru 31	180000h-1FFFFFh	512KB	Upper 1/4
0	1	0	1	16 thru 31	100000h-1FFFFFh	1MB	Upper 1/2
1	0	0	1	0	000000h-00FFFFh	64KB	Lower 1/32
1	0	1	0	0 and 1	000000h-01FFFFh	128KB	Lower 1/16
1	0	1	1	0 thru 3	000000h-03FFFFh	256KB	Lower 1/8
1	1	0	0	0 thru 7	000000h-07FFFFh	512KB	Lower 1/4
1	1	0	1	0 thru 15	000000h-0FFFFFh	1MB	Lower 1/2

(1) x = don't care

Table 2. Status Register Memory Protection (continued)

STATUS REGISTER				MEMORY PROTECTION			
TB(1)	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
x	1	1	X	0 thru 31	000000h-1FFFFFh	2MB	ALL

Instructions

The instruction set of the DLPR100 consists of fifteen basic instructions that are fully controlled through the SPI bus. Instructions are initiated by the falling edge of the Chip Select ($\overline{CS}$). The first byte of data clocked into the DIO input provides the instruction code. Data on the DIO input is sampled on the rising edge of the clock with most significant bit (MSB) first. Instructions are completed with the rising edge of $\overline{CS}$.

Table 3. Manufacturer and Device Identification

MANUFACTURER ID	(M7-M0)	
Winbond Serial Flash	EFH	
DEVICE ID	**(ID7-ID0)**	**(ID15-ID0)**
INSTRUCTION	**ABh, 90h**	**9Fh**
W25X16A	14h	3015h

Table 4. Instruction Set(1)

INSTRUCTION NAME	BYTE1 CODE	BYTE2	BYTE3	BYTE4	BYTE5	BYTE6	N-BYTES
Write Enable	06h						
Write Disable	04h						
Read Status Register	05h	(S7–S0)(1)					See (2)
Write Status Register	01h	S7–S0					
Read Data	03h	A23–A16	A15–A8	A7–A0	(D7–D0)	(Nest byte)	Continuous
Fast Read	0Bh	A23–A16	A15–A8	A7–A0	dummy	(D7–D0)	(Nest byte) continuous
Fast Read Dual Output	3Bh	A23–A16	A15–A8	A7–A0	dummy	I/O=(D6,D4,D2,D0) O=(D7,D5,D3,D1)	(one byte per 4 clocks cont.)
Page Program	02h	A23–A16	A15–A8	A7–A0	(D7–D0)	(Nest byte)	Up to 256 bytes
Block Erase (64KB)	D8h	A23–A16	A15–A8	A7–A0			
Sector Erase (4KB)	20h	A23–A16	A15–A8	A7–A0			
Chip Erase	C7h						
Power-down	B9h						
Release Power-down/Device ID	ABh	dummy	dummy	dummy	(ID7–ID0)(3)		
Manufacturer/Device ID(4)	90h	dummy	dummy	00h	(M7–M0)	(ID7–ID0)	
JEDEC ID	9Fh	(M7–M0) Manufacturer	(ID15–ID8) Memory Type	(ID7–ID0) Capacity			

(1) Data bytes are shifted with Most significant Bit first. Byte fields with data in parenthesis indicate data being read from the device on the DO pin.
(2) The status register contents will repeat continuously until $\overline{CS}$ terminates the instruction
(3) The Device ID will repeat continuously until $\overline{CS}$ terminates the instruction
(4) See Manufacturer and Device ID table for Device ID information

DLPR100 instruction example using the Read data (03h) instruction is shown in Figure 2.

Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the $\overline{CS}$pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23–A0) into the DIO pin. The code and address bits are latched in the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of the CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving the $\overline{CS}$ high. If a Read Data instruction is issued while a write operation is in process the instruction is ignored and will not have any effect on the current operation.

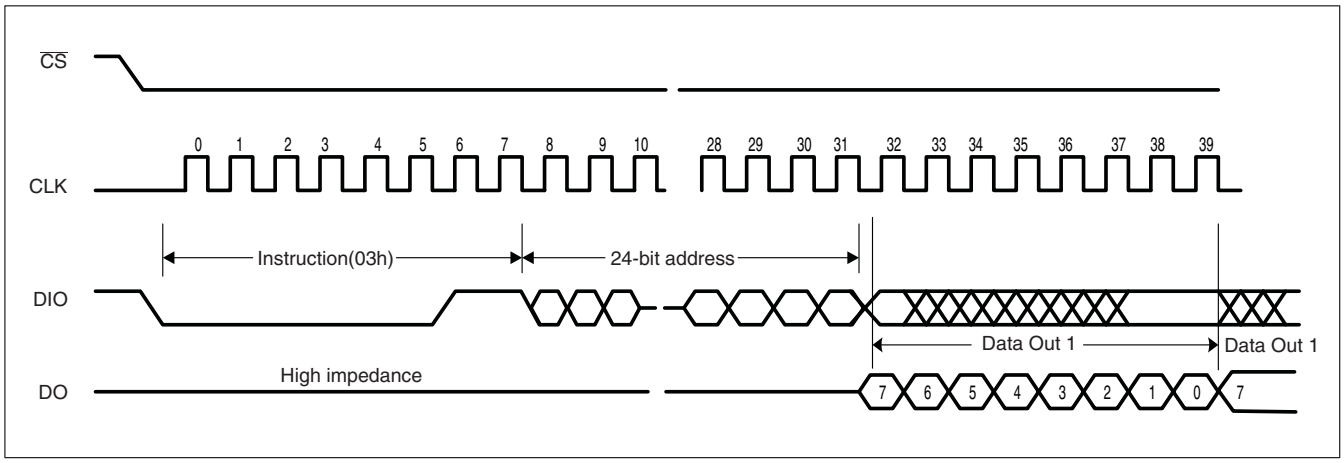


Figure 2. Read Data Instruction Sequence Diagram

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.6	4.0	V
V_{IO}	Voltage applied to any pin	Relative to ground	–0.6	V_{CC} + 0.4	V
V_{IOT}	Transient voltage on any pin	<20 ns transient relative to ground	–2.0	V_{CC} + 2.0	V
T_{stg}	Storage temperature		–65	150	°C
T_{LEAD}	Lead temperature			See (2)	°C
V_{ESD}	Electrostatic discharge voltage	Human Body Model(3)	–2000	2000	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Compliant with JEDEC standards J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substance (RoHS) 2002/95/EU.
(3) JEDEC Std JESD22-A114A (C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	Fr = 50MHz, f_R = 33 MHz	2.3	3.6	V
		Fr = 75 MHz, f_R = 33 MHz	2.7	3.6	
T_A	Ambient operating temperature	Industrial	–40	85	°C

POWER-UP TIMING AND WRITE INHIBIT THRESHOLD(1)

PARAMETER		MIN	MAX	UNIT
t_{VSL}	V_{CC}(min) to $\overline{CS}$ low	10		µs
t_{PUW}	Time delay before write instruction	1	10	ms
V_{WI}	Write inhibit threshold voltage	1	2	V

(1) Parameters are characterized only

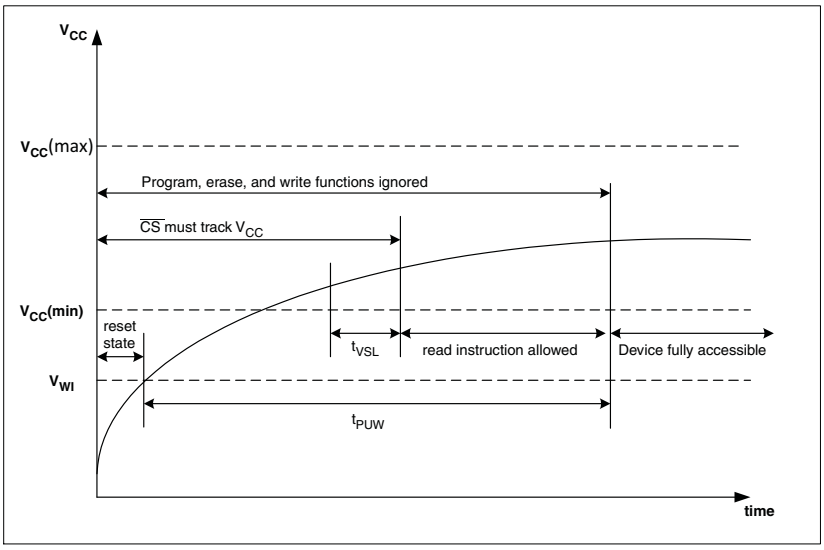


Figure 3. Power-Up Timing and Voltage Levels

DC ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance(1)	V_{IN} = 0 V				6	pF
C_{out}	Output capacitance(1)	V_{OUT} = 0 V				8	pF
I_{LI}	Input leakage					±2	µA
I_{LO}	I/O leakage					±2	µA
I_{CC1}	Standby current	$\overline{CS}$ = V_{CC}, V_{IN} = GND or V_{CC}			25	50	µA
I_{CC2}	Power-down current	$\overline{CS}$ = V_{CC}, V_{IN} = GND or V_{CC}			<1	10	µA
I_{CC3}	Current read data/dual output read(2)	C = 0.1 V_{CC}/0.9 V_{CC} DO = open	1 MHz		5/6	7/8	mA
			33 MHz		7/8	11/12	mA
			50 MHz		9/10	13/15	mA
			75 MHz		11/12	16/18	mA
I_{CC4}	Current page program	$\overline{CS}$ = V_{CC}			20	25	mA
I_{CC5}	Current Write Status Register	$\overline{CS}$ = V_{CC}			10	18	mA
I_{CC6}	Current sector/block erase	$\overline{CS}$ = V_{CC}			20	25	mA
I_{CC7}	Current chip erase	$\overline{CS}$ = V_{CC}			20	25	mA
V_{IL}	Low-level input voltage			–0.5		V_{CC} x 0.3	V
V_{IH}	High-level input voltage			V_{CC} x 0.7		V_{CC} + 0.4	V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA				0.4	V
V_{OH}	High-level output voltage	I_{OH} = –100 µA		V_{CC} - 0.7			V

(1) Tested on sample basis and specified through design and characterization data T_A= 25°C, V_CC = 3.0 V
(2) Checker board pattern

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.3 V to 3.6 V unless otherwise specified

SYMBOL	ALT	DESCRIPTION	MIN	TYP	MAX	UNIT
FR	f_C	Clock frequency for all instructions, except read data(03h) 2.3–3.6 V V_{CC}			50	MHz
FR	f_C	Clock frequency for all instructions, except read data(03h) 2.7–3.6 V V_{CC}			75	MHz
f_R		Clock frequency read data(03h)			33	MHz

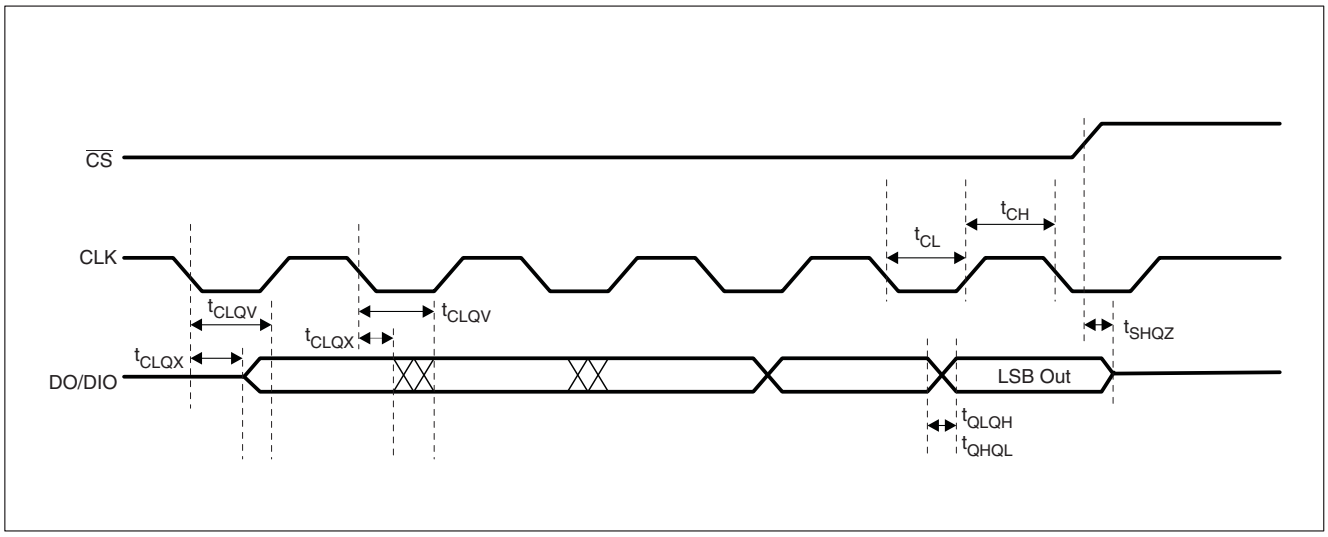
AC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 2.3 V to 3.6 V unless otherwise specified

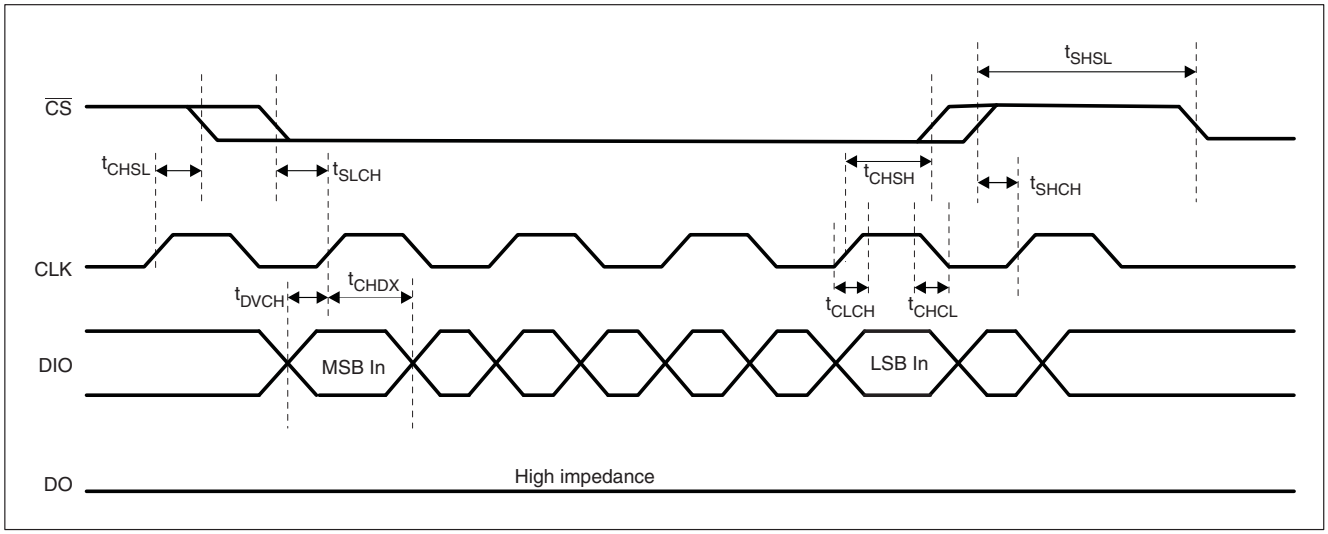
SYMBOL	ALT	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{CLH}, t_{CLL}		Clock high, low time, for fast read(0Bh, 3Bh)/other instructions except read data (03h)(1)	6/7			ns
tCLH, t_{CLL}		Clock high, low time, for all instructions 2.3 V-3.6 V V_{CC}(1)	8			ns
t_{CRLH}, t_{CRLL}		Clock high, low time, for read data(03h) instructions(1)	8			ns
t_{CLCH}		Clock rise time peak to peak(2)	0.1			V/ns
t_{CHCL}		Clock fall time peak to peak(2)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{CS}$ active setup time relative to CLK	5			ns
t_{CHSL}		$\overline{CS}$ Not active Hold time relative to CLK	5			ns
t_{DVCH}	t_{DSU}	Data in setup time	2			ns
t_{CHDX}	t_{DH}	Data in hold time	5			ns
t_{CHSH}		$\overline{CS}$ active hold time relative to CLK	5			ns
t_{SHCH}		$\overline{CS}$ not active setup time relative to CLK	5			ns
t_{SHSL}	t_{CSH}	$\overline{CS}$ deselect time (for array read->array read/erase or program->Read Status Register)	50/100			ns
t_{SHQZ}	t_{DIS}	Output disable time(3)			7	ns
t_{CLQV}	t_V	Clock low to output valid 2.7–3.6 V/ 3.0–3.6 V/ 2.3-3.6V			7/6/9	ns
t_{CLQX}	t_{OH}	Output hold time	0			ns
t_{HLCH}		$\overline{HOLD}$ active setup time relative to CLK	5			ns
t_{CHHH}		$\overline{HOLD}$ active Hold time relative to CLK	5			ns
t_{HHCH}		$\overline{HOLD}$ Not active setup time relative to CLK	5			ns
t_{CHHL}		$\overline{HOLD}$ Not active Hold time relative to CLK	5			ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ to output low-Z(3)			7	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ to output high-Z (3)			12	ns
t_{WHSL}		Write protect setup time before $\overline{CS}$ low(4)	20			ns
t_{SHWL}		Write protect Hold time after $\overline{CS}$ high(4)	100			ns
t_{DP}		$\overline{CS}$ high to power-down mode(3)			3	µs
t_{RES1}		$\overline{CS}$ high to standby mode without electronic signature Read(3)			3	µs
t_{RES2}		$\overline{CS}$ high to standby mode with electronic signature Read(3)			1.8	µs
t_W		Write Status Register time		10	15	ms
t_{BP1}		Byte program time (first byte)(5)		30	50	µs
t_{BP2}		Additional byte program time (after first byte)(5)		6	12	µs
t_{PP}		Page program time		1.6	3	ms
t_{SE}		Sector erase time (4KB)		120	200	ms
t_{BE}		Block erase time (64KB)		0.32	1	s
t_{CE}		Chip erase time		10	20	s

(1) Clock high + clock low must be less than or equal to 1/fC.
(2) Value ensured by design and/or characterization, not production tested.
(3) Value ensured by design and/or characterization, not production tested.
(4) Only applicable as a constraint for Write Status Register instruction when Sector Protect Bit is set to 1.
(5) For multiple bytes after the first byte within a page, $t_{BPN} = t_{BP1} + t_{BP2} * N$(typical) and $t_{BPN} = t_{BP1} + t_{BP2} * N$(max), where N = number of bytes programmed

Serial Output Timing



Input Timing



$\overline{\text{HOLD}}$ Timing

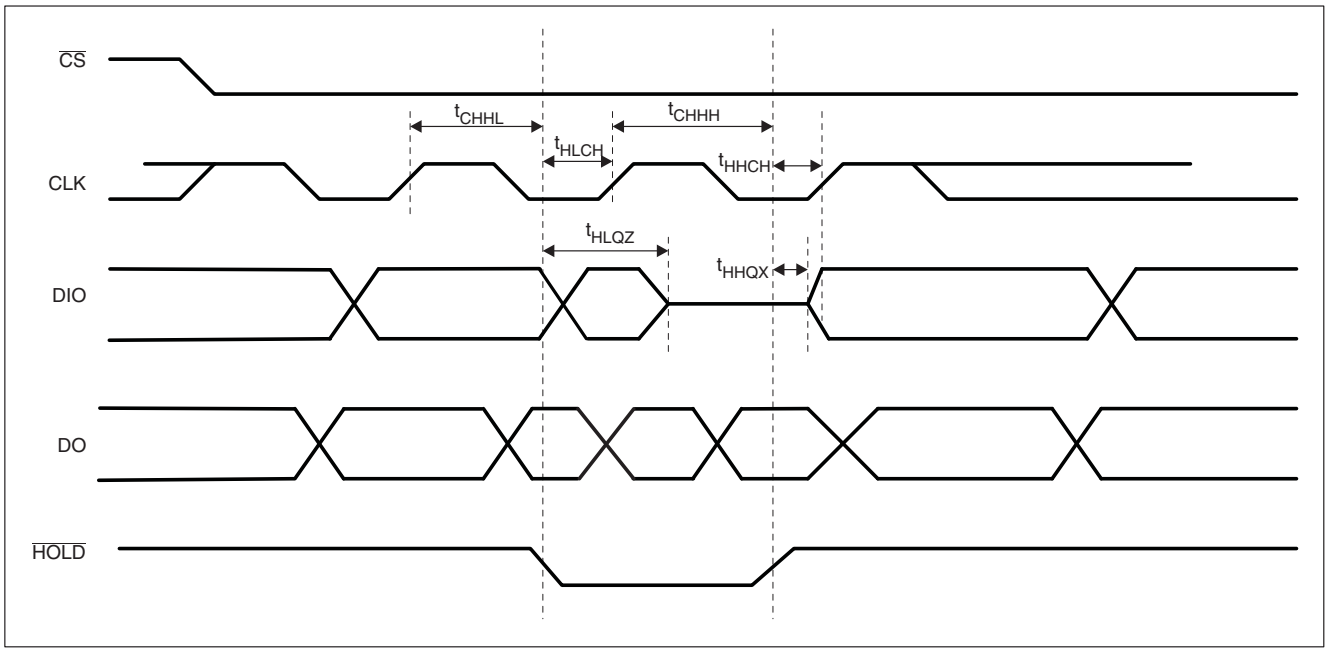


Table 5. Revision History

REVISION	SECTION(S)	COMMENT
*	All	Initial release

PACKAGING INFORMATION

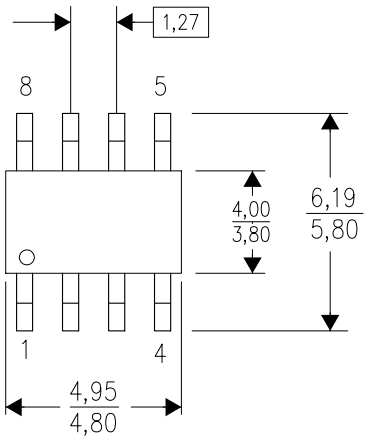
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DLPR100DWC	ACTIVE	SOIC	DWC	8	1	Pb-Free (RoHS)	POST-PLATE	Level-3-260C-168 HR	

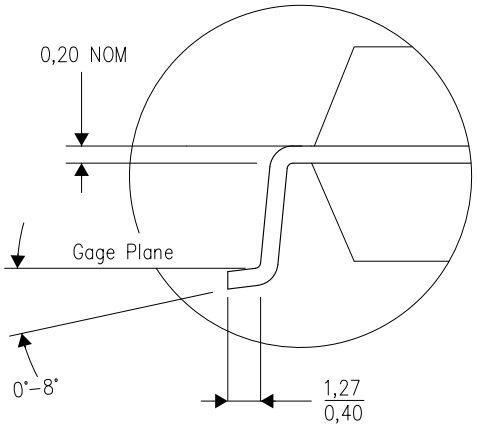
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

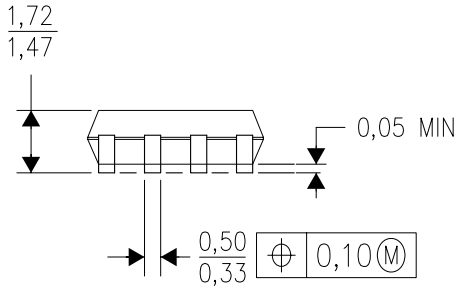
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

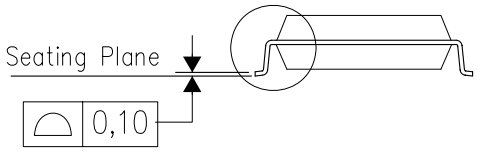
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DWC (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE









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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash protusions and should be measured from the bottom of the package.

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