

DLP® 0.17 HVGA DDR Series 210 DMD

Check for Samples: DLP1700

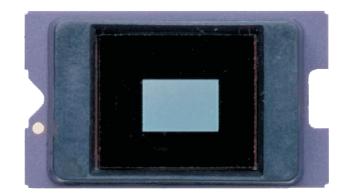
FEATURES

- 0.17-Inch Micromirror Array Diagonal
 - 480 × 320 Array of Aluminum,
 Micrometer-Sized Mirrors
 (Half-VGA Resolution)
 - 7.6-µm Micromirror Pitch
 - ±12° Micromirror Tilt Angle (Relative to Flat State)
 - Designed for Corner Illumination
- Designed for Use With Broadband Visible Light (420 nm–720 nm):
 - Window Transmission 97% (Single Pass, Through Two Window Surfaces)
 - Micromirror Reflectivity 88%
 - Array Diffraction Efficiency 86%
 - Array Fill Factor 92%
- 10-Bit, Double Data Rate (DDR) Input Data Bus
- 60 MHz Input Data Clock Rate
- Electrical Power Consumption as Low as 84 mW
- Built-In Reset Driver Circuitry
- 15.5 mm by 9 mm Package Footprint
- Package Includes a 46-pin Board-to-Board Connector

 Package Mates to a PANASONIC AXK5L46347G Socket

APPLICATIONS

- · Structured Light
- 3D Optical Measurement Systems
- Augmented Reality
- Portable Embedded Displays



DESCRIPTION

The DLP1700 Digital Micromirror Device (DMD) is a digitally controlled MOEMS (micro-opto-electromechanical system) spatial light modulator (SLM). When coupled to an appropriate optical system, the DLP1700 can be used to modulate the amplitude, direction, and/or phase of incoming (illumination) light.

Architecturally, the DLP1700 is a latchable, electrical-in/optical-out semiconductor device. This architecture makes the DLP1700 well suited for use in applications such as structured lighting, 3D optical metrology, augmented reality, microscopy, and spectroscopy. The compact physical size of the DLP1700 enables integration into portable equipment.

The DLP1700 is one of three components in the DLP 0.17 HVGA chip-set (see Figure 1). Proper function and operation of the DLP1700 requires that it be used in conjunction with the other components of the chip-set. Refer to DLP 0.17 HVGA chip-set data sheet (TI literature number DLPS017) for further details.

Electrically, the DLP1700 consists of a two-dimensional array of 1-bit CMOS memory cells, organized in a square grid of 480 memory cell columns by 320 memory cell rows. The CMOS memory array is written to on a column-by-column basis, over a 10-bit double data rate (DDR) bus. Row addressing is handled via a serial control bus. The specific CMOS memory access protocol is handled by the DLPC100 Digital Controller.

AV.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DLP is a registered trademark of Texas Instruments.



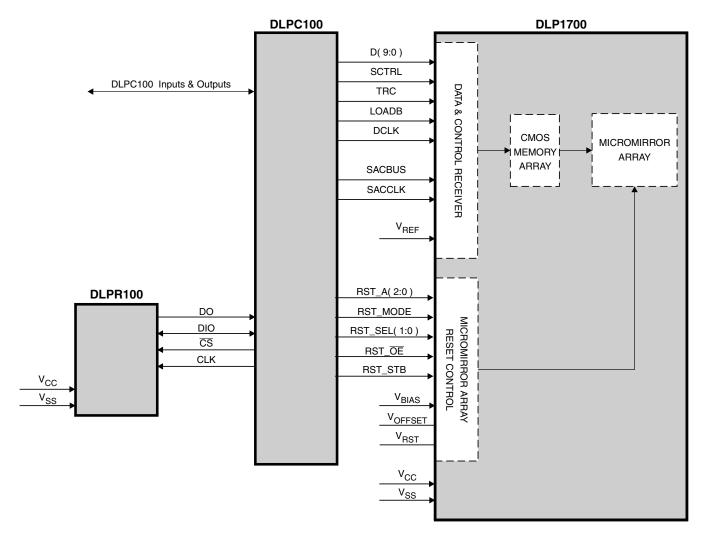


Figure 1. Block Diagram of 0.17 HVGA Chipset



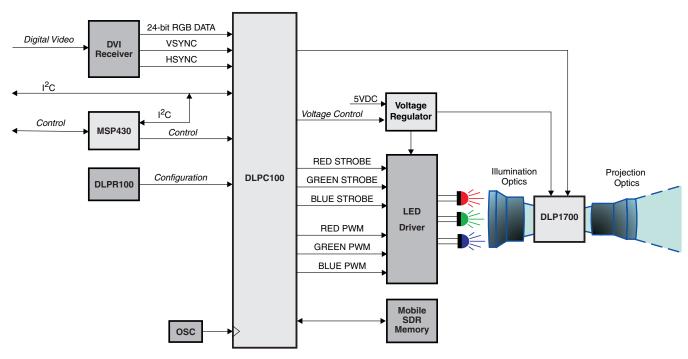


Figure 2. Typical Application

Optically, the DLP1700 consists of 153,600 highly reflective, digitally switchable, micrometer-sized mirrors ("micromirrors"), organized in a two-dimensional array of 480 micromirror columns by 320 micromirror rows (Figure 3). Each aluminum micromirror is approximately 7.6 microns in size (refer to "Micromirror Pitch" in Figure 3), and is switchable between two discrete angular positions: –12° and +12°. The angular positions are measured relative to a 0° "flat state", which is parallel to the array plane (see Figure 4). The tilt direction is perpendicular to the hinge-axis which is positioned diagonally relative to the overall array, with the "On State" landed position directed towards "Row 319, Column 0" corner of the device package (refer to "Micromirror Hinge-Axis Orientation" in Figure 3). In the field of visual displays, the 480 x 320 "pixel" resolution is referred to as "Half VGA" (HVGA).

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents. Writing a logic 1 into a memory cell will result in the corresponding micromirror switching to a $+12^{\circ}$ position. Writing a logic 0 into a memory cell will result in the corresponding micromirror switching to a -12° position.

The angular position (-12° or +12°) of the individual micromirrors changes synchronously with a micromirror "clocking pulse" (rather than being synchronous with the CMOS memory cell data update). The micromirror "clocking pulse" is referred to as a Mirror Reset. Application of the Mirror Reset results in each micromirror being electro-mechanically "latched" into the angular position dictated by the contents of the corresponding CMOS memory cell.

Operationally, updating the angular position of the micromirror array consists of first updating the contents of the CMOS memory, followed by application of a Mirror Reset to all or a portion of the micromirror array (depending upon the configuration of the system). Mirror Reset pulses are generated internally by the DLP1700 DMD, with application of the pulses being coordinated by the DLPC100 controller. Refer to SWITCHING CHARACTERISTICS timing specifications.

Around the perimeter of the 480 x 320 array of micromirrors is a uniform band of "border" micromirrors. The border micromirrors are not user-addressable. The border micromirrors land in the -12° position once power has been applied to the device. There are 14 border micromirrors on each side of the 480 by 320 active array.



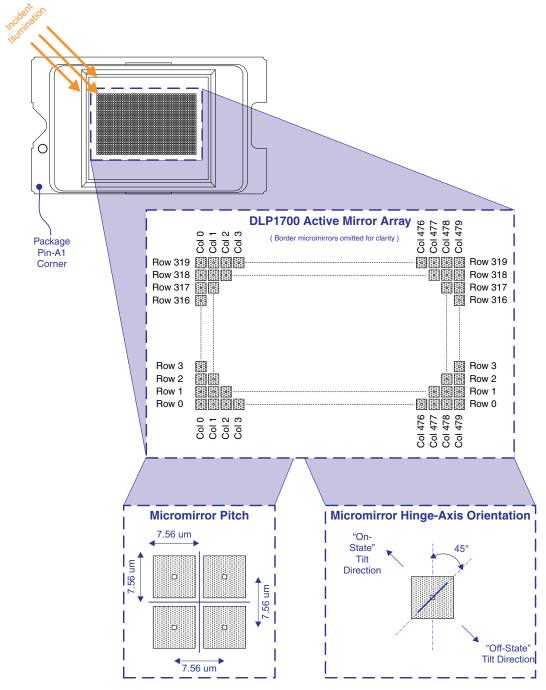


Figure 3. DMD Micromirror Array, Pitch, and Hinge-Axis Orientation



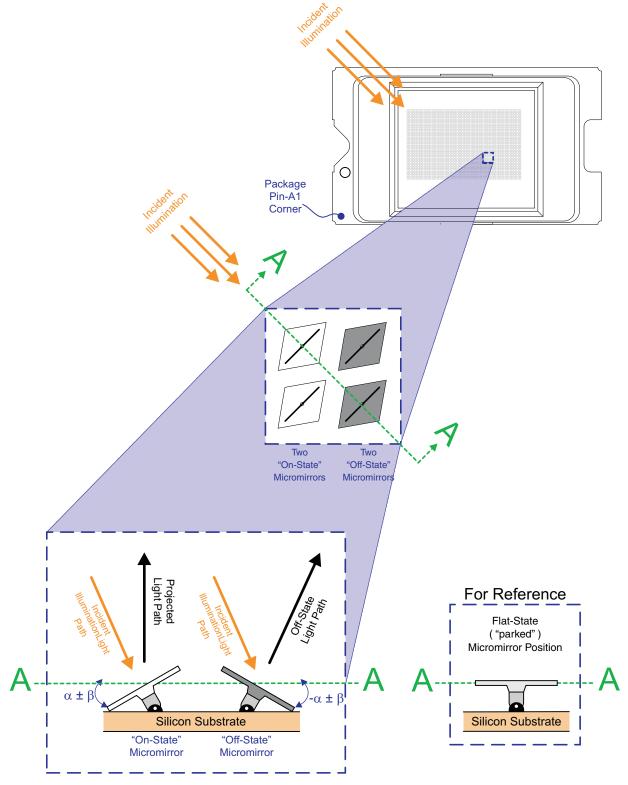


Figure 4. Micromirror Landed Positions and Light Paths



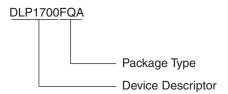
Related Documents

The following documents contain additional information related to the use of the DLP1700 device:

Table 1. Related Documents

DOCUMENT	TI LITERATURE NUMBER
DLP 0.17 HVGA Chip-Set data sheet	DLPS017
DLPC100 Digital Controller data sheet	DLPS019
DLPR100 Configurable PROM data sheet	DLPS020

Orderable Part Number



Device Marking

The device marking consists of the fields shown in Figure 5.

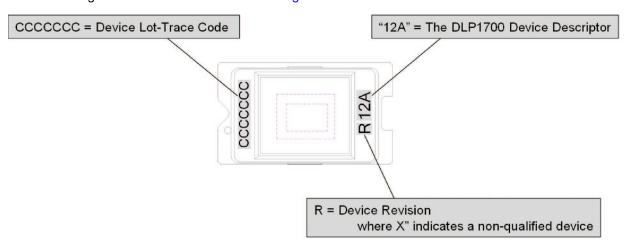


Figure 5. DMD Marking (Device Top View)



Device Terminals

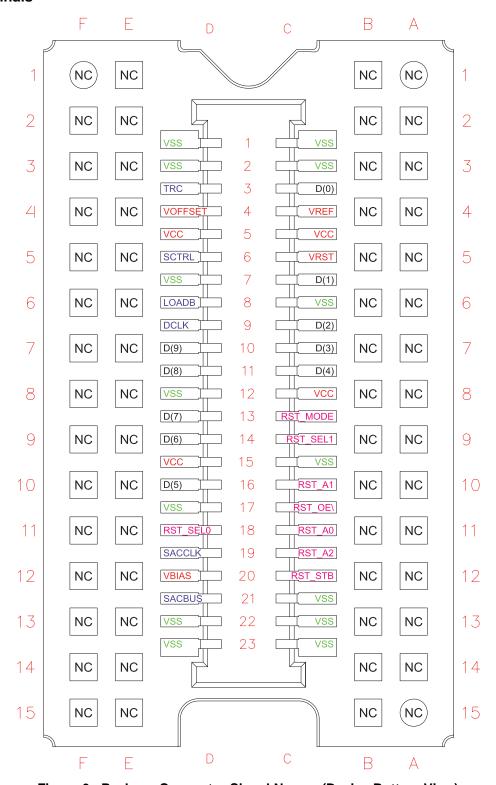


Figure 6. Package Connector Signal Names (Device Bottom View)



Table 2. Terminal Characteristics

TERMINAL NAME	PIN	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	DATA RATE	DESCRIPTION
Data Inputs					1		
D(0)	C3	Input	LVCMOS	None	DCLK	DDR	
D(1)	C7	Input	LVCMOS	None	DCLK	DDR	
D(2)	C9	Input	LVCMOS	None	DCLK	DDR	
D(3)	C10	Input	LVCMOS	None	DCLK	DDR	
D(4)	C11	Input	LVCMOS	None	DCLK	DDR	
D(5)	D16	Input	LVCMOS	None	DCLK	DDR	Input data bus
D(6)	D14	Input	LVCMOS	None	DCLK	DDR	
D(7)	D13	Input	LVCMOS	None	DCLK	DDR	
D(8)	D11	Input	LVCMOS	None	DCLK	DDR	
D(9)	D10	Input	LVCMOS	None	DCLK	DDR	
DCLK	D9	Input	LVCMOS	None	_	_	Input data bus clock
Data Control Inp	uts				1		
LOADB	D8	Input	LVCMOS	None	DCLK	DDR	Parallel data load enable
TRC	D3	Input	LVCMOS	None	DCLK	DDR	Input data toggle rate control
SCTRL	D6	Input	LVCMOS	None	DCLK	DDR	Serial control bus
SACBUS	D21	Input	LVCMOS	None	SACCLK	DDR	Serial SAC bus data
SACCLK	D19	Input	LVCMOS	None	_	_	Serial SAC bus clock
Mirror Reset Con	trol Inputs				-		
RST_A0	C18	Input	LVCMOS	None	RST_STB	SDR	
RST_A1	C16	Input	LVCMOS	None	RST_STB	SDR	Reset block address select
RST_A2	C19	Input	LVCMOS	None	RST_STB	SDR	
RST_MODE	C13	Input	LVCMOS	None	RST_STB	SDR	Reset driver mode
RST_SEL0	D18	Input	LVCMOS	None	RST_STB	SDR	5
RST_SEL1	C14	Input	LVCMOS	None	RST_STB	SDR	Reset driver output level select
RST_STB	C20	Input	LVCMOS	None	_	_	Reset driver input strobe
RST_OE	C17	Input	LVCMOS	None	_	_	Reset driver output enable
Power	l						
V _{BIAS}	D20	Power	Analog	None	_	_	Mirror reset bias voltage
V _{OFFSET}	D4	Power	Analog	None	_	_	Mirror reset offset voltage
V _{RST}	C6	Power	Analog	None	_	_	Mirror reset voltage
V _{REF}	C4	Power	Analog	None	-	-	Power supply for double data rate low voltage CMOS logic terminals
V _{CC}	C5, C12, D5, D15	Power	Analog	None	-	-	Power supply for single data rate LVCMOS logic terminals
V _{SS}	C1, C2,C8, C15, C21, C22, C23, D1, D2, D7, D12, D17, D22, D23	Power	Analog	None	-	-	Common return for all power inputs
NO_CONNECT	A1-A15, B1-B15, E1-E15, F1-F15	-	-	-	-	-	No connection (Any connection to these terminals may result in undesirable effects)



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. The Absolute Maximum Ratings are stress ratings only, and functional performance of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

	PARAMETER	CONDITIONS	MIN	MAX	UNIT
Electrica	I			<u>"</u>	
V _{CC}	Voltage applied to V _{CC} ⁽¹⁾⁽²⁾		-0.5	4	V
V _{REF}	Voltage applied to V _{REF} ⁽¹⁾⁽²⁾		-0.5	4	V
V _{OFFSET}	Voltage applied to V _{OFFSET} (1)(2)(3)		-0.5	9	V
V _{BIAS}	Voltage applied to V _{BIAS} (1)(2)(3)		-0.5	17	V
V _{RST}	Voltage applied to V _{RST} ⁽¹⁾⁽²⁾		-11	0.5	V
	Delta supply voltage V _{BIAS} – V _{OFFSET} (3)			9.0	V
	Voltage applied to all other input terminals ⁽¹⁾		-0.5	V _{REF} + 0.3	V
	Current required from a high-level output	V _{OH} = 2.4 V		-20	mA
	Current required from a low-level output	V _{OL} = 0.4 V		15	mA
Environn	nental				
_	(4)	Operating	-10	70	°C
T _C	Case temperature ⁽⁴⁾	Non-operating	-40	80	C
	Device temperature gradient ⁽⁵⁾	Operating		10	°C
	(6)	Operating		95	0/
	Local ambient relative humidity (6)	Non-operating		95	%
		< 400 nm		2	
	Illumination power density (7)	400 to 700		See ⁽⁸⁾	mW/cm ²
		> 700 nm		10	
	Electrostatic discharge immunity (9)	All pins		2000	V

- All voltages referenced to V_{SS} (ground).
- Voltages V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RST} are required for proper DMD operation.

 Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excess current draw.
- Case temperature as measured at the Thermal Test Point indicated in Figure 11.
- As measured between any two points on the exterior of the package, or as predicted between any two points inside the micromirror array cavity. Refer to the Thermal Characteristics for information related to calculating the micromirror array temperature.
- Non-condensing
- Total integrated illumination power density, above or below the indicated wavelength threshold.
- Limited only by the resulting case temperature.
- Tested in accordance with JESD22-A114-B Electrostatic Discharge (ESD) sensitivity testing Human Body Model (HBM).



RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT	
Electrica	I						
V_{REF}	LVCMOS interface supply voltage (1)(2)		1.65	1.8	1.95	V	
V_{CC}	LVCMOS logic supply voltage (1)(2)		2.25	2.5	3.6	V	
V _{OFFSET}	Mirror electrode and HVCMOS supply voltage (1)(2)(3)		8.25	8.5	8.75	V	
V_{BIAS}	Mirror electrode voltage ⁽¹⁾⁽²⁾⁽³⁾		15.5	16	16.5	V	
V_{RST}	Mirror electrode voltage ⁽¹⁾⁽²⁾		- 9.5	-10	-10.5	V	
	Delta supply voltage V _{BIAS} – V _{OFFSET} (3)				8.75	V	
V _{T+}	Positive-going threshold voltage		0.4 × V _{REF}		0.7 × V _{REF}	V	
V _T	Negative-going threshold voltage		0.3 × V _{REF}		0.6 × V _{REF}	V	
V _{hys}	Hysteresis voltage (V _{T+} – V _{T-})		0.1 × V _{REF}		0.4 × V _{REF}	V	
_	High lovel output ourrent	$V_{OH} = 2.4 \text{ V}, V_{CC} \ge 3.0 \text{ V}$			-20	A	
I _{OH}	High-level output current	$V_{OH} = 1.7 \text{ V}, V_{CC} \ge 2.25 \text{ V}$			-15	mA	
I _{OL}		$V_{OL} = 0.4 \text{ V}, V_{CC} \ge 3.0 \text{ V}$		1		mA	
	Low-level output current	$V_{OL} = 0.4 \text{ V}, V_{CC} \ge 2.25 \text{ V}$					
f _{DCLK}	DCLK clock frequency		40		60	MHz	
Mechanic	cal						
	Static load applied to the package electrical connector area ⁽⁴⁾ ⁽⁵⁾				45	N	
	Static load applied to the DMD mounting area ⁽⁶⁾ (5)				100	N	
Environn		•					
T _C	Case Temperature ⁽⁷⁾		0		70	°C	

- All voltages referenced to $V_{\mbox{\scriptsize SS}}$ (ground).
- $\begin{tabular}{lll} Voltages V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, V_{RST} are required for proper DMD operation. \\ Exceeding the recommended voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw. See the Absolute V_{CC} is a constant of the proper DMD operation. \\ \end{tabular}$ (3) Maximum Ratings for further details.
- Load should be uniformly distributed across the entire connector area. Refer to the Package Mechanical Characteristics for size and location of the connector interface area.
- See Figure 7
- Load should be uniformly distributed across the 3 datum-A surfaces. Refer to the Package Mechanical Characteristics for size and location of the datum-A surfaces.
- (7) Case temperature as measured at the Thermal Test Point indicated in Figure 11



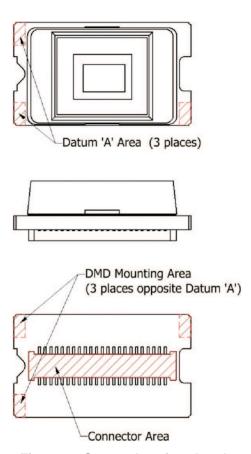


Figure 7. System Interface Loads



ELECTRICAL CHARACTERISTICS

over the range of recommended supply voltage and recommended case operating temperature (unless otherwise noted)

PARAMETER		CONDITION	CONDITIONS			UNIT	
\ /	Library Control of the control of th	V _{CC} = 3.3 V,	$I_{OH} = -34 \text{ mA}$	2.4			
V_{OH}	High-level output voltage (1)	V _{CC} = 2.5 V,	$I_{OH} = -23 \text{ mA}$	1.7		V	
	1 (1)	V _{CC} = 3.3 V,	I _{OH} = 19 mA		0.4	V	
V_{OL}	Low-level output voltage (1)	V _{CC} = 2.5 V,	I _{OH} = 16 mA		0.4	V	
l _{oz}	High impedance output current (1)	V _{CC} = 3.6 V			10	μΑ	
I _{IL}	Low-level input current ⁽¹⁾	V _{REF} = 1.95 V,	V _I = 0 V	-1.6		nA	
I _{IH}	High-level input current ⁽¹⁾	V _{REF} = 1.95 V,	$V_I = V_{REF}$		1.9	nA	
	Comment into V townsing	V 4.05.V	f _{DCLK} = 40 MHz		0.4		
I _{REF}	Current into V _{REF} terminal	$V_{REF} = 1.95 V$,	f _{DCLK} = 60 MHz		0.61		
		V 275 V	f _{DCLK} = 40 MHz		20.6		
	Command into M. Assessad	$V_{CC} = 2.75 \text{ V},$	f _{DCLK} = 60 MHz		30.8	Λ	
Icc	Current into V _{CC} terminal	V 26V	f _{DCLK} = 40 MHz		28	mA	
		$V_{CC} = 3.6 \text{ V},$	f _{DCLK} = 60 MHz		41.8		
I _{OFFSET}	Current into V _{OFFSET} terminal ⁽²⁾	V _{OFFSET} = 8.75 V			0.77	mA	
	Command into V to making (2)	$V_{BIAS} = 17 \text{ V},$ RST_ $\overline{OE} = Lc$	$RST_{\overline{OE}} = Low$		0.77	mA	
I _{BIAS}	Current into V _{BIAS} terminal ⁽²⁾	3 mirror resets in 200 µs	RST_OE = High		2.1		
I _{RST}	Current into V _{RST} terminal	V _{RST} = -12 V, 3 mirror resets	within 200 µs		0.44	mA	
<u> </u>	Danier into V	V 4.05.V	f _{DCLK} = 40 MHz		0.77	\^/	
P _{REF}	Power into V _{REF} terminal ⁽³⁾	$V_{REF} = 1.95 V$,	f _{DCLK} = 60 MHz		1.18	mW	
P _{CC}		V 075 V			56.6		
	Dower into V terminal (3)	$V_{CC} = 2.75 \text{ V},$	f _{DCLK} = 60 MHz		84.7	~\^/	
	Power into V _{CC} terminal ⁽³⁾	V 26V	f _{DCLK} = 40 MHz	10		mW	
		$V_{CC} = 3.6 \text{ V},$	f _{DCLK} = 60 MHz		150		
P _{OFFSET}	Power into V _{OFFSET} terminal ⁽³⁾	V _{OFFSET} = 8.75 V			6.7	mW	
P _{BIAS}	Dower into V terminal(3)	V _{BIAS} = 17 V,	$RST_{\overline{OE}} = Low$		14.2	m1/1/	
	Power into V _{BIAS} terminal ⁽³⁾	3 mirror resets within 200 µs	RST_OE = High		35.5	mW	
P _{RST}	Power into V _{RST} terminal ⁽³⁾	$V_{RST} = -12 V$,			5.3	mW	
C _I	Input capacitance (1)	f = 1 MHz			10	pF	
Co	Output capacitance (1)	f = 1 MHz			10	pF	

Applies to LVCMOS pins only. Exceeding the maximum allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excesses current draw. (Refer to Absolute Maximum Ratings for details)
In some applications, the total DMD heat load can be dominated by the amount of incident light energy absorbed. Refer to the Thermal

Characteristics for further details.



SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	MIN	TYP MAX	UNIT
	Setup time: DATA before rising or falling edge of DCLK	1.5		
t_{s1}	Setup time: TRC before rising or falling edge of DCLK	1.5		ns
	Setup time: SCTRL before rising or falling edge of DCLK	1.5		
t _{s2}	Setup time: LOADB low before rising edge of DCLK	1.5		ns
t_{s3}	Setup time: SAC_BUS low before rising edge of SAC_CLK	1.5		ns
	Hold time: DATA after rising or falling edge of DCLK	1.5		
t _{h1}	Hold time: TRC after rising or falling edge of DCLK	1.5		ns
	Hold time: SCTRL after rising or falling edge of DCLK	1.5		
t _{h2}	Hold time: LOADB low after falling edge of DCLK	1.5		ns
t _{h3}	Hold time: SAC_BUS low after rising edge of SAC_CLK	1.5		ns
t _{c1}	Clock cycle: DCLK	16.67	25	ns
t_{c3}	Clock cycle: SAC_CLK	16.67	25	ns
t _{w1}	Pulse width high or low: DCLK	6.67		ns
t _{w2}	Pulse width low: LOADB	6.67		ns
t _{w3}	Pulse width high or low: SAC_CLK	6.67		ns
	Rise time (20% – 80%): DCLK / SAC_CLK		2.5	
t _r	Rise time (20% – 80%): DATA / TRC / SCTRL / LOADB		2.5	ns
	Fall time (20% – 80%): DCLK / SAC_CLK		2.5	
t _f	Fall time (20% – 80%): DATA / TRC / SCTRL / LOADB		2.5	ns

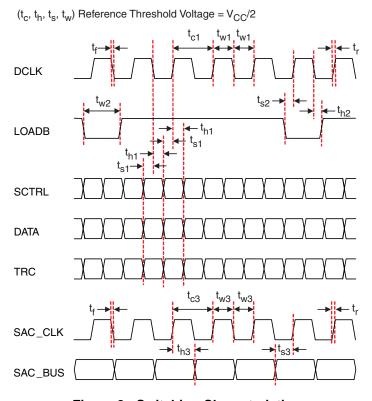


Figure 8. Switching Characteristics



LOAD CIRCUIT

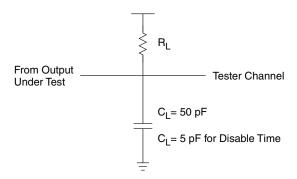


Figure 9. LVCMOS Output Test Load



POWER-UP AND POWER-DOWN PROCEDURES

CAUTION

Reliable performance of the DMD requires that the following conditions be met:

- 1) That the VCC, VREF, VOFFSET, VBIAS, and VRESET power supply inputs all be present during operation
- That the VCC, VREF, VOFFSET, VBIAS, and VRESET power supplies be sequence on and off in the manner perscribed below.

Repeated failure to adhere to the prescribed power-up and power-down procedures may affect device reliability

DMD Power Supply Power-Up Procedure

- Step 1: Power-Up V_{CC} and V_{REF} in any order
- Step 2: Wait for V_{CC} and V_{REF} to each reach a stable level within their respective recommended operating ranges.
- Step 3: Power-Up V_{BIAS}, V_{OFFSET}, and V_{RESET} in any order, provided that the maximum delta-voltage between V_{BIAS} and V_{OFFSET} is not exceeded (Refer to Absolute Maximum Ratings for details)
- Note 1: During the Power-Up procedure, the DMD's LVCMOS inputs should not be driven high until after Step 2 has been completed
- Note 2: Power supply slew rates during Power-Up are unrestricted, provided that all other conditions are met

DMD Power Supply Power-Down Procedure

- Step 1: Command the Chip-Set Controller to execute a "mirror parking sequence". Refer to the Controller data sheet (listed in Related Documents) for details.
- Step 2: Powerdown V_{BIAS}, V_{OFFSET}, and V_{RST} in any order, provided that the maximum delta voltage between V_{BIAS} and V_{OFFSET} is not exceeded. (Refer to Absolute Maximum Ratings for details)
- Step 3: Wait for V_{BIAS}, V_{OFFSET}, and V_{RST} to each discharge to a stable level within 4 V of the reference ground.
- Step 4: Powerdown V_{CC} and V_{REF} in any order.
- Note 1: During the Power-Down procedure, the DMD's LVCMOS inputs should be held at a level less than V_{REF} + 0.3 volts
- Note 2: Power supply slew rates during Power-Down are unrestricted, provided that all other conditions are met

Copyright © 2009–2011, Texas Instruments Incorporated

Submit D

Product Folder Link(s): DLP1700



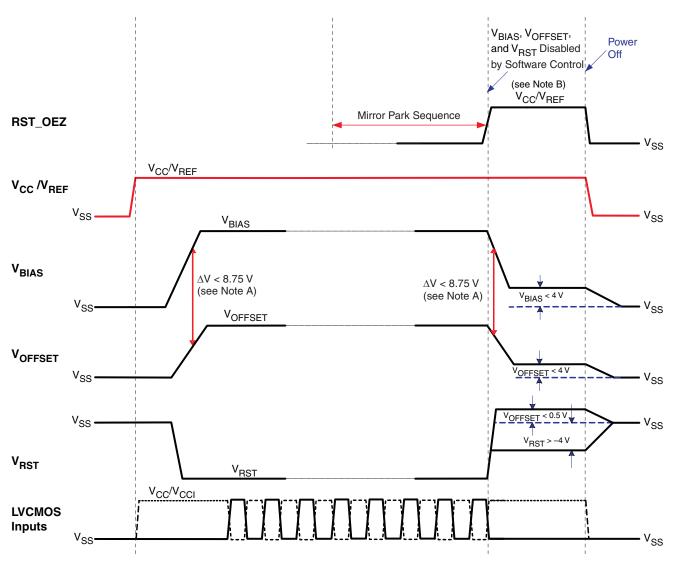


Figure 10. Power-Up / Power-Down Timing



Micromirror Array Physical Characteristics

Physical characteristics of the micromirror array are provided in Table 3. Additional details are provided in the Package Mechanical Characteristics section.

Table 3. Micromirror Array Physical Characteristics

PARAMETER	VALUE	UNITS
Number of active micromirror columns ⁽¹⁾	480	micromirrors
Number of active micromirror rows ⁽¹⁾	320	micromirrors
Micromirror pitch (1)	7.56	microns
A4:	320	micromirrors
Micromirror active array height (1)	2419.2	microns
Adii	480	micromirrors
Micromirror active array width (1)	3628.8	microns
Micromirror array border ⁽²⁾	14	mirrors/side

⁽¹⁾ See Figure 3

⁽²⁾ The mirrors that form the array border are hard-wired to tilt in the -12° ("Off") direction once power is applied to the DMD (see Figure 3 and Figure 4).



Micromirror Array Optical Characteristics

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Refer to the related Application Notes (listed in Related Documents) for guidelines.

Table 4. Micromirror Array Optical Characteristics

	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
~	Migromirror tilt angle	DMD "parked" state ⁽¹⁾⁽²⁾⁽³⁾ , see Figure 4		0		
α	Micromirror tilt angle	DMD "landed" state (1)(4)(5), see Figure 4		12		
β	Micromirror tilt angle variation (1)(4)(6)(7)(8)	See Figure 4	-1		1	degrees
	Orientation of the micromirror axis-of-rotation (9)	See Figure 3		45		
	Micromirror axis-of-rotation orientation variation (9)			See ⁽¹⁰⁾		
	Micromirror array optical efficiency ⁽¹¹⁾⁽¹²⁾	420 nm to 700 nm, with all micromirrors in the ON state		68		%
	Window material		Corn	ing Eagle	XG	
	Window refractive index	at 546.1 nm		1.5119		
	Window flatness ⁽¹³⁾	per 25 µm			4	fringes
	Window aperture			See (14)		

- (1) Measured relative to the plane formed by the overall micromirror array
- (2) "Parking" the micromirror array returns all of the micromirrors to an essentially flat (0°) state (as measured relative to the plane formed by the overall micromirror array).
- (3) When the micromirror array is "parked", the tilt angle of each individual micromirror is uncontrolled.
- (4) Additional variation exists between the micromirror array and the package datums, as shown in the Package Mechanical Characteristics section.
- (5) When the micromirror array is "landed", the tilt angle of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of "1" will result in a micromirror "landing" in an nominal angular position of "+12 degrees". A binary value of 0 will result in a micromirror "landing" in an nominal angular position of "-12 degrees".
- (6) Represents the "landed" tilt angle variation relative to the Nominal "landed" tilt angle.
- (7) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
- (8) For some applications, it is critical to account for the micromirror tilt angle variation in the overall System Optical Designs. With some System Optical Designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some System Optical Designs, the micromirror tilt angle variation between devices may result in colorimetry variations and/or system contrast variations.
- (9) Measured relative to the package datums "B" and "C", shown in the Package Mechanical Characteristics section.
- (10) Variation of the micromirror axis-of-rotation is subject to the location tolerance of the active array, as shown in the Package Mechanical Characteristics section.
- (11) The minimum or maximum DMD optical efficiency observed in a specific application depends on numerous application-specific design variables, such as:
 - (a) Illumination wavelength, bandwidth/line-width, degree of coherence
 - (b) Illumination angle, plus angle tolerance
 - (c) Illumination and projection aperture size, and location in the system optical path
 - (d) Illlumination overfill of the DMD micromirror array
 - (e) Aberrations present in the illumination source and/or path
 - (f) Aberrations present in the projection path
 - (g) Etc.

The specified nominal DMD optical efficiency is based on the following use conditions:

- (a) Visible illumination (420 nm 700 nm)
- (b) Input illumination optical axis oriented at 24° relative to the window normal
- (c) Projection optical axis oriented at 0° relative to the window normal
- (d) f/3.0 illumination aperture
- (e) f/2.4 projection aperture

Based on these use conditions, the nominal DMD optical efficiency results from the following four components:

- (a) Micromirror array fill factor: nominally 92.5%
- (b) Micromirror array diffraction efficiency: nominally 86%
- (c) Micromirror surface reflectivity: nominally 88%
- (d) Window transmission: nominally 97% (single pass, through two surface transitions)
- (12) Does not account for the effect of micromirror switching duty cycle, which is application dependant. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, the projection aperture size, and the micromirror array update rate.
- (13) At a wavelength of 632.8 nm.
- (14) Refer to the Package Mechanical Characteristics for details regarding the size and location of the window aperture.



Thermal Characteristics

Achieving optimal DMD performance requires proper management of the maximum DMD case temperature, the maximum temperature of any individual micromirror in the active array, the maximum temperature of the window aperture, and the temperature gradient between any two points on or within the package.

Refer to the Absolute Maximum Ratings and Recommended Operation Conditions for applicable temperature limits.

Case Temperature

The temperature of the DMD case can be measured directly. For consistency, a Thermal Test Point location is defined, as shown in Figure 11.

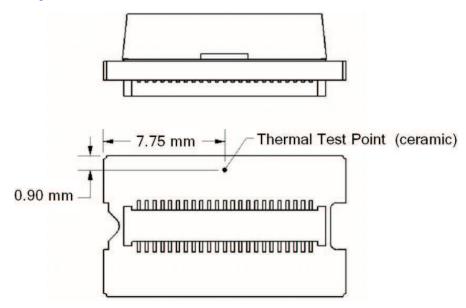


Figure 11. Thermal Test Point Location

Copyright © 2009–2011, Texas Instruments Incorporated



Package Electrical Characteristics

The package interconnect trace lengths are provided in Table 5. Refer to the DLP 0.17 HVGA Chip-Set Data Sheet (TI literature number DLPS017) for details regarding signal integrity considerations for end-equipment designs.

Table 5. Package Trace Length Data

PIN NO.	PIN NAME	PACKAGE TRACE LENGTH (µm)			
C1	V _{SS}				
C2	V _{SS}	_			
C3	D(0)	776			
C4	V_{REF}	_			
C5	V _{CC}	_			
C6	V _{RST}	_			
C7	D(1)	2903			
C8	V _{SS}	_			
C9	D(2)	4145			
C10	D(3)	4596			
C11	D(4)	5472			
C12	V _{CC}	_			
C13	RST_MODE	5292			
C14	RST_SEL1	4536			
C15	V _{SS}				
C16	RST_A1	3418			
C17	RST_ OE	3839			
C18	RST_A0	3278			
C19	RST_A2	2525			
C20	RST_STB	3024			
C21	V _{SS}	_			
C22	V _{SS}	_			
C23	V _{SS}	_			
D1	V _{SS}	_			
D2	V _{SS}	_			
D3	TRC	632			
D4	V_{OFFSET}	_			
D5	V _{CC}	_			
D6	SCTRL	2513			
D7	V_{SS}	_			
D8	LOADB	3270			
D9	DCLK	4173			
D10	D(9)	4471			
D11	D(8)	5335			
D12	V_{SS}	_			
D13	D(7)	6171			
D14	D(6)	6917			
D15	V _{CC}	_			
D16	D(5)	8145			
D17	V_{SS}	_			
D18	RST_SEL0	3564			
D19	SACCLK	4515			



Table 5. Package Trace Length Data (continued)

PIN NO.	PIN NAME	PACKAGE TRACE LENGTH (μm)
D20	V _{BIAS}	_
D21	SACBUS	716
D22	V _{SS}	_
D23	V _{SS}	_

Package Mechanical Characteristics

The mechanical characteristics of the DLP1700 are specified on the following pages.



Table 6. Revision History

REVISION	SECTION(S)	COMMENT				
*	All	Initial release				
Α	All	Refined content				
В	Table 4	Added table note "At a wavelength of 632.8 nm"				



PACKAGE OPTION ADDENDUM

10-Oct-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
DLP1700FQA	ACTIVE	LCCC	FQA	46	1	Green (RoHS & no Sb/Br)	Call TI	Level-1-NC-NC	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

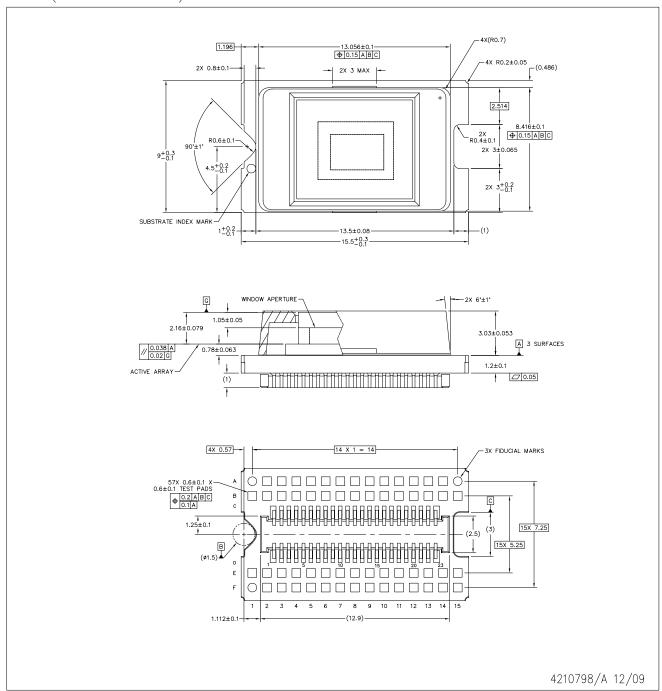
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

FQA (R-CLGA-N46)

CERAMIC LAND GRID ARRAY PACKAGE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.

- B. This drawing is subject to change without notice.
- C. Pins shall be gold plated.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products Applications

Audio www.ti.com/audio Communications and Telecom www.ti.com/communications **Amplifiers** amplifier.ti.com Computers and Peripherals www.ti.com/computers dataconverter.ti.com Consumer Electronics www.ti.com/consumer-apps **Data Converters DLP® Products** www.dlp.com **Energy and Lighting** www.ti.com/energy DSP dsp.ti.com Industrial www.ti.com/industrial Clocks and Timers www.ti.com/clocks Medical www.ti.com/medical

Interface interface.ti.com Security www.ti.com/security

Logic Space, Avionics and Defense www.ti.com/space-avionics-defense

Power Mgmt power.ti.com Transportation and Automotive www.ti.com/automotive
Microcontrollers Microcontroller.ti.com Video and Imaging www.ti.com/video

RFID <u>www.ti-rfid.com</u>

OMAP Mobile Processors www.ti.com/omap

Wireless Connectivity www.ti.com/wirelessconnectivity

TI E2E Community Home Page <u>e2e.ti.com</u>