SN74CBT162292 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS SCDS052E – MARCH 1998 – REVISED OCTOBER 2000

- Member of Texas Instruments' Widebus™ Family
- TTL-Compatible Control Input Levels
- Isolation Under Power-Off Conditions
- Make-Before-Break Feature
- Internal 500-Ω Pulldown Resistors to Ground
- A-Port Inputs/Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Latch-Up Performance Exceeds 250 mA Per JESD 17

description

The SN74CBT162292 is a 12-bit 1-of-2 high-speed TTL-compatible FET multiplexer/ demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1, and R_{INT} is connected to port B2. When S is high, port A is connected to port B2, and R_{INT} is connected to port B1.

The A-port inputs/outputs include equivalent $25-\Omega$ series resistors to reduce overshoot and undershoot.

DGG, DGV, OR DL PACKAGE (TOP VIEW)						
S L L L 1A L L 2A L L NC A L SA L G ND L G A A L SA L	(TOP V) 1 2 3 4 5 6 7 8 9 10 11	56 55 54 53 52 51 50 49 48 47 46	NC NC 1B1 1B2 2B1 2B2 3B1 3B1 GND 3B2 4B1 4B2			
NC 6A NC 7A	12 13 14 15	45 44 43 42	5B1 5B2 6B1 6B2			
NC V _{CC} 8A GND	16 17 18 19	41 40 39 38	7B1 7B2 8B1 GND			
NC L 9A C 10A C 10A C 11A C NC C 12A C	20 21 22 23 24 25 26 27	 37 36 35 34 33 32 31 30 	882 981 982 1081 1082 1181 1182 1281			
NCL	28	29	12B2			

NC - No internal connection

ORDERING INFORMATION

т _А	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SSOP – DL	Tube	SN74CBT162292DL	CBT162292
–40°C to 85°C	330F - DL	Tape and reel	SN74CBT162292DLR	CB1102292
-40 C 10 85 C	TSSOP – DGG	Tape and reel	SN74CBT162292DGGR	CBT162292
	TVSOP – DGV	Tape and reel	SN74CBT162292DGVR	CY2292

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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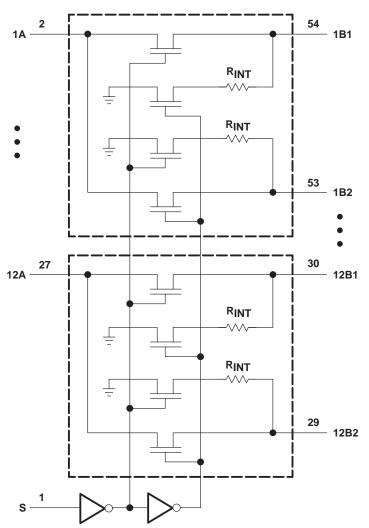
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SCDS052E - MARCH 1998 - REVISED OCTOBER 2000

FUNCTION TABLE							
INPUT S	FUNCTION						
L	A port = B1 port R _{INT} = B2 port						
н	A port = B2 port R _{INT} = B1 port						

logic diagram (positive logic)





SCDS052E - MARCH 1998 - REVISED OCTOBER 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5	V to 7 V
Input voltage range, V _I (see Note 1)		0.5	V to 7 V
Continuous channel current			128 mA
Input clamp current, I _{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package		64°C/W
	DGV package		48°C/W
	DL package		56°C/W
Storage temperature range, T _{stg}		-65°C 1	to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
ТА	Operating free-air temperature	-40	85	°C
-			-	

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDITION	MIN	TYP‡	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	lı = –18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_{I} = V_{CC} \text{ or } GND$				±5	μΑ
l _{off}		$V_{CC} = 0,$	$V_{I} \text{ or } V_{O} = 0 \text{ to } 7 \text{ V}$				10	μΑ
ICC	-	V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC} \text{ or } GND$			3	μΑ
∆ICC§	Control input	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control input	V _I = 3 V or 0				3.5		pF
C _{io}		$V_{CC} = 0,$	$V_{O} = 3 V \text{ or } 0$			8		pF
		$V_{CC} = 4 V,$ TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lj = 15 mA		38	55	
ron¶			$V_{I} = 0$	lı = 45 mA		39	63	Ω
		V _{CC} = 4.5 V	vI=0	I _I = 30 mA		37	55	
			V _I = 2.4 V,	lı = 15 mA		37	55	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SCDS052E - MARCH 1998 - REVISED OCTOBER 2000

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF, (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} :	= 4 V	= V _{CC} ± 0.	= 5 V 5 V	UNIT
		(001101)	MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A		1.9		1.85	ns
ten	S	A or B	1	10.7	1	9.5	ns
^t dis	S	A or B	1	10.9	1	9.7	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

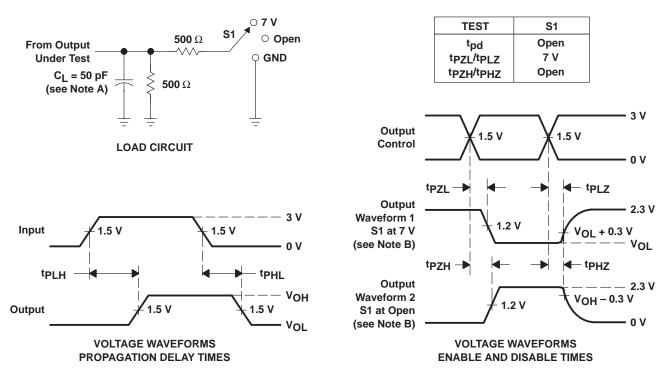
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF, (unless otherwise noted) (see Figure 1)

PARAMETER	DESCRIPTION	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
		MIN	MAX	MIN	MAX	
t _{mbb} ‡	Make-before-break time	0	2	0	2	ns

[‡]The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.



SCDS052E - MARCH 1998 - REVISED OCTOBER 2000



PARAMETER MEASUREMENT INFORMATION

- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when connected to the internal 500-Ω pulldown resistor. Waveform 2 is for an output with internal conditions such that the output is high except when connected to the internal 500-Ω pulldown resistor.
 - C. All pulse inputs and DC inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} . $Z = R_{INT} = 500 \Omega$.
 - F. t_{PZL} and t_{PZH} are the same as t_{en} . $Z = R_{INT} = 500 \Omega$.
 - G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74CBT162292DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT162292DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT162292DGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT162292DGVRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT162292DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT162292DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT162292DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT162292DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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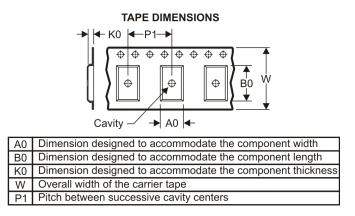
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT162292DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CBT162292DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

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PACKAGE MATERIALS INFORMATION

29-Jul-2009



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT162292DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74CBT162292DGVR	TVSOP	DGV	56	2000	346.0	346.0	41.0

MECHANICAL DATA

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

DL (R-PDSO-G**)



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



MECHANICAL DATA

PLASTIC SMALL-OUTLINE

MPDS006C - FEBRUARY 1996 - REVISED AUGUST 2000

DGV (R-PDSO-G**)

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153

14/16/20/56 Pins – MO-194



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