1.4 W/CH STEREO CLASS-D AUDIO SUBSYSTEM WITH DirectPath™ HEADPHONE AMPLIFIER AND 2:1 INPUT MUX

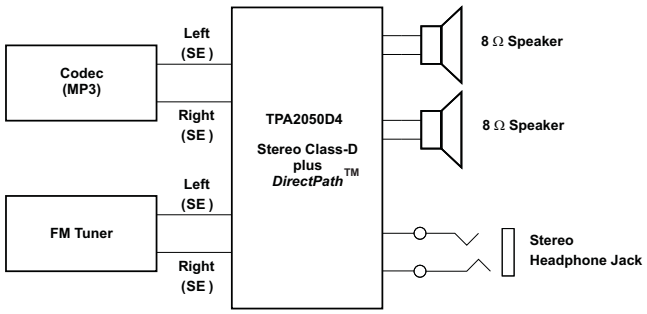
FEATURES

- **Stereo Class-D Amp:**
  - **1.4 W into 8 Ω from 5.0 V (10% THD + N)**
  - **1.25 W into 8 Ω from 5.0 V (1% THD + N)**
- ***DirectPath*™ Stereo Headphone Amplifier**
  - **No Output Capacitors Required**
- **Gain Select for Headphone Amplifier**
- **Eight Programmable Maximum Headphone Voltage Limits**
- **Two Single-Ended or One Differential Stereo Input**
- **2:1 Input MUX with Mode Control**
- **32-Step Volume Control for Both Input Channels**
- **Independent Shutdown for Headphone and Class-D Amplifiers**
- **Short-Circuit and Thermal-Overload Protection**
- **±8 kV HBM ESD Protection on Headphone Outputs**
- **I^2C™ Interface**
- **25-Ball 2,61 mm × 2,61 mm WCSP**

APPLICATIONS

- **Smart Phones / Cellular Phones**
- **Laptop Computers**
- **Portable Gaming**
- **Portable Media Players**

SIMPLIFIED SYSTEM BLOCK DIAGRAM



DESCRIPTION

The TPA2050D4 features a stereo Class-D power amplifier along with a stereo DirectPath™ headphone amplifier. The TPA2050D4 has two stereo single-ended (SE) inputs that can be configured as one stereo differential input. Both input channels have a 32-step volume control and the DirectPath headphone amplifier has a 4-level gain control for coarse volume adjustment. All amplifiers have output short-circuit and thermal- overload protection.

The Class-D amplifiers deliver 1.25 W into 8 Ω at 1% THD from a 5.0 V supply, and 700 mW from 3.6 V. The DirectPath headphone amplifier features an output voltage limiter to reduce the maximum output power to one of seven possible limits. The voltage limiter is programmed through the I^2C interface.

DirectPath eliminates the need for external DC-blocking output capacitors to the headphones. The built-in charge pump creates a negative supply voltage for the headphone amplifier, allowing a 0-V DC bias at the output.

The DirectPath headphone amplifier gains are 0 dB (default), –6 dB, –12 dB, and –20 dB, selected through the I2C interface. This allows the headphone volume to be different from the loudspeaker volume if both are used simultaneously.

The TPA2050D4 has a 2:1 input MUX for audio source selection. The MUX has mode control which directs the input-to-output signal path. Mode and gain controls operate from a 1.8 V compatible I^2C interface.

The voltage supply range for both the Class-D amplifiers and the headphone charge pump is 2.5 V to 5.5 V. The Class-D amplifiers use a combined 7 mA and the headphone amplifier uses 10 mA of typical quiescent current. Total supply current reduces to less than 2μA.

The TPA2050D4YZK is available in a 25-ball 2.61 mm × 2.61 mm WCSP package.

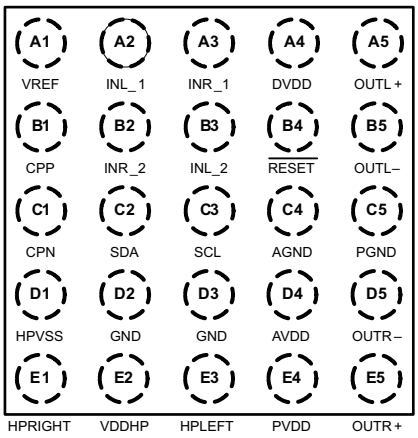
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGED DEVICES(1)	PART NUMBER(2)
–40°C to 85°C	25-ball, 2,61 mm × 2,61 mm WCSP (+0.01/-0.09 mm tolerance)	TPA2050D4YZKR
	25-ball, 2,61 mm × 2,61 mm WCSP (+0.01/-0.09 mm tolerance)	TPA2050D4YZKT

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) The YZK packages are only available taped and reeled. The suffix R indicates a reel of 3000, the suffix T indicates a reel of 250.

DEVICE PINOUT



FUNCTIONAL BLOCK DIAGRAM

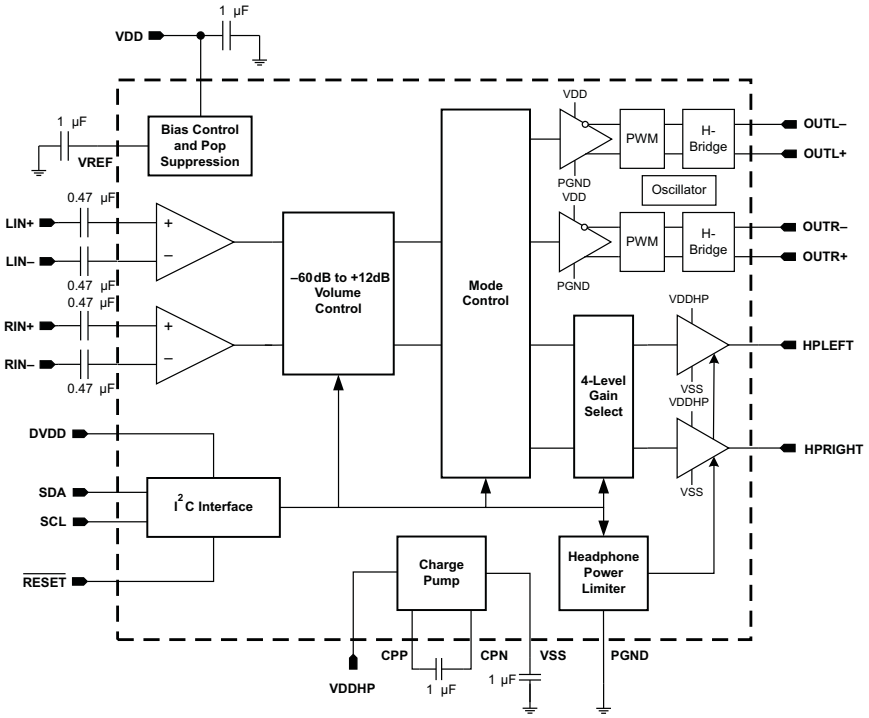


Figure 1. Differential Input Mode

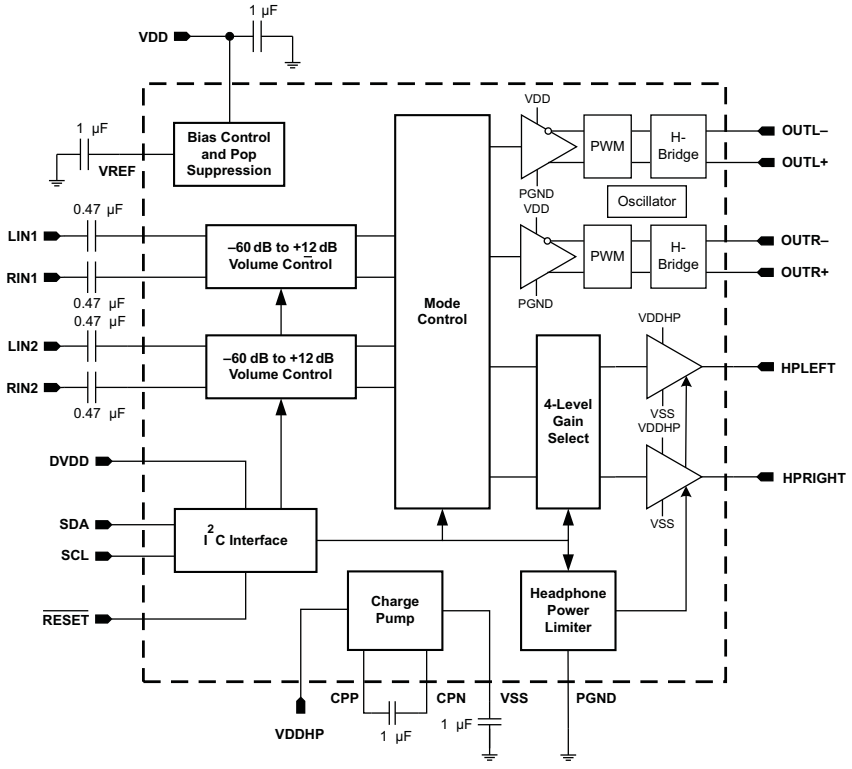


Figure 2. Single-Ended (SE) Input Mode

TERMINAL FUNCTIONS

TERMINAL		INPUT/ OUTPUT/ POWER (I/O/P)	DESCRIPTION
NAME	BALL WCSP		
OUTL+	A5	O	Left speaker positive output; connect to + terminal of loudspeaker
DVDD	A4	P	I2C supply voltage; connect to 1.8V digital supply
INR_1	A3	I	Channel 1 right input (SE-In mode); Left– input (Diff-In mode); connect to ground through 0.47 μF capacitor if unused
INL_1	A2	I	Channel 1 left input (SE-In mode); Left+ input (Diff-In mode); connect to ground through 0.47 μF capacitor if unused
VREF	A1	I	1.65 V reference voltage; connect a 1 μF capacitor to ground
OUTL–	B5	O	Left speaker negative output; connect to negative terminal of loudspeaker
$\overline{\text{RESET}}$	B4	I	Set to logic low to shut device down and return all I2C register to default state; I2C can only be programmed once $\overline{\text{RESET}}$ returns to logic high
INL_2	B3	I	Channel 2 left input (SE-In mode); Right+ input (Diff-In mode); connect to ground through 0.47 μF capacitor if unused
INR_2	B2	I	Channel 2 right input (SE-In mode); Right– input (Diff-In mode); connect to ground through 0.47 μF capacitor if unused
CPP	B1	P	Charge pump flying capacitor positive terminal; connect positive side of capacitor between CPP and CPN
PGND	C5	P	Class-D ground; connect to ground
AGND	C4	P	Analog ground; connect to ground
SCL	C3	I/O	I2C clock input
SDA	C2	I/O	I2C data input
CPN	C1	P	Charge pump flying capacitor negative terminal; connect negative side of capacitor between CPP and CPN
OUTR–	D5	O	Right speaker negative output; connect to negative terminal of loudspeaker
AVDD	D4	P	Supply voltage
GND	D3	I	Connect to ground
GND	D2	I	Connect to ground
HPVSS	D1	P	Negative supply generated by the charge pump; connect a 1μF capacitor to ground to reduce voltage ripple
OUTR+	E5	O	Right speaker positive output; connect to positive terminal of loudspeaker
PVDD	E4	P	Supply voltage
HPLEFT	E3	O	Headphone left channel output
VDDHP	E2	P	Headphone charge pump supply voltage
HPRIGHT	E1	O	Headphone right channel output

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range, T_A = 25°C (unless otherwise noted)

			VALUE	UNIT
	Supply voltage,	VDDHP, PVDD, AVDD	–0.3 to 6.0	V
		DVDD	-0.3 to 3.6	V
V_I	Input voltage	INL_1, INL_2, INR_1, INR_2	–0.3 to VDD + 0.3	V
		SDA, SCL, $\overline{\text{RESET}}$	-0.3 to DVDD + 0.3	V
	Output continuous total power dissipation		See Dissipation Rating Table	
T_A	Operating free-air temperature range		–40 to 85	°C
T_J	Operating junction temperature range		–40 to 150	°C
T_{stg}	Storage temperature range		–65 to 150	°C
ESD	Electrostatic discharge, HBM	OUTL+, OUTL–, OUTR+, OUTR–	2 k	V
		HPLEFT and HPRIGHT	8 k	V
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	T_A < 25°C	DERATING FACTOR	T_A = 70°C	T_A = 85°C
YZK (WCSP)	1.12 W	9 mW/°C	720 mW	585 mW

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Class-D supply voltage, PVDD		2.5	5.5	V
	Charge pump supply voltage, VDDHP		2.5	5.5	V
	I2C supply voltage, DVDD		1.7	1.95	V
V_{IH}	High-level input voltage	SDA, SCL, $\overline{\text{RESET}}$	1.3		V
V_{IL}	Low-level input voltage	SDA, SCL, $\overline{\text{RESET}}$		0.3	V
T_A	Operation free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Power supply rejection ratio (Class-D amplifiers)	V_{DD} = 2.5 V to 5.5 V, Single-ended mode	48	75		dB
DC Power supply rejection ratio (headphone amplifiers)	V_{DD} = 2.5 V to 5.5 V, Single-ended mode	60	80		dB
High-level input current (SDA, SCL, $\overline{\text{RESET}}$)				1	µA
Low-level input current (SDA, SCL, $\overline{\text{RESET}}$)				1	µA
Supply current	V_{DD} = 5.5 V, Class-D and Headphone ampifiers active, no load		15.8	20	mA
	V_{DD} = 4.2 V, Class-D active, Headphone deactivated, no load		7.5	10.5	mA
	V_{DD} = 4.2 V, Headphone active, Class-D deactivated, no load		10	13.5	mA
	V_{DD} = 2.5 V to 5.5 V, SWS=1 or $\overline{\text{RESET}}$ ≤ 0.3 V (shutdown mode)		0.15	2	µA

TIMING CHARACTERISTICS

For I^2C Interface Signals Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLN}	Frequency, SCL	No wait states			400	kHz
$t_{W(H)}$	Pulse duration, SCL high		0.6			µs
$t_{W(L)}$	Pulse duration, SCL low		1.3			µs
t_{su1}	Setup time, SDA to SCL		100			ns
t_{h1}	Hold time, SCL to SDA		10			ns
$t_{(buf)}$	Bus free time between stop and start condition		1.3			µs
t_{su2}	Setup time, SCL to start condition		0.6			µs
t_{h2}	Hold time, start condition to SCL		0.6			µs
t_{su3}	Setup time, SCL to stop condition		0.6			µs

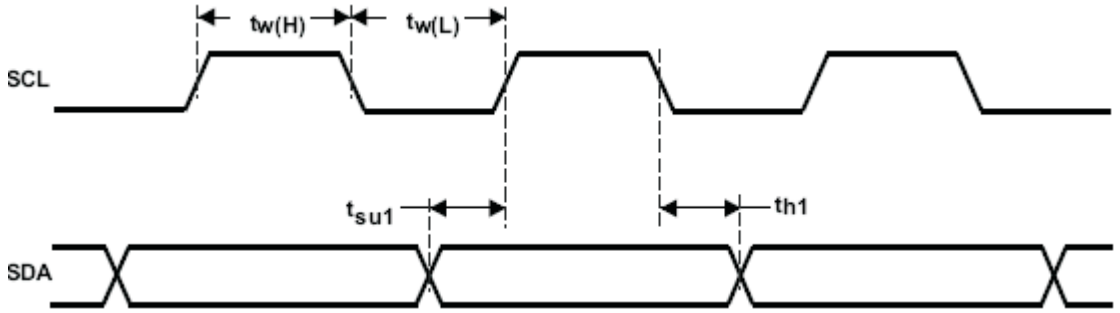


Figure 3. SCL and SDA Timing

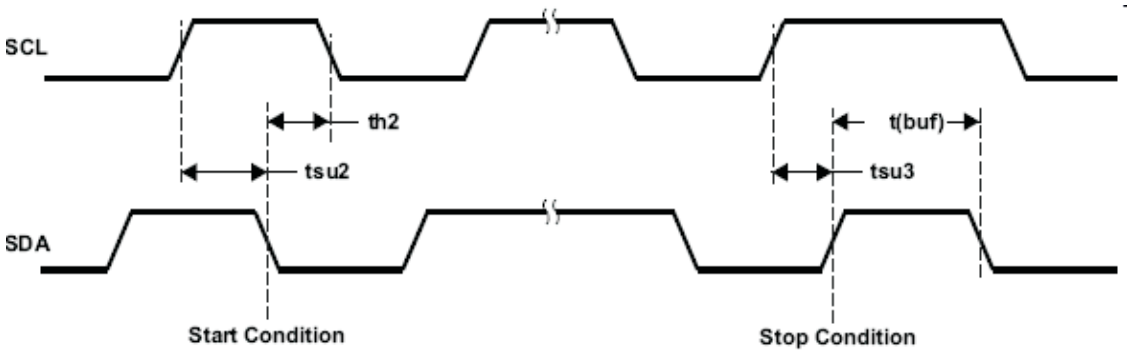


Figure 4. Start and Stop Conditions Timing

DEVICE RESET

Apply logic low to the $\overline{\text{RESET}}$ pin to deactivate the TPA2050D4 and return all I^2C registers to their default state. This clears the LIM_Lock bit to logic low, allowing changes to the headphone output limiter byte. Refer to the Register Map section for a complete list of default states. The I2C registers cannot be programmed until $\overline{\text{RESET}}$ returns to logic high. $\overline{\text{RESET}}$ requires a 1 ms minimum hold time at logic low for a valid reset command.

On power-up, ensure that the DVDD and VDDHP voltages have settled and DVDD is at least 1.7V before setting $\overline{\text{RESET}}$ to logic high. The TPA2050D4 activates in soft shutdown mode, SWS bit at logic high.

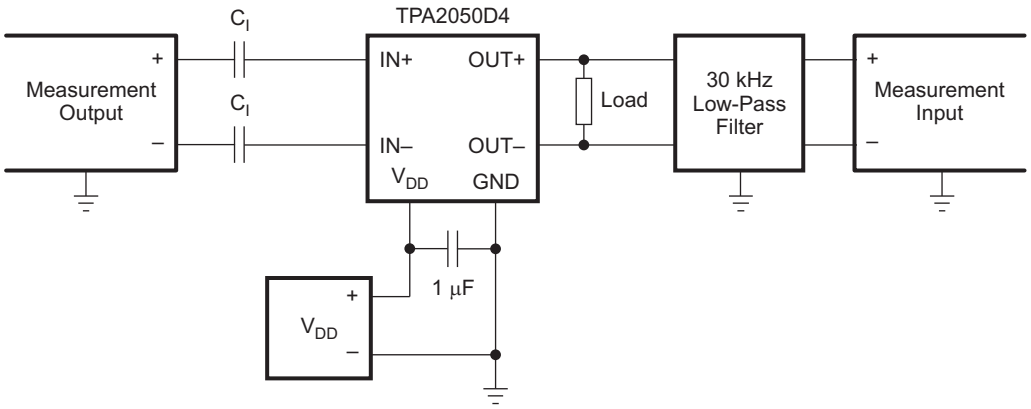
OPERATING CHARACTERISTICS

V_{DD} = 3.6 V, T_A = 25°C, $R_{SPEAKER}$ = 8 Ω + 33 µH, $R_{HEADPHONES}$ = 16 Ω, Volume = 6 dB, HP Gain = 0 dB, MODE[2:0] = 001 (single-ended mode)(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER AMPLIFIER						
P_O	Speaker output power	THD = 1%, V_{DD} = 3.6 V, f = 1 kHz		700		mW
		THD = 10%, V_{DD} = 3.6 V, f = 1 kHz		860		mW
		THD = 1%, V_{DD} = 4.2 V, f = 1 kHz		940		mW
V_{OS}	Offset Voltage	V_{DD} = 5.5 V, Volume = 0 dB	-13	5	13	mV
	Output impedance in shutdown			2		kΩ
SNR	Signal-to-noise ratio	P_O = 600 mW;		90		dB
E_n	Noise output voltage	Volume = 0 dB; A-weighted		19.4		μV_{RMS}
THD+N	Total harmonic distortion plus noise	V_{DD} = 5.0 V, PO = 1 W, f = 1 kHz		0.22		%
		V_{DD} = 3.6 V, PO = 0.6 W, f = 1 kHz		0.27		%
k_{SVR}	AC-Power supply rejection ratio	200 mV_{pp} ripple, f = 217 Hz, Volume = 0 dB		-77.7		dB
		200 mV_{pp} ripple, f = 4 kHz, Volume = 0 dB		-60.3		dB
	Thermal shutdown	Threshold		155		°C
		Hysteresis		35		°C
	Output short-circuit protection			2.4		A
f_{CLK}	Class-D switching frequency		250	300	350	kHz
ΔA_V	Gain matching	Between left and right channels		0.1		dB
HEADPHONE AMPLIFIER						
P_O	Headphone output power(1) (Outputs in Phase)	THD = 1%, V_{DD} = 5.0 V, HP_Vout[2:0] = 000		145		mW
		THD = 1%, V_{DD} = 3.0 V, HP_Vout[2:0] = 000		79		
V_O	Maximum headphone output voltage	THD = 10 %, HP_VOUT[2:0] = 111		0.14		V_{RMS}
		THD = 10 %, HP_VOUT[2:0] = 100		0.23		
V_{OS}	Offset Voltage	V_{DD} = 5.5 V, Volume = 0 dB	-3.5	0.5	3.5	mV
	Output impedance in shutdown			30		Ω
SNR	Signal-to-noise ratio	P_O = 50 mW;		90		dB
E_n	Noise output voltage	Volume = 0 dB; A-weighted, V_{DD} = 5.0 V		12		μV_{RMS}
THD+N	Total harmonic distortion plus noise(1)	P_O = 20 mW into 16 Ω, V_{DD} = 3.6 V, f = 1 kHz		0.005		%
		P_O = 50 mW into 32 Ω, V_{DD} = 5.0 V, f = 1 kHz		0.0067		%
k_{SVR}	AC-Power supply rejection ratio	200 mV_{pp} ripple, f = 217 Hz, Volume = 0 dB		-78.5		dB
		200 mV_{pp} ripple, f = 4 kHz, Volume = 0 dB		-75.6		dB
	Output short-circuit protection			200		mA
f_{OSC}	Charge pump switching frequency			300		kHz
ΔA_V	Gain matching	Between Left and Right channels		0.1		dB
INPUT SECTION						
R_{IN}	Input impedance	Volume = 12 dB	11	14.7		kΩ
V_{REF}	Reference voltage	V_{DD} = 3.6 V, all active modes		1.65		V
	Start-up time from shutdown			8.25		ms

(1) Per output channel

TEST SET-UP FOR GRAPHS



(1) All measurements were taken with a 1-µF C_I (unless otherwise noted.)

(2) A 33-µH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.

(3) The 30-kHz low-pass filter is required, even if the analyzer has an internal low-pass filter. An RC low-pass filter (1 kΩ 4.7 nF) is used on each output for the data sheet graphs.

TYPICAL CHARACTERISTIC GRAPHS

C_I= 1µF, C_{bypass}= 1µF

TOTAL HARMONIC DISTORTION+NOISE (SP) VS FREQUENCY

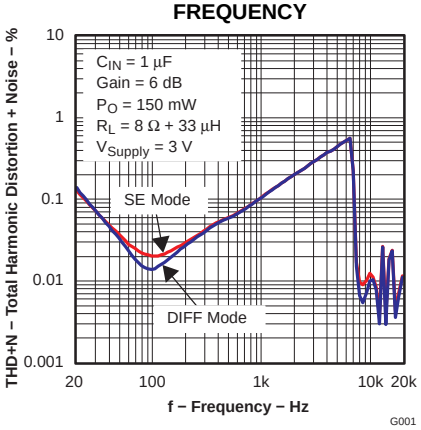


Figure 6.

TOTAL HARMONIC DISTORTION+NOISE (SP) VS FREQUENCY

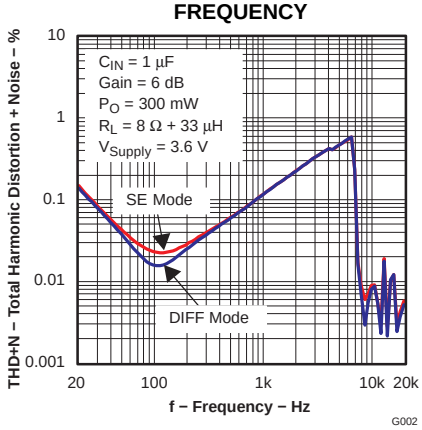


Figure 7.

TOTAL HARMONIC DISTORTION+NOISE (SP) VS FREQUENCY

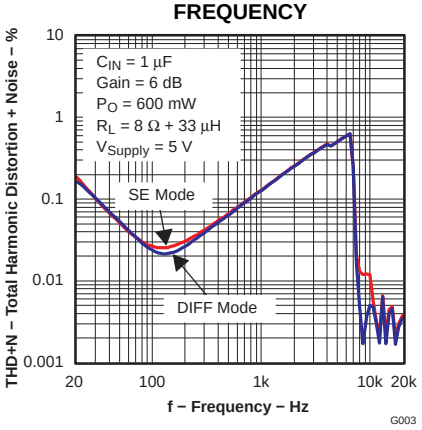


Figure 8.

TOTAL HARMONIC DISTORTION+NOISE (HP) VS FREQUENCY

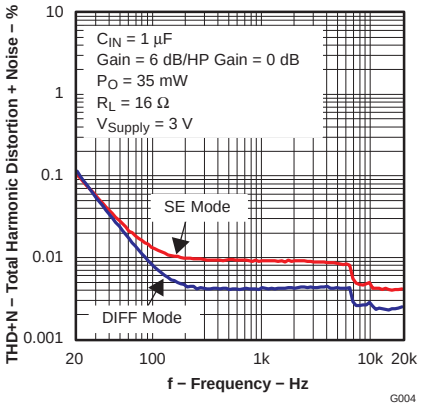


Figure 9.

TOTAL HARMONIC DISTORTION+NOISE (HP) VS FREQUENCY

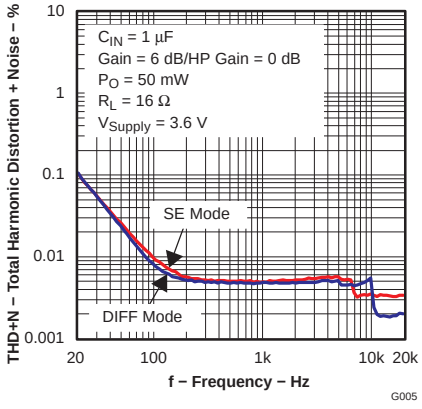


Figure 10.

TOTAL HARMONIC DISTORTION+NOISE (HP) VS FREQUENCY

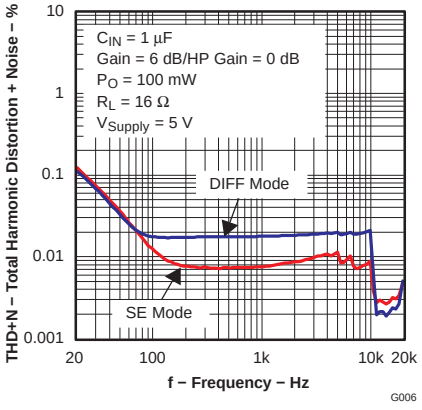


Figure 11.

TOTAL HARMONIC DISTORTION+NOISE (HP) VS FREQUENCY

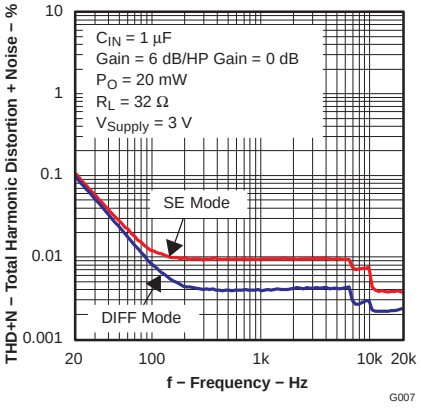


Figure 12.

TOTAL HARMONIC DISTORTION+NOISE (HP) VS FREQUENCY

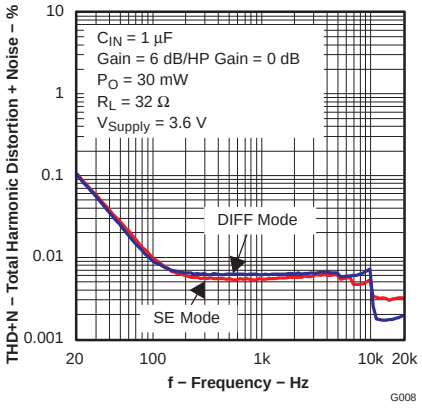


Figure 13.

TOTAL HARMONIC DISTORTION+NOISE (HP) VS FREQUENCY

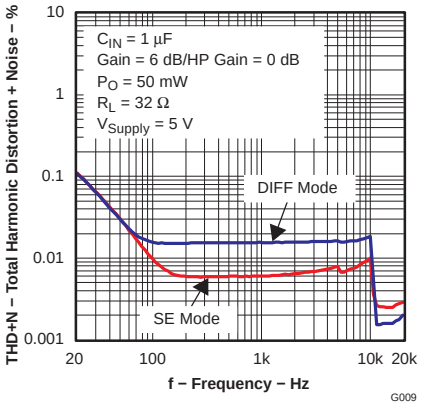


Figure 14.

TYPICAL CHARACTERISTIC GRAPHS (continued)

C_I= 1µF, C_{bypass}= 1µF

TOTAL HARMONIC DISTORTION+NOISE (SP) VS POWER

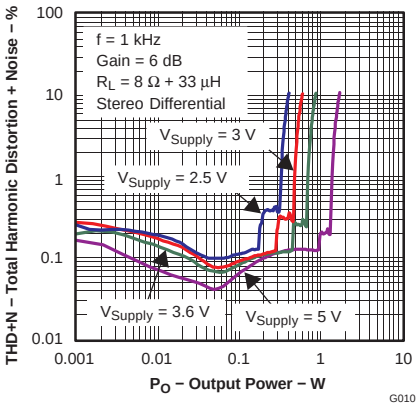


Figure 15.

TOTAL HARMONIC DISTORTION+NOISE (SP) VS POWER

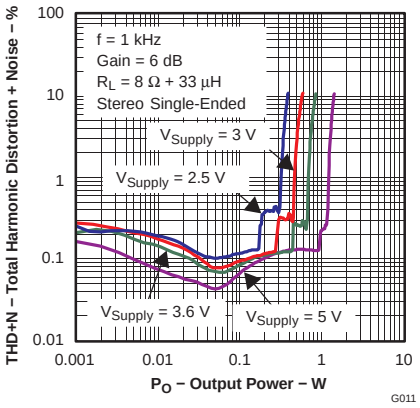


Figure 16.

TOTAL HARMONIC DISTORTION+NOISE (HP) VS POWER

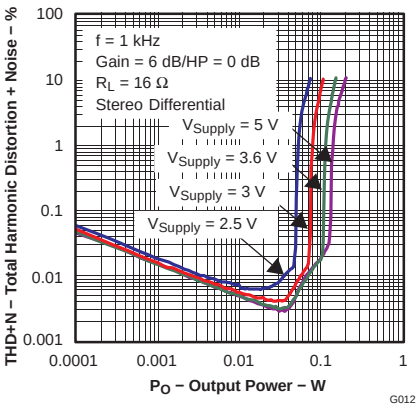


Figure 17.

TOTAL HARMONIC DISTORTION+NOISE (HP) VS POWER

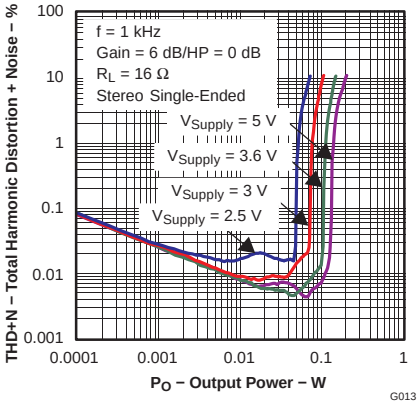


Figure 18.

TOTAL HARMONIC DISTORTION+NOISE (HP) VS POWER

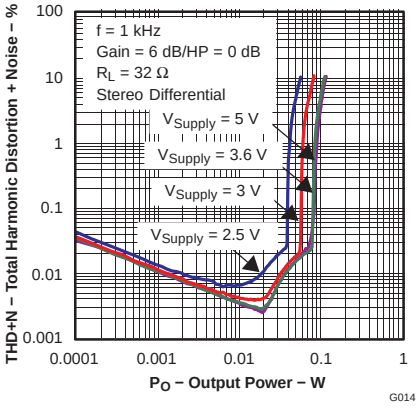


Figure 19.

TOTAL HARMONIC DISTORTION+NOISE (HP) VS POWER

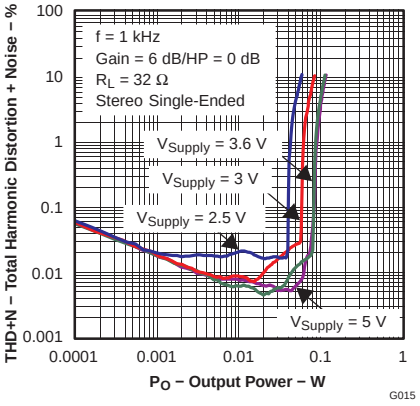


Figure 20.

SUPPLY RIPPLE REJECTION RATIO (SP) VS FREQUENCY

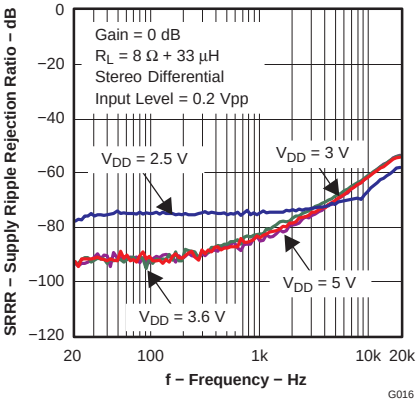


Figure 21.

SUPPLY RIPPLE REJECTION RATIO (SP) VS FREQUENCY

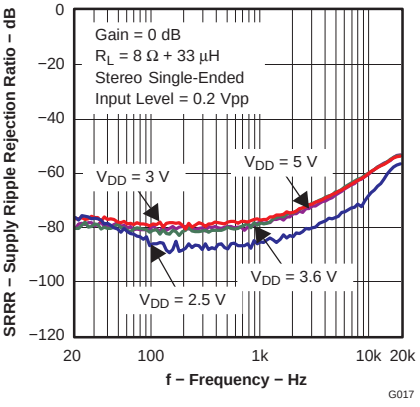


Figure 22.

SUPPLY RIPPLE REJECTION RATIO (HP) VS FREQUENCY

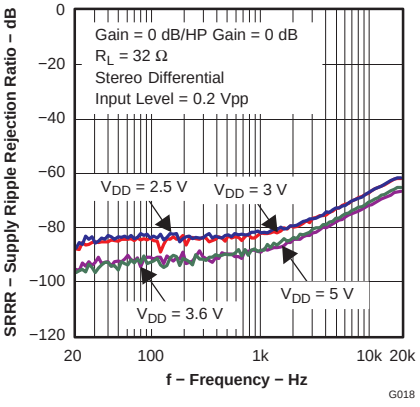


Figure 23.

TYPICAL CHARACTERISTIC GRAPHS (continued)

C_I= 1µF, C_{bypass}= 1µF

SUPPLY RIPPLE REJECTION RATIO (HP) VS FREQUENCY

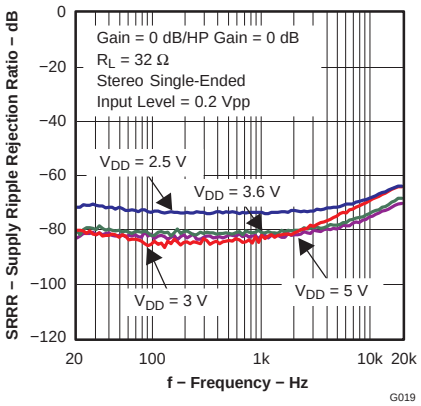


Figure 24.

EFFICIENCY (SP) VS OUTPUT POWER PER CHANNEL

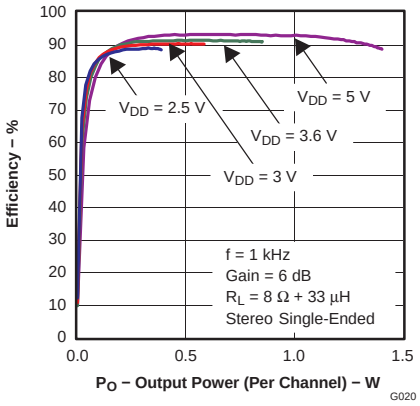


Figure 25.

TOTAL POWER DISSIPATION (SP) VS TOTAL OUTPUT POWER

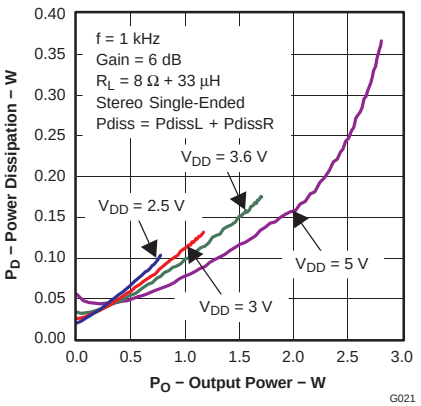


Figure 26.

TOTAL POWER DISSIPATION (HP) VS TOTAL OUTPUT POWER

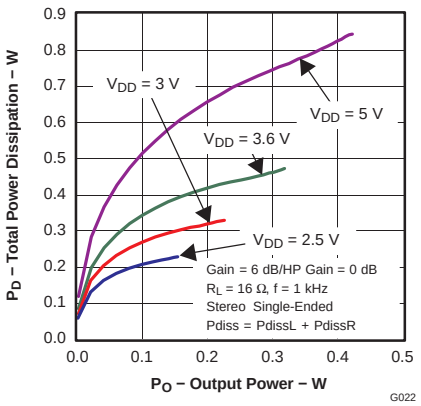


Figure 27.

TOTAL POWER DISSIPATION (HP) VS TOTAL OUTPUT POWER

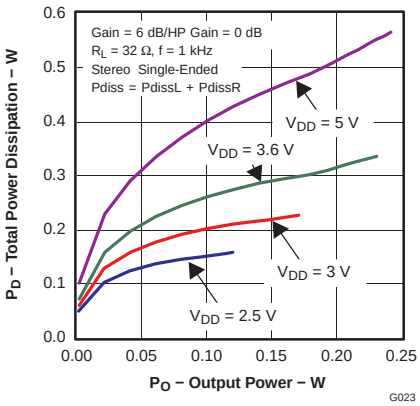


Figure 28.

OUTPUT POWER PER CHANNEL (SP) VS SUPPLY VOLTAGE

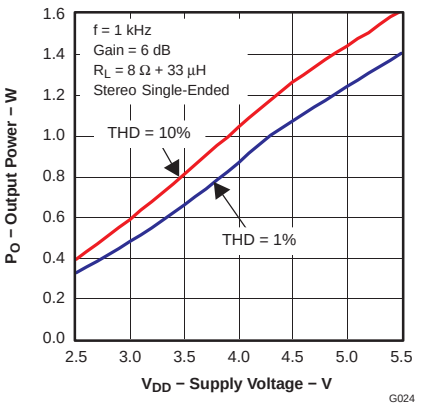


Figure 29.

OUTPUT POWER PER CHANNEL (HP) VS SUPPLY VOLTAGE

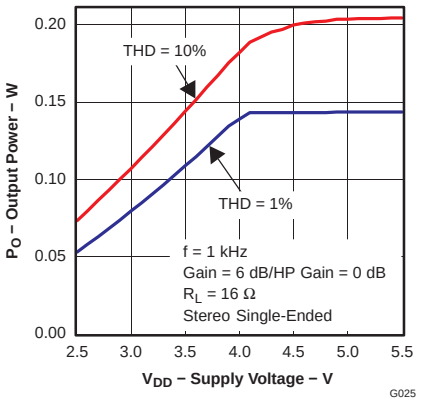


Figure 30.

OUTPUT POWER PER CHANNEL (HP) VS SUPPLY VOLTAGE

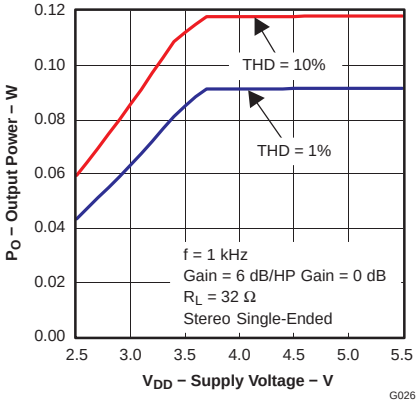


Figure 31.

COMMON-MODE REJECTION RATIO (SP) VS FREQUENCY

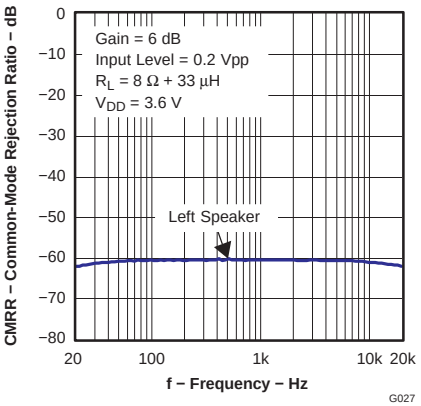


Figure 32.

TYPICAL CHARACTERISTIC GRAPHS (continued)

C_I= 1µF, C_{bypass}= 1µF

COMMON-MODE REJECTION RATIO (HP) VS FREQUENCY

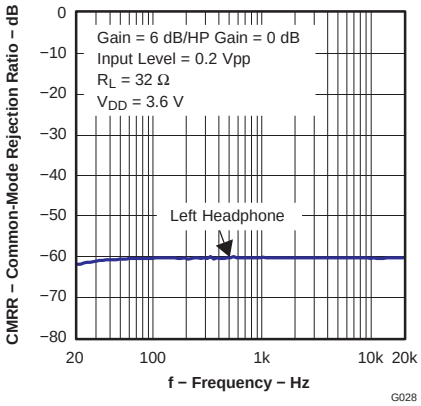


Figure 33.

CROSSTALK (SP) VS FREQUENCY

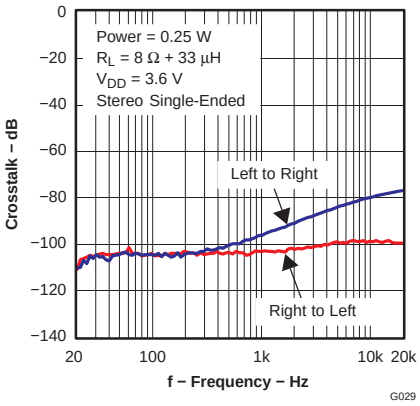


Figure 34.

CROSSTALK (HP) VS FREQUENCY

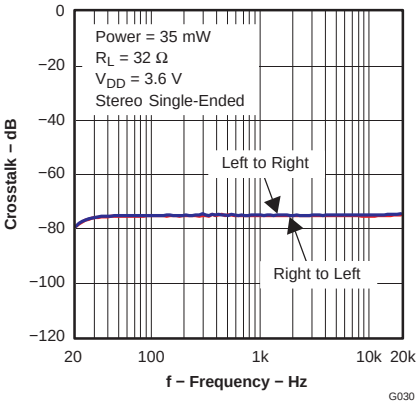


Figure 35.

SUPPLY CURRENT VS SUPPLY VOLTAGE

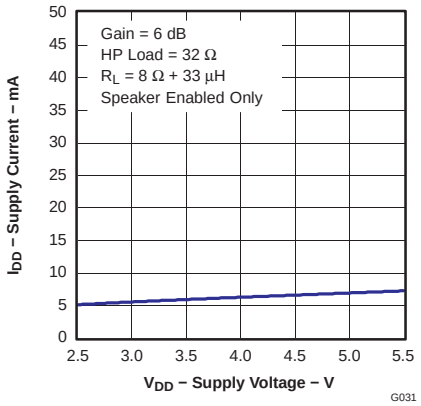


Figure 36.

SUPPLY CURRENT VS SUPPLY VOLTAGE

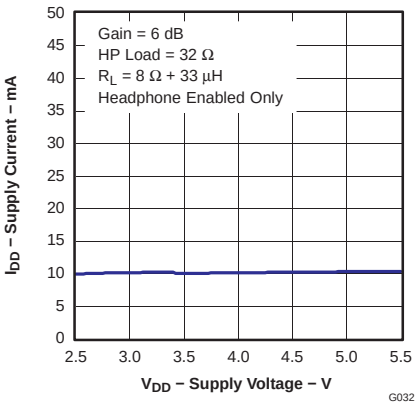


Figure 37.

SUPPLY CURRENT VS SUPPLY VOLTAGE

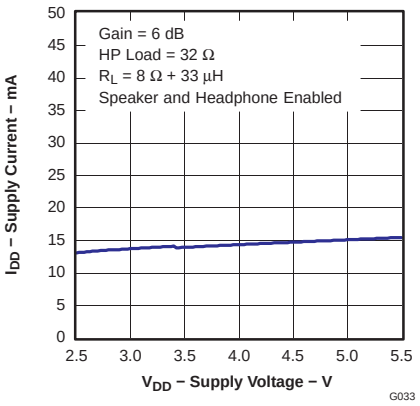


Figure 38.

TYPICAL CHARACTERISTIC GRAPHS (continued)

C_i= 1µF, C_{bypass}= 1µF

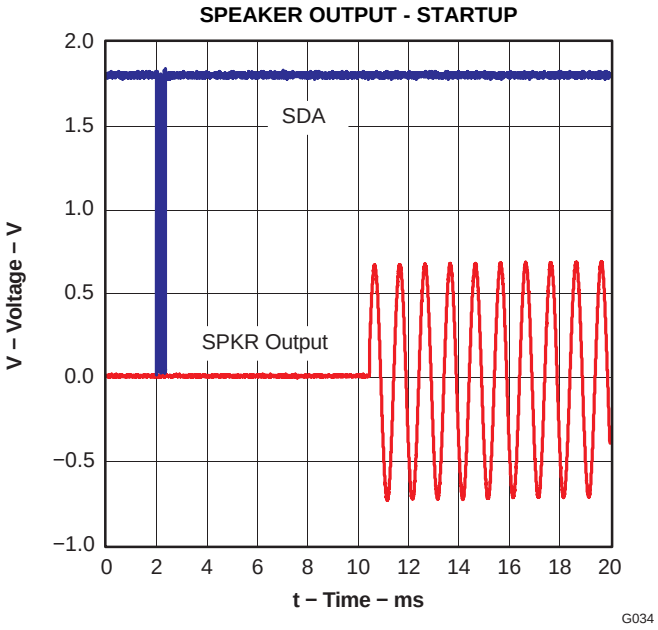


Figure 39.

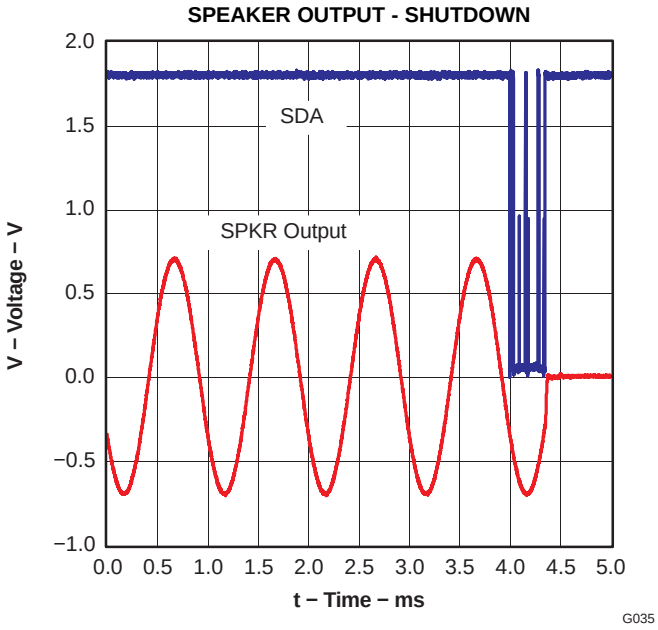


Figure 40.

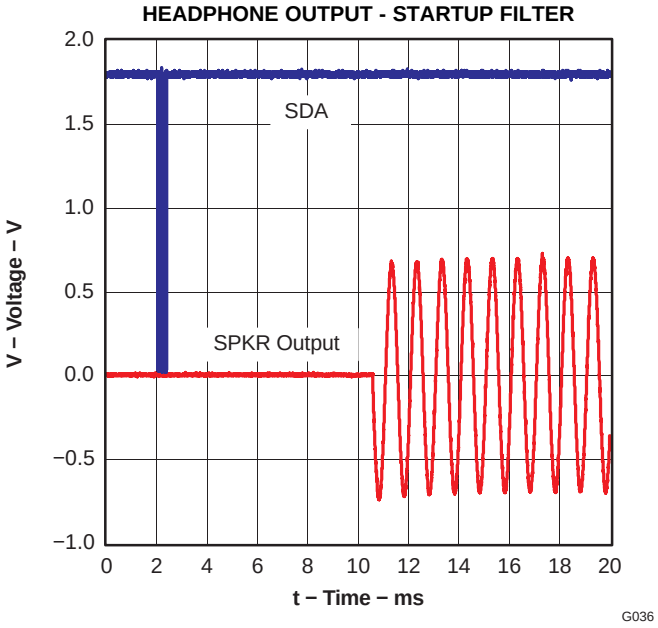


Figure 41.

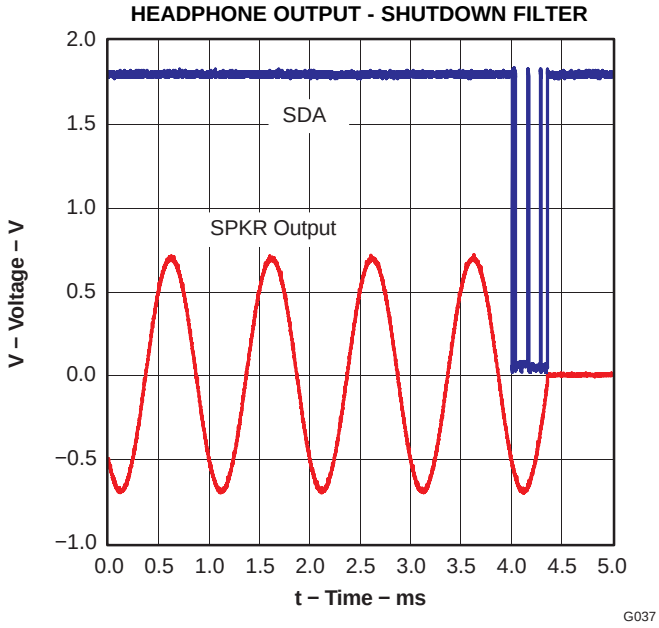


Figure 42.

DETAILED DESCRIPTION

GENERAL I²C OPERATION

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially one bit at a time. The address and data 8-bit bytes are transferred most significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transistions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transistion on SDA indicates a start and a low-to-high transistion indicates a stop. Normal data-bit transistions bust occur within the low time of the clock period. Figure 43 shows a typical sequence. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The TPA2050D4 holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

An external pull-up resistor must be used for the SDA and SCL signals to set the logic high level for the bus. When the bus level is 5 V, use pull-up resistors between 1 kΩ and 2 kΩ.

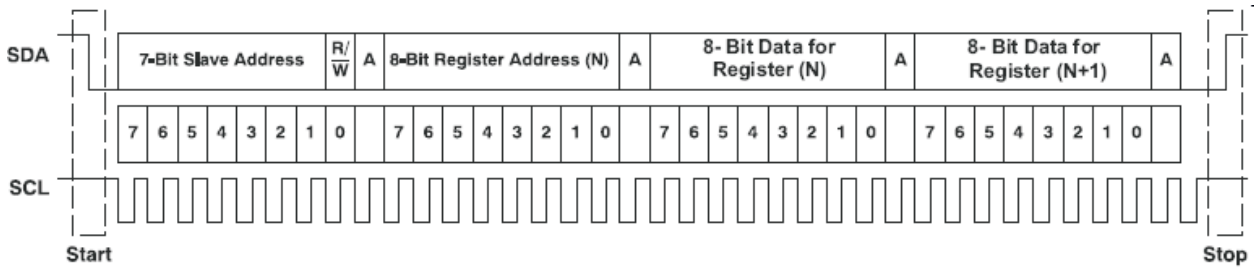


Figure 43. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. Figure 43 shows a generic data transfer sequence.

SINGLE AND MULTI-BYTE TRANSFERS

The serial control interface supports both single-byte and multi-byte read/write operations for all registers. During multi-byte reads, the TPA2050D4 responds with data, one byte at a time, starting at the register assigned provided the master devices continues to respond with acknowledgements.

The TPA2050D4 supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction has occurred. For I²C sequential write transactions, the register issued then serves as the starting point and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many registers are written to.

SINGLE-BYTE WRITE

As shown in Figure 44, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit must be set to 0. After receiving the correct I²C device address and the read/write bit, the TPA2050D4 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the TPA2050D4 internal memory address being accessed. After receiving the regitster byte, the TPA2050D4 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

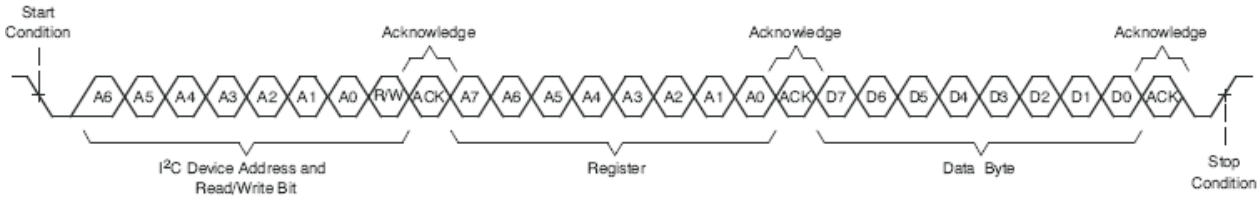


Figure 44. Single-Byte Write Transfer

MULTI-BYTE WRITE AND INCREMENTAL MULTI-BYTE WRITER

A multiple-byte data write transfer is identical to a single-byte data write transfer with the exception that multiple data bytes are transmitted by the master device to the TPA2050D4 as shown in Figure 45. After receiving each data byte, the TPA2050D4 responds with an acknowledge bit.

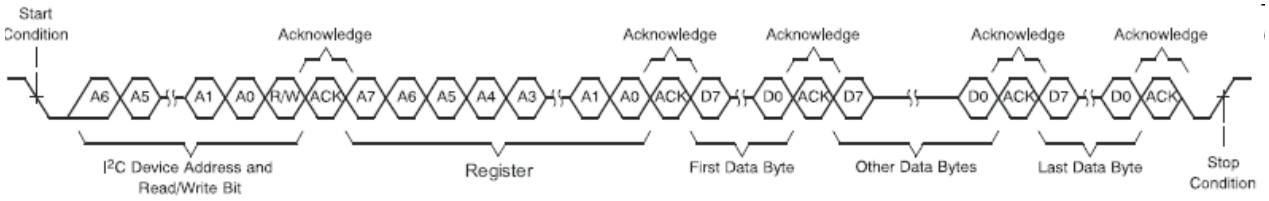


Figure 45. Multiple-Byte Write Transfer

SINGLE-BYTE READ

As shown in Figure 46, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the TPA2050D4 address and the read/write bit, the TPA2050D4 responds with an acknowledge bit. The master then sends the internal memory address byte, after which the TPA2050D4 issues an acknowledge bit. The master device transmits another start condition followed by the TPA2050D4 address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the TPA2050D4 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a notacknowledge followed by a stop condition to complete the single-byte data read transfer.

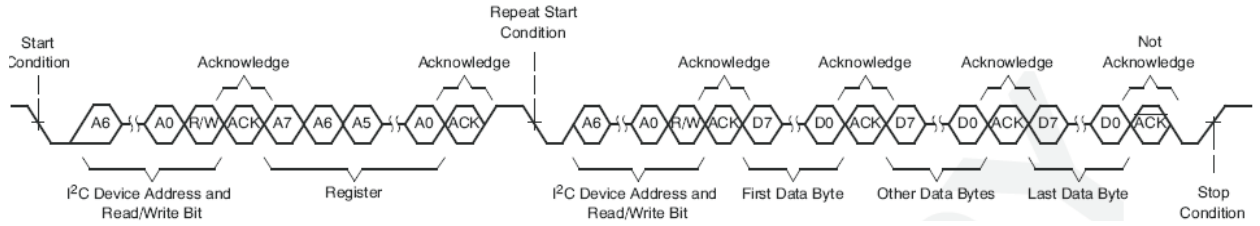


Figure 46. Single-Byte Read Transfer

MULTI-BYTE READY

A multiple-byte data read transfer is identical to a single-byte read transfer except that multiple data bytes are transmitted by the TPA2050D4 to the master device as shown in Figure 47. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

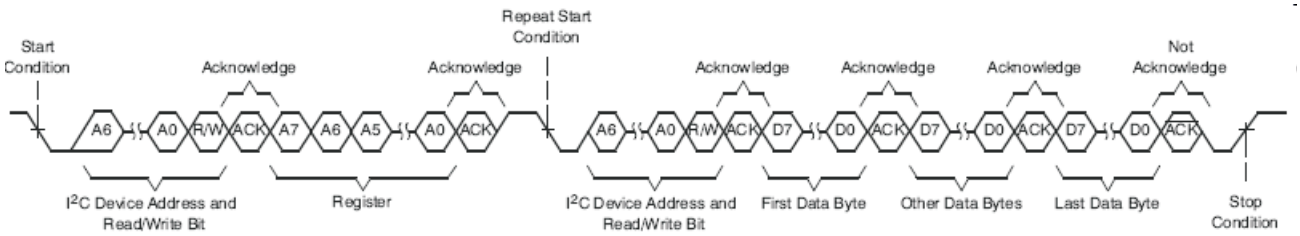


Figure 47. Multi-Byte Read Transfer

REGISTER MAPS

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	Reserved	Reserved	Reserved	PAL_Fault	PAR_Fault	HPL_Fault	HPR_Fault	Thermal
2	Reserved	Reserved	Reserved	SWS	HPL_Enable	HPR_Enable	PA_Enable	Reserved
3	LIM_Lock	Reserved	Reserved	Reserved	Reserved	Mode[2]	Mode[1]	Mode[0]
4	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5	Reserved	Reserved	Reserved	ST1_Vol[4]	ST1_Vol[3]	ST1_Vol[2]	ST1_Vol[1]	ST1_Vol[0]
6	Reserved	Reserved	Reserved	ST2_Vol[4]	ST2_Vol[3]	ST2_Vol[2]	ST2_Vol[1]	ST2_Vol[0]
7	Reserved	Reserved	Reserved	HP_Vout[2]	HP_Vout[1]	HP_Vout[0]	HP_Gain[1]	HP_Gain[0]

The TPA2050D4 I2C address is 0xE0 (binary 11100000) for writing and 0xE1 (binary 11100001) for reading. Refer to the General I2C Operation section for more details.

Bits labeled *Reserved* are reserved for future enhancements. They may not be written to as it may change the function of the device. If read, these bits may assume any value.

Any register above address 0x07 is reserved for testing and should not be written to because it may change the function of the device. If read, these bits may assume any value.

Fault Register (Address: 1)

BIT	7	6	5	4	3	2	1	0
Function	Reserved	Reserved	Reserved	PAL_Fault	PAR_Fault	HPL_Fault	HPR_Fault	Thermal
Reset Value	0	0	0	0	0	0	0	0

Reserved	These bits are reserved for future enhancements. They will not change state if programmed. If read these bits may assume any value.
PAL_Fault	Logic high indicates an over-current event has occurred on the Class-D left channel output. This bit is clear-on-write. Only logic low can be written to this bit.
PAR_Fault	Logic high indicates an over-current event has occurred on the Class-D right channel output. This bit is clear-on-write. Only logic low can be written to this bit.
HPL_Fault	Logic high indicates an over-current event has occurred on the headphone left channel output. This bit is clear-on-write. Only logic low can be written to this bit.
HPR_Fault	Logic high indicates an over-current event has occurred on the headphone right channel output. This bit is clear-on-write. Only logic low can be written to this bit.
Thermal	Logic high indicates thermal shutdown activated. Bit automatically clears when the thermal condition lowers past the hysteresis threshold.

Power Management Register (Address: 2)

BIT	7	6	5	4	3	2	1	0
Function	Reserved	Reserved	Reserved	SWS	HPL_Enable	HPR_Enable	PA_Enable	Reserved
Reset Value	0	0	0	1	0	0	0	0

Reserved	These bits are reserved for future enhancements. They will not change state if programmed. If read these bits may assume any value.
SWS	Software shutdown. Set to logic high to deactivate the TPA2050D4. Logic low reactivates the charge pump and input amplifiers; enable headphone and Class-D amplifiers using HPL_Enable, HPR_Enable, and PA_Enable. Default on turn-on is SWS logic high.
HPL_Enable	Headphone left channel enable. Set to logic low to deactivate left channel.
HPR_Enable	Headphone right channel enable. Set to logic low to deactivate right channel.
PA_Enable	Class-D power amplifier enable. Set to logic low to deactivate both left and right Class-D power amplifiers.

Mux Output Control Register (Address: 3)

BIT	7	6	5	4	3	2	1	0
Function	LIM_Lock	Reserved	Reserved	Reserved	Reserved	Mode[2]	Mode1]	Mode[0]
Reset Value	0	0	0	0	0	0	0	1

Reserved	These bits are reserved for future enhancements. They will not change state if programmed. If read these bits may assume any value.
LIM_Lock	Limiter change lockout. Set bit to logic high to prevent any changes to the HP_Vout[2:0] and LIM_Lock bits. The LIM_Lock bit can only be returned to 0 by applying logic low to the $\overline{\text{RESET}}$ pin or powering down VDD.
Mode[2:0]	Sets mux output mode. Refer to Modes of Operation section for details. Default mode is 001 (Stereo 1 Input mode) on power-up.

Reserved Control Register (Address: 4)

BIT	7	6	5	4	3	2	1	0
Function	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset Value	0	0	0	1	0	0	1	1

Reserved	These bits are reserved for future enhancements. They will not change state if programmed. If read these bits may assume any value.

Stereo Input 1 Volume Control Register (Address: 5)

BIT	7	6	5	4	3	2	1	0
Function	Reserved	Reserved	Reserved	ST1_Vol[4]	ST1_Vol[3]	ST1_Vol[2]	ST1_Vol[1]	ST1_Vol[0]
Reset Value	0	0	0	1	0	0	1	1

Reserved	These bits are reserved for future enhancements. They will not change state if programmed. If read these bits may assume any value.
ST1_Vol[4:0]	Five-bit volume control for Stereo Input 1 in single-ended input mode and stereo input pair in differential input mode. 11111 sets device to its highest gain (+12 dB); 00000 sets device to its lowest gain (–60 dB). Default setting on power-up is 10011 (+0 dB).

Stereo Input 2 Volume Control Register (Address: 6)

BIT	7	6	5	4	3	2	1	0
Function	Reserved	Reserved	Reserved	ST2_Vol[4]	ST2_Vol[3]	ST2_Vol[2]	ST2_Vol[1]	ST2_Vol[0]
Reset Value	0	0	0	1	0	0	1	1

Reserved These bits are reserved for future enhancements. They will not change state if programmed. If read these bits may assume any value.

ST2_Vol[4:0] Five-bit volume control for Stereo Input 2. 11111 sets device to its highest gain (+12 dB); 00000 sets device to its lowest gain (–60 dB). Default setting on power-up is 10011 (+0 dB).

Headphone Output Control Register (Address: 7)

BIT	7	6	5	4	3	2	1	0
Function	Reserved	Reserved	Reserved	HP_Vout[2]	HP_Vout[1]	HP_Vout[0]	HP_Gain[1]	HP_Gain[0]
Reset Value	0	0	0	0	0	0	0	0

Reserved These bits are reserved for future enhancements. They will not change state if programmed. If read these bits may assume any value.

HP_Vout[2:0] Headphone output voltage limiter. Sets the maximum output voltage / power to the headphones.

HP_Gain[1:0] Headphone gain select. Sets the gain of the headphone output amplifiers.

MODES OF OPERATION

The TPA2050D4 has several operating modes for single-ended and differential inputs. Stereo 1 refers to the LIN_1 and RIN_1 input pair; Stereo 2 refers to the LIN_2 and RIN_2 input pair.

Mux Output Mode

The input mux selects which device input is directed to both the Class-D and headphone amplifiers. Mux summing and output are after the channel volume controls, as shown in the Simplified Functional Diagram. Program the mux mode using the Mode[2:0] bits in Mux Output Control (Register 3, Bits 0–2). Select the appropriate mode according to the table below.

MODE BYTE: MODE[2:0]	MUX MODE	MUX OUTPUT		MUX OUTPUT DESCRIPTION
		LEFT	RIGHT	
000	Reserved	Mute	Mute	No audio available at mux output
001	Stereo 1 Input	LIN_1	RIN_1	LIN_1 and RIN_1 stereo single-ended input
010	Stereo 2 Input	LIN_2	RIN_2	LIN_2 and RIN_2 stereo single-ended input
011	Stereo Differential	LIN_1–RIN_1	LIN_2–RIN_2	LIN_1 and RIN_1 compose the left channel; LIN_2 and RIN_2 compose the right channel
100	Mono Differential	(LIN_1–RIN_1) + (LIN_2–RIN_2)	(LIN_1–RIN_1) + (LIN_2–RIN_2)	Left and right differential inputs summed and directed to left and right mux output
101	Stereo 1 (monomode)	LIN_1 + RIN_1	LIN_1 + RIN_1	LIN_1 + RIN_1 distributed to both left and right inputs of the headphone and Class-D amplifiers
110	Stereo 2 (monomode)	LIN_2 + RIN_2	LIN_2 + RIN_2	LIN_2 + RIN_2 distributed to both left and right inputs of the headphone and Class-D amplifiers
111	Mute	Mute	Mute	All inputs muted; no audio available at mux output

Differential Input Mode

The LIN_1 and RIN_1 input pair and the LIN_2 and RIN_2 input pair are configurable as either single-ended or differential inputs. Differential transmission between an audio source and the TPA2050D4 input improves system noise rejection when compared to single-ended transmission.

In differential input modes, connect the Left+ and Left– source signal to LIN_1 and RIN_1, respectively; connect Right+ and Right– to LIN_2 and RIN_2, respectively. Single-ended input modes allow selection between two stereo sources. Differential input modes allow connection to only one stereo source.

START-UP SEQUENCING AND SHUTDOWN CONTROL

For correct start up with no turn-on pop, apply PVDD and VDDHP before applying DVDD while keeping $\overline{\text{RESET}}$ at logic low. Once DVDD has settled to a minimum of 1.7 V, set $\overline{\text{RESET}}$ to logic high to complete the start-up sequence. The TPA2050D4 starts up in soft shutdown mode with the SWS bit (Register 2, Bit 4) at logic high.

The stereo Class-D power amplifiers, left headphone amplifier, and right headphone amplifier each have their own enable bits within the Power Management byte (Register 2, Bits 3–1). Set the corresponding bit to logic high to enable these amplifiers. Disabling an amplifier mutes its output and reduces supply current. Set SWS to logic high to deactivate all sections except the I2C interface, reducing total supply current to 2 μA,max.

Set $\overline{\text{RESET}}$ to logic low to deactivate all sections including the I^2C interface. The I^2C registers cannot be programmed while $\overline{\text{RESET}}$ remains at logic low. Refer to the Headphone Output Limiter Lockout section for more details on using $\overline{\text{RESET}}$.

All register contents are maintained provided the supply voltage is not powered down and $\overline{\text{RESET}}$ remains at logic high. On deactivation of DVDD or PVDD, or on $\overline{\text{RESET}}$ set to logic low, all information programmed into the registers by the user is lost, returning to their default state once power is reapplied.

Class-D Output Amplifiers

To enable both Class-D power amplifiers, set the PA_Enable bit (Register 2, Bit 1) to logic high. The left and right channel Class-D outputs cannot be separately activated. Total Class-D section typical current is 7 mA when active and less than 1 μA when deactivated.

All Class-D outputs have short-circuit current protection and thermal overload protection. The PAL_Fault and PAR_Fault bits (Register 1, Bits 4 and 3) indicate an over-current event on the left and right Class-D channel outputs. These bits are clear-on-write; only logic low can be written.

The Thermal bit (Register 1, Bit 1) goes to logic high if a thermal shutdown event occurs. It returns to logic low once the device temperature returns below 150°C.

DirectPath Headphone Amplifier

Set the HPL_Enable bit (Register 2, Bit 3) to logic high to enable the headphone left output and the HPR_Enable bit (Register 2, Bit 2) to logic high to enable the headphone right output. The headphone amplifier draws 10 mA of typical supply current with both left and right outputs active and less than 1 μA when deactivated.

The HPL_Fault and HPR_Fault bits (Register 1, Bits 2 and 1) indicate an over-current event on the left and right headphone outputs. These bits are clear-on-write; only logic low can be written.

HEADPHONE OUTPUT LIMITER LOCKOUT

Setting the LIM_Lock bit (Register 3, Bit 7) to logic high prevents any register changes to the HP_Vout byte (Register 7, Bits 4-2) and the LIM_Lock bit itself. The LIM_Lock bit will remain locked at logic high until the power supply is deactivated or logic low is applied to the $\overline{\text{RESET}}$ pin. All volume control, mux modes and shutdown registers remain writable regardless of LIM_Lock status.

MAXIMUM HEADPHONE POWER REGULATOR

The HP_Vout byte (Register 7, Bits 4-2) sets the maximum output voltage from the headphone amplifiers. This is useful for limiting the maximum output power to the headphones. The HP_Vout byte sets the internally regulated supply voltage to the headphone amplifiers according to the table below. The table also shows the equivalent 10% THD output into 16Ω and 32Ω loads.

MAX HEADPHONE OUTPUT BYTE: HP_VOUT[2:0]	$V_{OUT,MAX}$	$P_{OUT,MAX}$ INTO 16Ω (10% THD)	$P_{OUT,MAX}$ INTO 32Ω (10% THD)
000	±VDDHP (1)	130 mW (at VDDHP = 3.6 V)	65 mW (at VDDHP = 3.6 V)
001	±1.13 V	40 mW	20 mW
010	±0.54 V	9 mW	4.5 mW
011	±0.38 V	4.5 mW	2.3 mW
100	±0.315 V	3.1 mW	1.6 mW
101	±0.253 V	2.0 mW	1.0 mW
110	±0.227 V	1.6 mW	0.8 mW
111	±0.196 V	1.2 mW	0.6 mW

(1) With no load. Maximum output voltage decreases as load resistance decreases.

HEADPHONE GAIN VALUES

For the DirectPath headphone amplifier, left and right output channels

HEADPHONE GAIN REGISTER BYTE: HP_GAIN[1:0]	NOMINAL GAIN
00	0 dB
01	–6 dB
10	–12 dB
11	–20 dB

INPUT VOLUME CONTROL

The TPA2050D4 has two independent volume controls: One for the STEREO1 input pair (LIN_1 and RIN_1), and one for the STEREO2 input pair (LIN_2 and RIN_2). Each has 5-bit (32-step) resolution and are audio tapered; gain step changes are smaller at higher gain settings. The volume control range is –60 dB to +12 dB.

The Stereo Input 1 volume control byte is located at Register 5, Bits 4–0. The Stereo Input 2 volume control byte is at Register 6, Bits 4–0. Gain matching between the left and right channels for STEREO1 and STEREO2 is within 0.1 dB. In differential input mode, the Stereo Input 1 byte (Register 5) controls left and right channel gain.

The input impedance to the TPA2050D4 decreases as channel gain increases. See the Operating Characteristics section for specifications. Values listed in Audio Taper Gain Values table are nominal values.

AUDIO TAPER GAIN VALUES

For input channel volume controls

VOLUME CONTROL REGISTER BYTE: VOL[4:0]	NOMINAL GAIN	VOLUME CONTROL REGISTER BYTE: VOL[4:0]	NOMINAL GAIN
00000	–60 dB	10000	–3.0 dB
00001	–48 dB	10001	–2.0 dB
00010	–43 dB	10010	–1.0 dB
00011	–38 dB	10011	+0 dB
00100	–33 dB	10100	+1.0 dB
00101	–29 dB	10101	+2.0 dB
00110	–25 dB	10110	+3.0 dB
00111	–21 dB	10111	+4.0 dB
01000	–17 dB	11000	+5.0 dB
01001	–15 dB	11001	+6.0 dB
01010	–13 dB	11010	+7.0 dB
01011	–11 dB	11011	+8.0 dB
01100	–9.0 dB	11100	+9.0 dB
01101	–7.5 dB	11101	+10 dB
01110	–6.0 dB	11110	+11.0 dB
01111	–4.5 dB	11111	+12.0 dB

DECOUPLING CAPACITOR (C_S)

The TPA2050D4 is a high-performance Class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) 1-μF ceramic capacitor (typically) placed as close as possible to the device PVDD (L, R) lead works best. Placing this decoupling capacitor close to the TPA2050D4 is important for the efficiency of the Class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 4.7 μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

INPUT CAPACITORS (C_I)

The input capacitors and input resistors form a high-pass filter with the corner frequency, f_C, determined in Equation 1.

$$f_C = \frac{1}{(2\pi \times R_I \times C_I)} \quad (1)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Not using input capacitors can increase output offset. Equation 2 is used to solve for the input coupling capacitance. If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

$$C_I = \frac{1}{(2\pi \times R_I \times f_C)} \quad (2)$$

BOARD LAYOUT

In making the pad size for the WCSP balls, it is recommended that the layout use non solder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 48 and Table 1 shows the appropriate diameters for a WCSP layout. The TPA2050D4 evaluation module (EVM) layout is shown in the next section as a layout example.

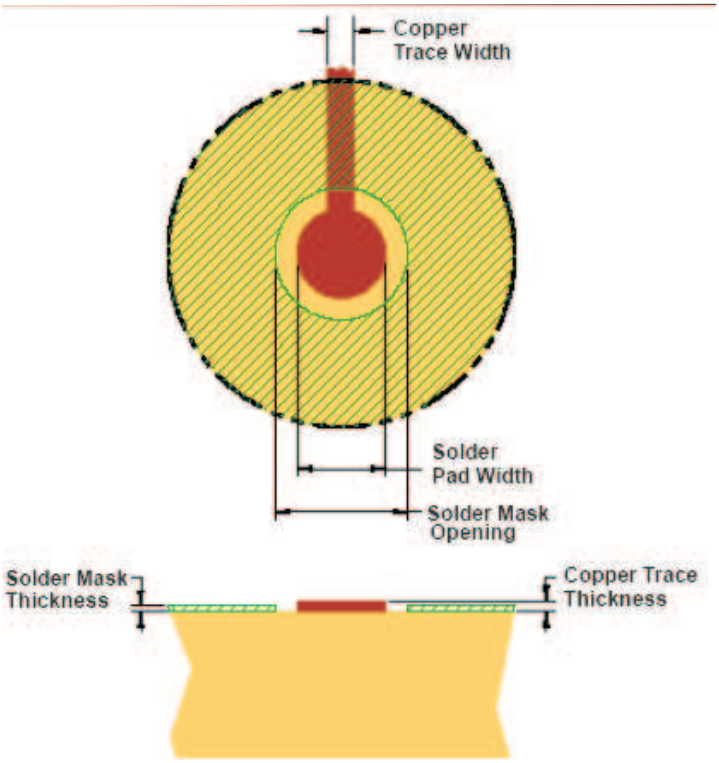


Figure 48. Land Pattern Dimensions

Table 1. Land Pattern Dimensions(1) (2) (3) (4)

SOLDER PAD DEFINITIONS	COPPER PAD	SOLDER MASK(5) OPENING	COPPER THICKNESS	STENCIL(6) (7) OPENING	STENCIL THICKNESS
Non solder mask defined (NSMD)	275 µm (+0.0, –25 µm)	375 µm (+0.0, –25 µm)	1 oz max (32 µm)	275 µm × 275 µm Sq. (rounded corners)	125 µm thick

(1) Circuit traces from NSMD defined PWB lands should be 75 µm to 100 µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
(2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
(3) Recommend solder paste is Type 3 or Type 4.
(4) For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5 mm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 µm on top of the copper circuit pattern
(6) Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
(7) Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

COMPONENT LOCATION

Place all the external components very close to the TPA2050D4. Placing the decoupling capacitor, C_S, close to the TPA2050D4 is important for the efficiency of the Class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

TRACE WIDTH

Recommended trace width at the solder balls is 75 µm to 100 µm to prevent solder wicking onto wider PCB traces. For high current pins (PVDD (L, R), PGND, and audio output pins) of the TPA2050D4, use 100-µm trace widths at the solder balls and at least 500-µm PCB traces to ensure proper performance and output power for the device. For the remaining signals of the TPA2050D4, use 75-µm to 100-µm trace widths at the solder balls. The audio input pins (INR± and INL±) must run side-by-side to maximize common-mode noise cancellation.

EFFICIENCY AND THERMAL INFORMATION

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the packages are shown in the dissipation rating table. Converting this to θ_{JA} for the WCSP package:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.009} = 111^{\circ}\text{C/W} \quad (3)$$

Given θ_{JA} of 111°C/W, the maximum allowable junction temperature of 150°C, and the maximum internal dissipation of 0.12 W (0.06 W per channel) for 1.4 W per channel, 8-Ω load, 5-V supply, from Figure 25 , the maximum ambient temperature can be calculated with the following equation:

$$T_A\text{Max} = T_J\text{Max} - \theta_{JA}P_{DMAX} = 150 - 111(0.12) = 137^{\circ}\text{C} \quad (4)$$

Equation 4 shows that the calculated maximum ambient temperature is 137°C at maximum power dissipation with a 5-V supply and 8-Ω a load. The TPA2050D4 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Also, using speakers more resistive than 8-Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier.

OPERATION WITH DACS AND CODECS

In using Class-D amplifiers with CODECs and DACs, sometimes there is an increase in the output noise floor from the audio amplifier. This occurs when mixing of the output frequencies of the CODEC/DAC mix with the switching frequencies of the audio amplifier input stage. The noise increase can be solved by placing a low-pass filter between the CODEC/DAC and audio amplifier. This filters off the high frequencies that cause the problem and allow proper performance. See the functional block diagram.

FILTER FREE OPERATION AND FERRITE BEAD FILTERS

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter and the frequency sensitive circuit is greater than 1 MHz. This filter functions well for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. When choosing a ferrite bead, choose one with high impedance at high frequencies, and low impedance at low frequencies. In addition, select a ferrite bead with adequate current rating to prevent distortion of the output signal.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker. Figure 49 shows typical ferrite bead and LC output filters.

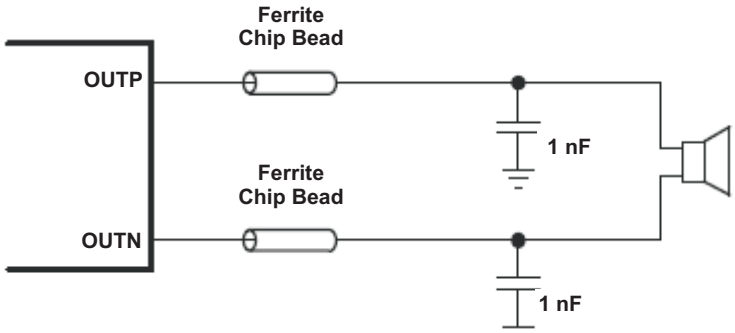


Figure 49. Typical Ferrite Bead Filter (Chip bead example: TDK: MPZ1608S221A)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPA2050D4YZKR	ACTIVE	DSBGA	YZK	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPA2050D4YZKT	ACTIVE	DSBGA	YZK	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

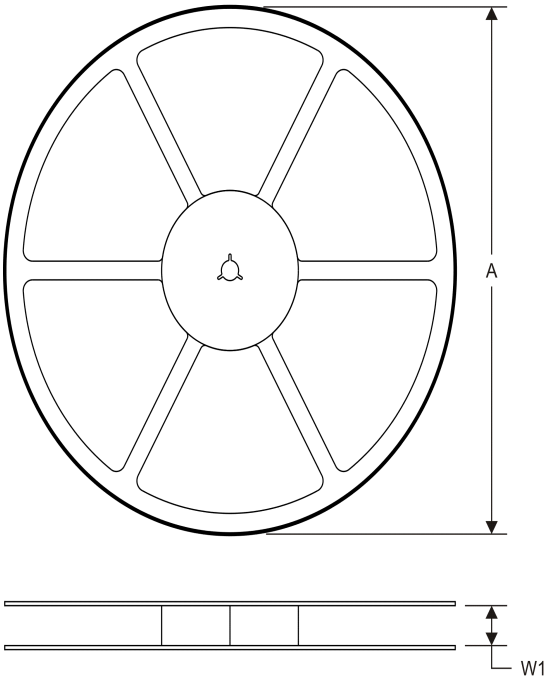
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

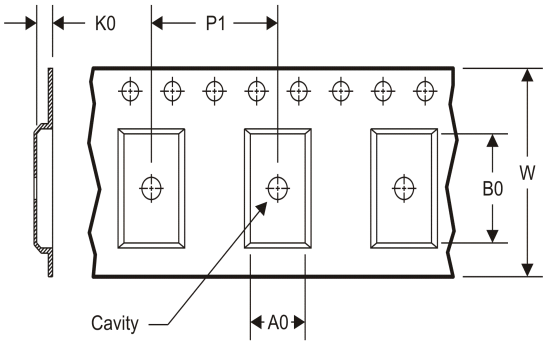
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



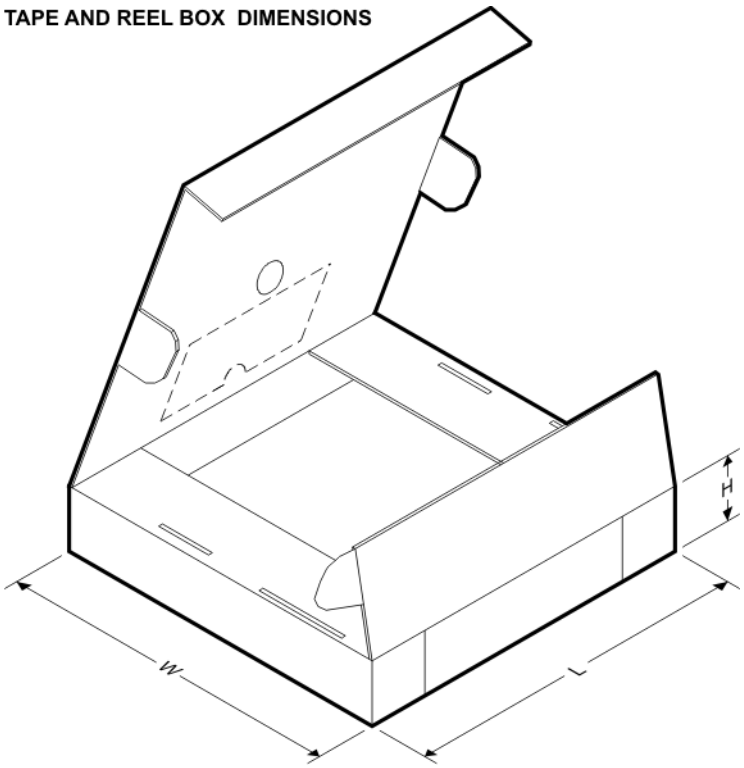
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2050D4YZKR	DSBGA	YZK	25	3000	180.0	8.4	2.75	2.75	0.81	4.0	8.0	Q1
TPA2050D4YZKT	DSBGA	YZK	25	250	180.0	8.4	2.75	2.75	0.81	4.0	8.0	Q1

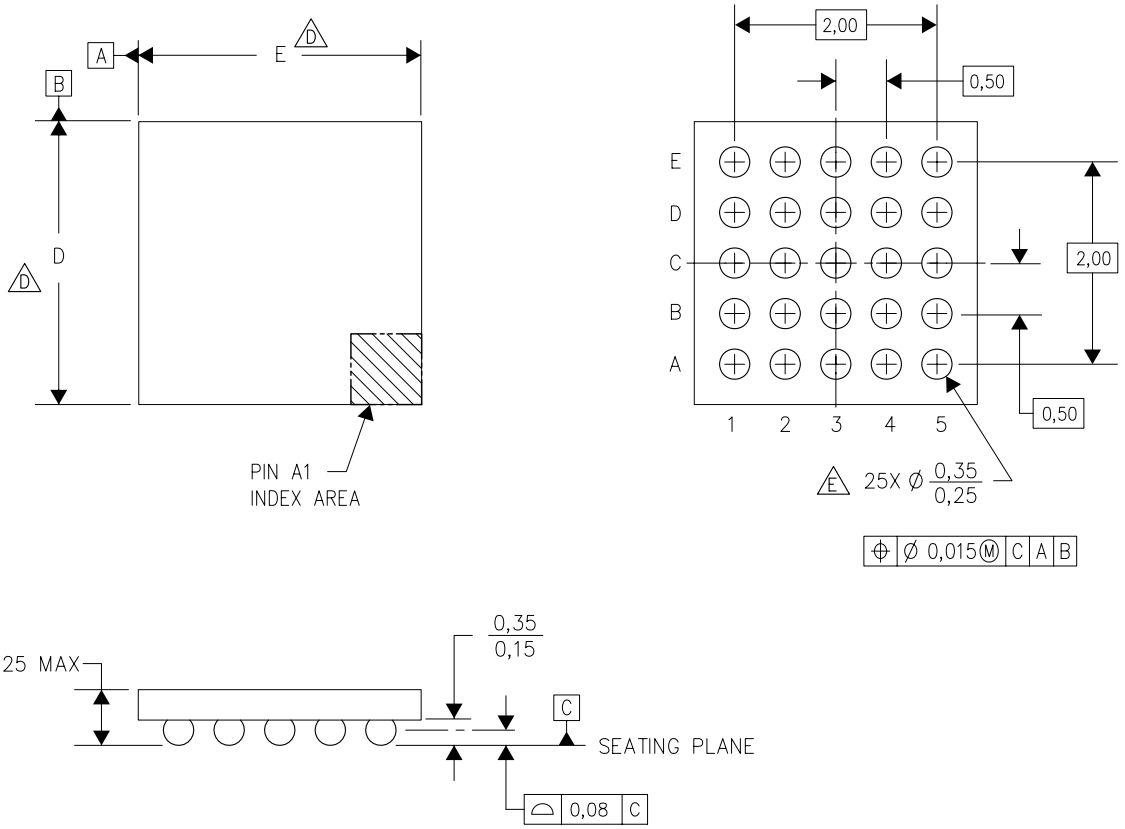
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2050D4YZKR	DSBGA	YZK	25	3000	210.0	185.0	35.0
TPA2050D4YZKT	DSBGA	YZK	25	250	210.0	185.0	35.0

YZK (S–XBGA–N25) DIE–SIZE BALL GRID ARRAY



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZK package can have dimension D ranging from 2.44 to 3.15 mm and dimension E ranging from 2.44 to 3.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 5 x 5 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YEK (Drawing #4204185) for tin–lead (SnPb) balls.

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