

High-Voltage Types (20-Volt Rating)

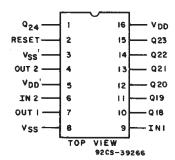
CMOS 24-Stage Frequency Divider

- Features:
- Reset disables the RC oscillator for lowpower standby condition
- Voo' and Vss' pins are brought out from the crystal oscillator to allow use of external resistors for low-power operation . Meets all requirements of JEDEC
- Maximum input current of 1 µA at 18 V over full package-temperature range: 100 nA at 18 V and 25° C
- Common reset

- 100% tested for 20-V quiescent current
- 5, 10 and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

CD4521B consists of an oscillator section and 24 ripple-carry binary counter stages. The oscillator configuration (using IN1) allows design of either RC or crystal oscillator circuits. IN1 should be tied either HIGH or LOW when not in use. A HIGH on the RESET causes the counter to go to the all-0's state and disables the oscillator. The count is advanced on the negative transition of IN1 (and IN2). A time-saving test mode is described in the Functional Test Sequence Table and in Fig. 6.

The CD4521B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M. M96, MT. and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).



TERMINAL ASSIGNMENT

OUTPUT	COUNT CAPACITY	
Q18	218 = 262,144	
Q19	219 = 524,288	
Q20	2 ²⁰ = 1,048,576	
Q21	2 ²¹ = 2,097,152	
Q22	2 ²² = 4,194,304	
Q23	2 ²³ = 8,388,608	
Q24	2 ²⁴ = 16,777,216	

MAXIMUM RATINGS, Absolute-Maximum Values:

• • • • • • • • • • • • • • • • • • • •	
DC SUPPLY-VOLTAGE RANGE, (VDD)	
Voltages referenced to VSS Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	+0.5V to Vnn +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (PD):	
For T _A = -55°C to +100°C	500mW
For T _A = +100°C to +125°C	erate Linearity at 12mW/OC to 200mW
FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (TA)	55°C to +125°C
STORAGE TEMPERATURE RANGE (T _{stg})	65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max	+265°C

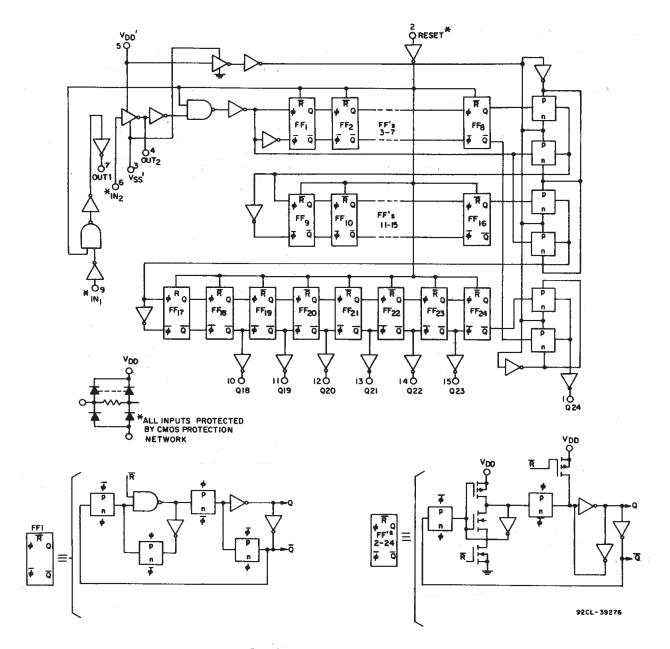


Fig. 1 - Logic diagram for CD4521B.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	со	NDITIO	NS	LIN	MITS AT	TS AT INDICATED TEMPERATURES (°C)					UNITS
	Vo	VO VIN VDD	+25			1 1					
	(v)	(V)	(V)	-55	-40	+85	+125	Min.	Тур.	Max.	<u> </u>
		0, 5	- 5	5.	. 5	150	150	_	0.04	5	
Quiescent Device	— ·	0, 10	10	10	10	300	300		0.04	10	μΑ
Current, IDD Max.		0, 15	15	20	20	600	600		0.04	20] "
	-	0, 20	20	100	100	3000	3000		0.08	100]
Out-11 (Si-1)	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	-1 ⁵	_	
Output Low (Sink)	0.5	0, 10	-10	1.6	1.5	1.1	0.9	1.3	2.6	_]
Current, IoL Min.	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	_	mA
\$	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1		
Output High (Source)	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	_	
Current, Ion Min.	9.5	0, 10	10	-1.6	1.5	1.1	-0.9	-1.3	-2.6		
	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	_	
Output Valtages	_	0, 5	5		0.	05			0	0.05	
Output Voltage:	_	0, 10	10		0.	05		_	0	0.05	
Low-Level, Vol Max.		0, 15	. 15		0.	.05		· —	0	0.05	
Output Valtage	_	0, 5	5 .		4.	95		4.95	5		
Output Voltage:		0, 10	10 -		9.	95		9.95	10	_	
High-Level, V _{он} Min.	_	0, 15	15 🗸		1.4	.95	-	14.95	15	_	V
Innuit I am Valtage	0.5,4.5	_	5	-	1	.5		_		1.5] '
Input Low Voltage, V _{IL} Max.	1, 9	_	10			3				3	
	1.5,13.5	_	15			4				4]
Input High Voltage	0.5,4.5		5		3	3.5		3.5]
Input High Voltage,	1, 9		10			7		7] [
V _{IH} Min.	1.5,13.5		15			l 1		11			
Input Current, I _{IN} Max.	T -	0, 18	18	±0.1	±0.1	±1	±1		±10 ⁻⁵	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:

01145407774	VDD	LIM	ITS	UNITS	
CHARACTERISTIC	(V)	Min.	Max.	UNITS	
Supply-Voltage Range (For TA = Full Package-Ter	_	3	18	٧	
		5	340		
Input Pulse Width	tw ø	10	150		
•		15	120	_	
		5	180	-	ns
Reset Pulse Width	t _{w(R)}	10	80	_	
		15	50	_	
		5	_	2	
Input Pulse Frequency	fφ	10	_	5	MHz
	,	15	_	6.5	
****		5	_	15	
Input Pulse Rise or Fall Time	$t_{r}oldsymbol{\phi}, t_{t}oldsymbol{\phi}$	10	_	15	μs
·		15	_	15	
		5	1K	10M	
R _T Operating Range		10	1K	10M	Ω
		15	1K	10M	
		5	15p	10M	
C _T Operating Range		10	15p	10M	F
		15	15p	10M	

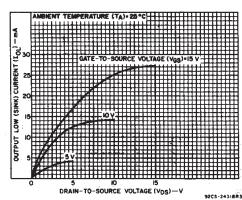


Fig. 2 - Typical output low (sink) current characteristics.

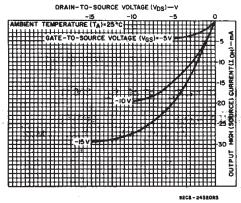


Fig. 4 - Typical output high (source) current characteristics.

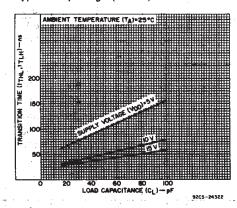


Fig. 6 - Typical transition time as a function of load capacitance.

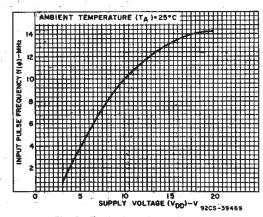


Fig. 8 - Typical maximum input pulse frequency vs. supply voltage.

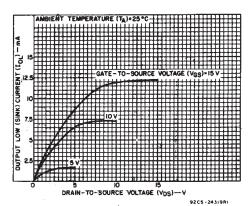


Fig. 3 - Minimum output low (sink) current characteristics.

ORAIN-TO-SOURCE VOLTAGE (VDS)—V

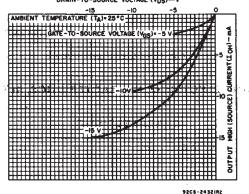


Fig. 5 - Minimum output high (source) current characteristics.

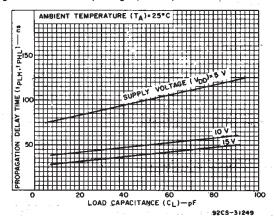


Fig. 7 - Typical propagation delay time $(Q_n \text{ to } Q_n + 1)$ as a function of load capacitance.

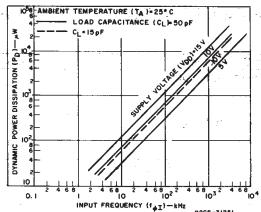
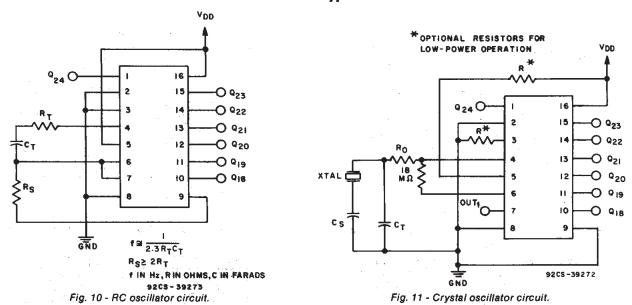


Fig. 9 - Typical dynamic power dissipation as a function of input frequency.



DYNAMIC ELECTRICAL CHARACTERISTICS, At TA = 25°C; Input t_r, t_f = 20 ns, CL = 50 pF, RL = 200 Ω

011404077010710		TEST CONDITIO	NS		LIMITS		UNITS
CHARACTERISTIC			V _{DD} (V)	Min.	Тур.	Max.	UNITS
Propagation Delay Time:	tpLH, tpHL	:	5	-	4.5	9	
Input to Q18		4.7	10	.— .	1.7	3.5	
			15		1.3	2.7	450
			- 5		6	12	μs
Input to Q24			10		2.2	4.5	
			15	-	1.7	3.5	
	. :		5	_	400	800	
Reset to Qn			10	4 ****	170	340	
			15	_	120	240	
Transition Time*	t _{THL} , t _{TLH}	*-	5	_	100	200	
.			10	. —	50	100	
			15		40	80	ns
Minimum Input Pulse Width	t _w ϕ		5	: - -	170	340	""
			10	-	75	150	
	<u> </u>		15		60	120]
Minimum Reset Pulse Width	t _{w(A)}	4 1 7 .	5	_	90	180	
			10	-	40	80	
		<u></u>	15		25	50	
Maximum Input Pulse Frequency	fφ		5	2	4	-	l
and the second s			10	5	10	-	MHz
			15	6.5	13		
Input Pulse Rise or Fall Time	$t_r \phi$, $t_f \phi$.5		-	15	1
A Commence of the Commence of			10		_	15	μs
			15	_		15	
Input Capacitance	Cin	Any Input			5	7.5	pF
R _T Operating Range		the state of the state of	5	1K	-	10M	
			10.	1K	-	10M	Ω
		<u> </u>	15	1K		10M	
C _T Operating Range			5	15p	-	10μ	
		1	10	15p	-	10μ	F
	<u> </u>		15	15p		10μ	<u> </u>
Maximum Oscillator Frequency		R _T =1 KΩ	5	0.5	0.7	0.9	1
		C _τ =15 pF	10	1.2	1.5	1.8	MHz
<u> </u>		R _s =30 KΩ	15	1.7	2.1	2.5	

^{*}Not applicable for pin 4 (OUT2).

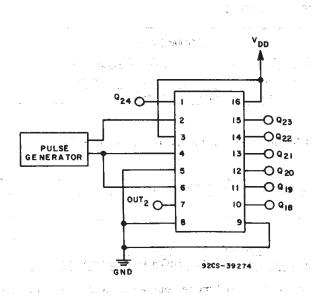


Fig. 12 - Functional test circuit.

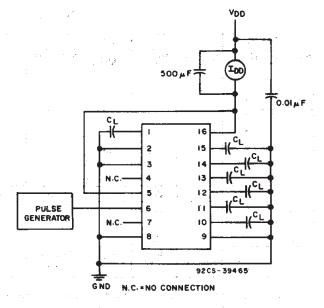


Fig. 13 - Dynamic power dissipation test circuit.

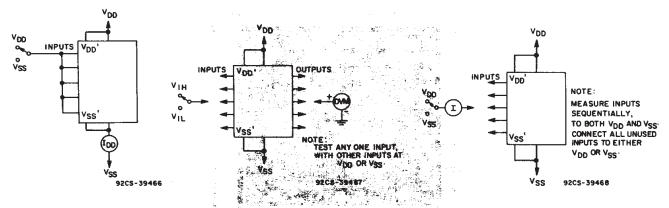


Fig. 14 - Quiescent device current.

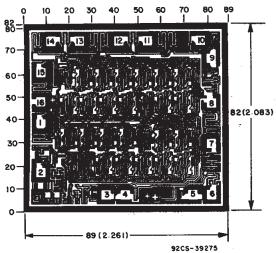
Fig. 15 - Input voltage.

Fig. 16 - Input current.

FUNCTIONAL TEST SEQUENCE

INPUTS			OÚ.	TPUTS	T	COMMENTS		
RESET	IN 2	OUT 2	V _{SS} '	V _{DD} '	Q18-Q24	COMMENTS		
						Counter is in three 8-stage sections in parallel mode.		
1	0	0	Vpp	Vss	LOW	Counter is reset. IN 2 and OUT 2 are tied together.		
0	1	1	Vop	Vss		First LOW-to-HIGH transition at IN 2.		
	0	0						
	1	1 1						
0	_	_	V _{DD}	Vss	1	255 LOW-to-HIGH transitions are clocked in at IN 2.		
	_	-	_			•		
	_	1 -						
0	1 ;	1	V _{DD}	Vss	HIGH	The 255th LOW-to-HIGH transition.		
0	0	0	VDD	Vss	HIGH			
0	0	0	Vss	Vss	HIGH	Counter is converted back to 24-stage serial-mode operation.		
0	1	0	Vss	VDD	HIGH			
0	1	1	Vss	V _{DD}	HIGH	OUT 2 reverts to output operation.		
0	0	<u> </u>	Vss	V _{DD}	LOW	Counter ripples from an all-HIGH state to an all-LOW state.		

A test function, which divides, has been included to reduce the time required to test all 24 stages of the counter. Three sections are loaded in parallel to 255 counts, forcing all the outputs to be in the HIGH state. The counter is changed back to serial-mode operation and one additional LOW-to-HIGH transition is entered at IN 2, which causes the outputs to ripple from an all-HIGH state to an all-LOW state.



Dimensions and pad layout for CD4521BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch) .

PACKAGE OPTION ADDENDUM

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4521BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4521BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4521BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BMTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



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retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4521BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4521BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
Γ	CD4521BM96	SOIC	D	16	2500	333.2	345.9	28.6
Γ	CD4521BNSR	SO	NS	16	2000	346.0	346.0	33.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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