

**STRUCTURE** Silicon Monolithic Integrated Circuit

**PRODUCT NAME** BU9718KV

**FUNCTION** 96 Segment Driver

**FEATURE**

- Up to 32 segment outputs and 3 common outputs can be displayed, for a total of 96 segments.
- 1/3 duty display
- Each 1/2 or 1/3 can be selected for power supply for LCD display.

○ **ABSOLUTE MAXIMUM RATINGS** ( $T_a=25^{\circ}\text{C}$ ,  $V_{SS}=0\text{V}$ )

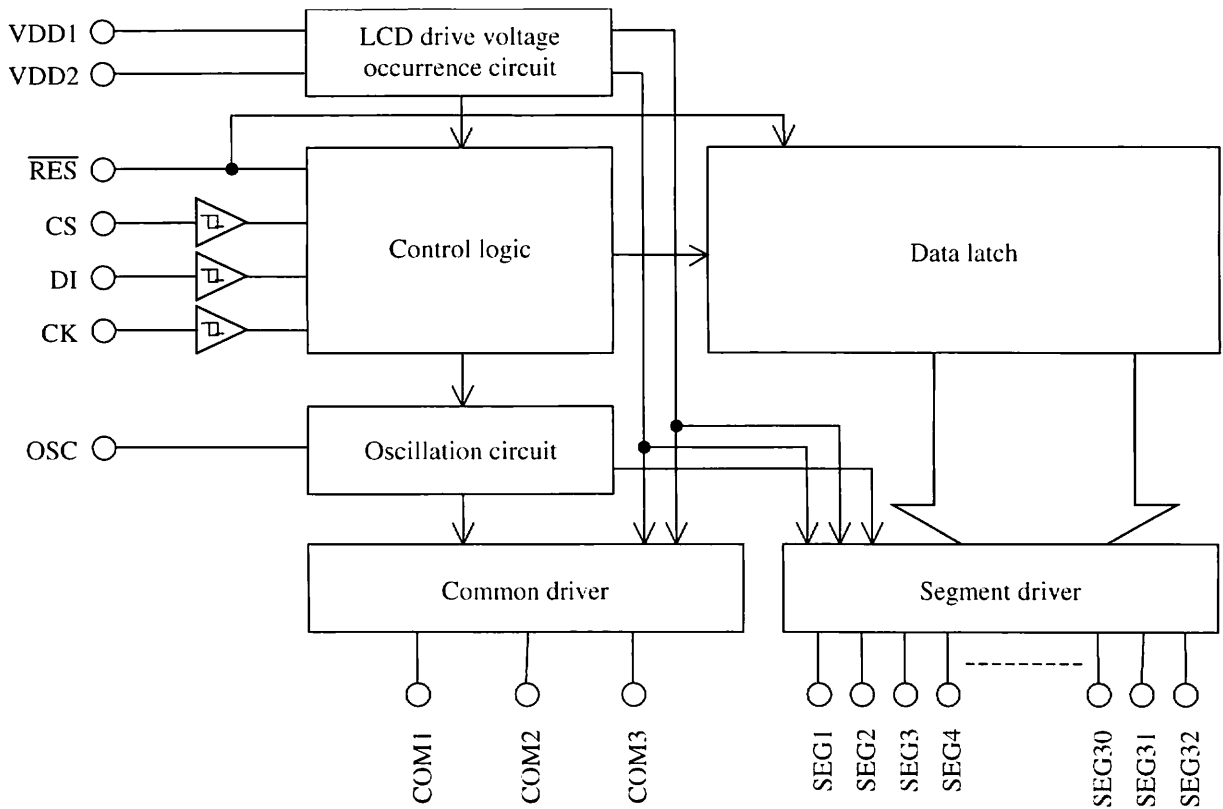
Parameter	Symbol	Terminal	Limits	Unit
Maximum power supply voltage	VDD	VDD	-0.3~+7.0	V
Input voltage	VIN	OSC, CS, CK, DI, $\overline{\text{RES}}$	-0.3~VDD+0.3	V
Output voltage	VOUT	OSC	-0.3~VDD+0.3	V
Output current	ISO	S1~S32	300	mA
	ICO	COM1~COM3	3	mA
Power dissipation	Pd	-	400 <sup>*1</sup>	mW
Surrounding temperature Range	Tstg	-	-55~+125	°C

\*1: Power dissipation is done at 4.0mW/°C for operation above  $T_a \geq 25^{\circ}\text{C}$ .

○ **RECOMMENDED OPERATING RANGE** ( $T_a=25^{\circ}\text{C}$ ,  $V_{SS}=0\text{V}$ )

Parameter	Symbol	Terminal	Min.	Typ.	Max.	Unit
Power supply voltage	VDD	VDD	+2.7		+3.5	V
Input voltage	VDD1	VDD1	0	2/3VDD	VDD	V
	VDD2	VDD2	0	1/3VDD	VDD	V
External Input wave frequency	fOSC	OSC	-	38	100	kHz
Recommended external resistor	R	OSC	-	47	-	k $\Omega$
Recommended external capacitor	C	OSC	-	1000	-	pF
Operating Temperature	Topr	—	-40	-	+85	°C

○ BLOCK DIAGRAM



○ ELECTRICAL CHARACTERISTICS

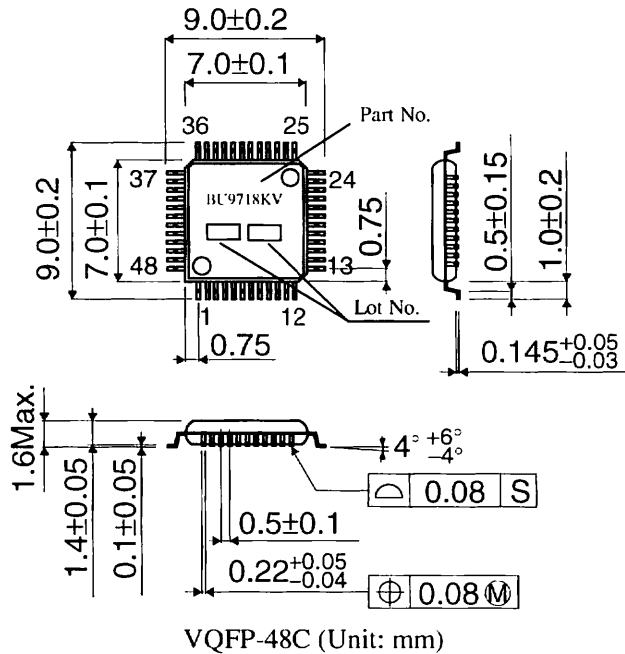
DC CHARACTERISTICS (Unless Otherwise Specified VDD=2.75~3.5V, VSS=0V, Ta=25°C)

Parameter	Symbol	Terminal	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	VIH	CS, CK, DI, $\overline{\text{RES}}$		0.8VDD	-	VDD	V
"L" Input Voltage	VIL	CS, CK, DI, $\overline{\text{RES}}$		0	-	0.2VDD	V
"H" Input Current	IIH	CS, CK, DI, $\overline{\text{RES}}$	VI=VDD	0	-	6.0	$\mu\text{A}$
"L" Input Current	IIL	CS, CK, DI, $\overline{\text{RES}}$	VI=VSS	0	-	6.0	$\mu\text{A}$
"H" Output Voltage	VSOH	S1~S32	IO=-20mA	-	VDD-1.0	-	V
	VCOH	COM1~COM3	IO=-100mA	-	VDD-1.0	-	V
"H" Output Voltage	VSOL	S1~S32	IO=20mA	-	1.0	-	V
	VCOL	COM1~COM3	IO=100mA	-	1.0	-	V
Center-Level Output Voltage	VCM1	COM1~COM3	1/2bias	-	1/2VDD	-	V
	VSM1	S1~S32	1/3bias	-	2/3VDD	-	V
	VCM2	COM1~COM3	1/3bias	-	2/3VDD	-	V
	VSM2	S1~S32	1/3bias	-	1/3VDD	-	V
	VCM3	COM1~COM3	1/3bias	-	1/3VDD	-	V
Power supply electric current	IQ		Low-power Mode	-	30	70	$\mu\text{A}$
	IDD		fOSC=38kHz	-	200	500	$\mu\text{A}$

AC CHARACTERISTICS (Unless Otherwise Specified VDD=2.7V~3.5V、Ta=25°C)

Parameter	Symbol	Terminal	Min.	Typ.	Max.	Unit	Condition
Oscillator frequency guaranteed range	fOSC	OSC	10	38	80	kHz	R=47k Ω,C=1000pF
Oscillation guarantee range	fOSC	OSC	-	-	100	kHz	External Inputs
Data set up time	tDS	CK, DI	200	-	-	ns	
Data hold time	tDH	CK, DI	200	-	-	ns	
CS setup time	tCS	CS, CK	200	-	-	ns	
CS hold time	tCH	CS, CK	200	-	-	ns	
"H" CK pulse width	tCKH	CK	200	-	-	ns	
"L" CK pulse width	tCKL	CK	200	-	-	ns	
Rise Time	tr	CS, CK, DI	-	-	100	ns	
Fall Time	tf	CS, CK, DI	-	-	100	ns	

○ Contour dimension figure, marking



○ Terminal number, terminal name

Terminal No.	Terminal name	Terminal No.	Terminal name	Terminal No.	Terminal name	Terminal No.	Terminal name
1	S1	13	S12	25	N.C.	37	COM2
2	S2	14	S13	26	S23	38	COM3
3	S3	15	S14	27	S24	39	$\overline{\text{RES}}$
4	S4	16	S15	28	S25	40	VDD
5	S5	17	S16	29	S26	41	VDD1
6	S6	18	S17	30	S27	42	VDD2
7	S7	19	S18	31	S28	43	VSS
8	S8	20	S19	32	S29	44	OSC
9	S9	21	S20	33	S30	45	CS
10	S8	22	S21	34	S31	46	CK
11	S9	23	S22	35	S32	47	DI
12	N.C.	24	N.C.	36	COM1	48	N.C.

## ○ Cautions on use

- (1) Absolute Maximum Ratings  
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.
- (2) Operating conditions  
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.
- (3) Reverse connection of power supply connector  
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.
- (4) Power supply line  
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.  
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.
- (5) GND voltage  
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state.  
Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.
- (6) Short circuit between terminals and erroneous mounting  
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.
- (7) Operation in strong electromagnetic field  
Be noted that using ICs in the strong electromagnetic field can malfunction them.
- (8) Inspection with set PCB  
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress.  
Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.
- (9) Input terminals  
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.
- (10) Ground wiring pattern  
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.
- (11) External capacitor  
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.
- (12) No Connecting input terminals  
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

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