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- 12-Bit Voltage Output DAC
- Programmable Settling Time vs Power Consumption
 - 3 μ s in Fast Mode 9 μ s in Slow Mode
- Ultra Low Power Consumption: 900 μW Typ in Slow Mode at 3 V 2.1 mW Typ in Fast Mode at 3 V
- Differential Nonlinearity . . . < 0.5 LSB Typ
- Compatible With TMS320 and SPI Serial Ports
- Power-Down Mode (10 nA)
- Buffered High-Impedance Reference Input

description

The TLV5616 is a 12-bit voltage output digital-to-analog converter (DAC) with a flexible 4-wire serial interface. The 4-wire serial interface allows glueless interface to TMS320, SPI, QSPI, and Microwire serial ports. The TLV5616 is programmed with a 16-bit serial string containing 4 control and 12 data bits. Developed for a wide range of supply voltages, the TLV5616 can operate from 2.7 V to 5.5 V.

- Voltage Output Range ... 2 Times the Reference Input Voltage
- Monotonic Over Temperature
- Available in MSOP Package

applications

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

,	·	or P I op Vie		CKAGE
DIN [1	υ	8] V _{DD}
SCLK [2		7] OUT
CS [3		6] REFIN
FS [4		5] AGND

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class AB output stage to improve stability and reduce settling time. The settling time of the DAC is programmable to allow the designer to optimize speed versus power dissipation. The settling time is chosen by the control bits within the 16-bit serial input string. A high-impedance buffer is integrated on the REFIN terminal to reduce the need for a low source impedance drive to the terminal.

Implemented with a CMOS process, the TLV5616 is designed for single supply operation from 2.7 V to 5.5 V. The device is available in an 8-terminal SOIC package. The TLV5616C is characterized for operation from 0°C to 70°C. The TLV5616I is characterized for operation from -40° C to 85°C.

		AVAILABLE	E OPTIONS	
			PACKAGE	
	Τ _Α	SMALL OUTLINE [†] (D)	MSOP (DGK)	PLASTIC DIP (P)
0	°C to 70°C	TLV5616CD	TLV5616CDGK	TLV5616CP
-4	0°C to 85°C	TLV5616ID	TLV5616IDGK	TLV5616IP

 † Available in tape and reel as the TLV5616CDR and the TLV5616IDR



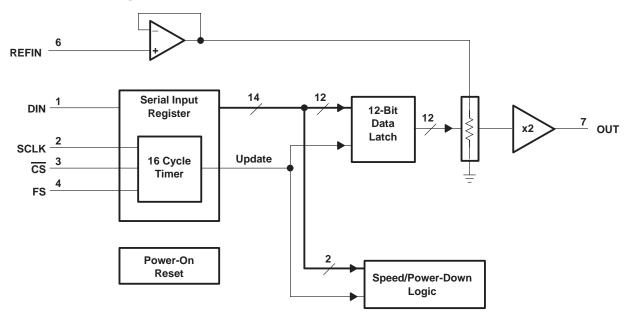
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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functional block diagram



Terminal Functions

TERMI	NAL		
NAME	NO.	1/0	DESCRIPTION
AGND	5		Analog ground
CS	3	I	Chip select. Digital input used to enable and disable inputs, active low.
DIN	1	I	Serial digital data input
FS	4	Т	Frame sync. Digital input used for 4-wire serial interfaces such as the TMS320 DSP interface.
OUT	7	0	DAC analog output
REFIN	6	I	Reference analog input voltage
SCLK	2	I	Serial digital clock input
V _{DD}	8		Positive power supply



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage (V _{DD} to AGND)	
Reference input voltage range	
Digital input voltage range	– 0.3 V to V _{DD} + 0.3 V
Operating free-air temperature range, T _A : TLV5616C	0°C to 70°C
TLV5616I	40°C to 85°C
Storage temperature range, T _{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		Ν	/IN	NOM	MAX	UNIT
	$V_{DD} = 5 V$		4.5	5	5.5	V
Supply voltage, V _{DD}	$V_{DD} = 3 V$		2.7	3	3.3	V
Lligh lovel digital input valtage Mus	$DV_{DD} = 2.7 V$		2			V
High-level digital input voltage, VIH	DV _{DD} = 5.5 V		2.4			V
Low level digital input voltage Ve	DV _{DD} = 2.7 V				0.6	V
Low-level digital input voltage, V_{IL}	DV _{DD} = 5.5 V				1	V
Reference voltage, Vref to REFIN terminal	$V_{DD} = 5 V$ (see Note 1)	AG	ND	2.048	V _{DD} -1.5	V
Reference voltage, Vref to REFIN terminal	$V_{DD} = 3 V$ (see Note 1)	AG	ND	1.024	V _{DD} -1.5	V
Load resistance, RL			2	10		kΩ
Load capacitance, CL					100	pF
Clock frequency, fCLK					20	MHz
Operating free air temperature T	TLV5616C		0		70	°C
Operating free-air temperature, T _A	TLV5616I	-	-40		85	°C

NOTE 1: Due to the x2 output buffer, a reference input voltage $\geq V_{DD/2}$ causes clipping of the transfer function.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

power supply

	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
			V_{DD} = 5 V, VREF = 2.048 V, No load,	Fast		0.9	1.35	mA
laa Power supply current		All inputs = AGND or V_{DD} , DAC latch = 0x800	Slow		0.4	0.6	mA	
סטי	IDD Power supply current		V_{DD} = 3 V, VREF = 1.024 V No load,			0.7	1.1	mA
		All inputs = AGND or V_{DD} , DAC latch = 0x800		Slow		0.3	0.45	mA
	Power down supply current (see Figure	e 12)				10		nA
PSRR		Zero scale	See Note 2			-80		dB
PORK	Power supply rejection ratio	Full scale	See Note 3			-80		uВ
	Power on threshold voltage, POR					2		V

NOTES: 2. Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by:

 $PSRR = 20 \log [(E_{ZS}(V_{DD}max) - E_{ZS}(V_{DD}min))/V_{DD}max]$

3. Power supply rejection ratio at full scale is measured by varying $V_{\mbox{DD}}$ and is given by:

PSRR = 20 log [(E_G(V_{DD}max) – E_G(V_{DD}min))/V_{DD}max]



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

static DAC specifications R_L = 10 kΩ, C_L = 100 pF

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			12	12	bits
INL	Integral nonlinearity	See Note 4		±1.9	±4	LSB
DNL	Differential nonlinearity	See Note 5		± 0.5	± 1	LSB
EZS	Zero-scale error (offset error at zero scale)	See Note 6			±10	mV
	Zero-scale-error temperature coefficient	See Note 7		10		ppm/°C
EG	Gain error	See Note 8			±0.6	% of FS voltage
	Gain-error temperature coefficient	See Note 9		10		ppm/°C

NOTES: 4. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors. Tested from code 10 to code 4095.

5. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code. Tested from code 10 to code 4095.

6. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.

7. Zero-scale-error temperature coefficient is given by: $E_{ZS} TC = [E_{ZS} (T_{max}) - E_{ZS} (T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$. 8. Gain error is the deviation from the ideal output ($2V_{ref} - 1 LSB$) with an output load of 10 k Ω excluding the effects of the zero-error. 9. Gain temperature coefficient is given by: $E_G TC = [E_G(T_{max}) - E_G (T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.

output specifications

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VO	Voltage output range	RL = 10 kΩ	0		AV _{DD} -0.1	V
	Output load regulation accuracy	$R_L = 2 k\Omega$, vs 10 k Ω		0.1	±0.25	% of FS voltage

reference input (REF)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
VI	Input voltage range			0		V _{DD} -1.5	V
RI	Input resistance				10		MΩ
Cl	Input capacitance				5		pF
	Defense a location de late		Slow		525		kHz
	Reference input bandwidth	$REFIN = 0.2 V_{pp} + 1.024 V dc$	Fast		1.3		MHz
	Reference feed through	REFIN = 1 V _{pp} at 1 kHz + 1.024 V dc (see Note 10)			-75		dB

NOTE 10: Reference feedthrough is measured at the DAC output with an input code = 0x000.

digital inputs

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Iн	High-level digital input current	$V_I = V_{DD}$			±1	μA
١ _{IL}	Low-level digital input current	$V_{I} = 0 V$			±1	μA
Cl	Input capacitance			3		pF



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operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

analog output dynamic performance

	PARAMETER	TEST	CONDITIONS		MIN	TYP	MAX	UNIT
	Ordered a still and incention	R _L = 10 kΩ, ^C	С _L = 100 рF,	Fast		3	5.5	_
^t s(FS)	Output settling time, full scale	See Note 11		Slow		9	20	μs
		$R_L = 10 k\Omega$, C	C _L = 100 pF,	Fast		1		μs
^t s(CC)	Output settling time, code to code	See Note 12		Slow		2		μs
0.0	Olympicate	R _L = 10 kΩ, 0	C _L = 100 pF,	Fast		3.6		N// -
SR	Slew rate	See Note 13	_	Slow		0.9		V/µs
	Glitch energy	Code transition fro	om 0x7FF to 0x80	0		10		nV–s
S/N	Signal to noise					74		dB
S/(N+D)	Signal to noise + distortion		out = 1.1 kHz ,			66		dB
THD	Total harmonic distortion	$R_L = 10 k\Omega$, C BW = 20 kHz	C _L = 100 pF,			-68		dB
	Spurious free dynamic range					70		dB

NOTES: 11. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x080 to 0x3FF or 0x3FF to 0x080. Not tested, ensured by design.

12. Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of one count. Code change from 0x1FF to 0x200. Not tested, ensured by design.

13. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

digital input timing requirements

		MIN	NOM	MAX	UNIT
tsu(CS-FS)	Setup time, $\overline{\text{CS}}$ low before FS \downarrow	10			ns
^t su(FS–CK)	Setup time, FS low before first negative SCLK edge	8			ns
^t su(C16–FS)	Setup time, sixteenth negative edge after FS low on which bit D0 is sampled before rising edge of FS $$	10			ns
^t su(C16–CS)	Setup time, sixteenth positive SCLK edge (first positive after D0 is sampled) before \overline{CS} rising edge. If FS is used instead of the sixteenth positive edge to update the DAC, then the setup time is between the FS rising edge and \overline{CS} rising edge.	10			ns
t _{wH}	Pulse duration, SCLK high	25			ns
t _{wL}	Pulse duration, SCLK low	25			ns
^t su(D)	Setup time, data ready before SCLK falling edge	8			ns
^t h(D)	Hold time, data held valid after SCLK falling edge	5			ns
^t wH(FS)	Pulse duration, FS high	20			ns



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PARAMETER MEASUREMENT INFORMATION

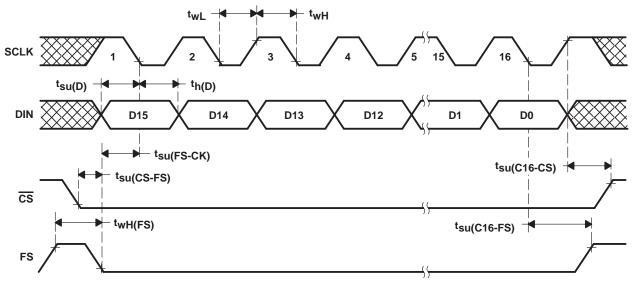
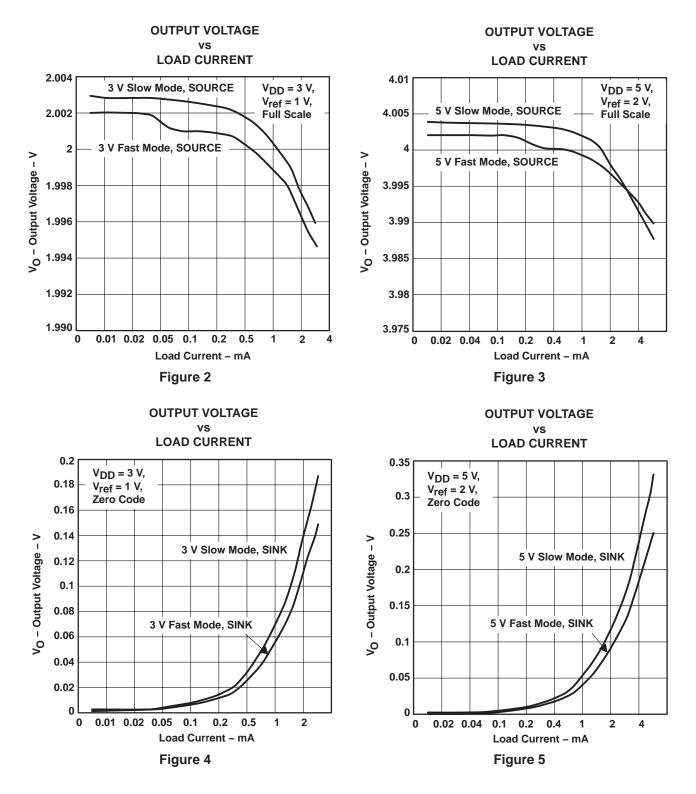


Figure 1. Timing Diagram



TLV5616C, TLV5616I 2.7-V TO 5.5-V LOW POWER 12-BIT DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN SLAS152D – DECEMBER 1997 – REVISED APRIL 2004

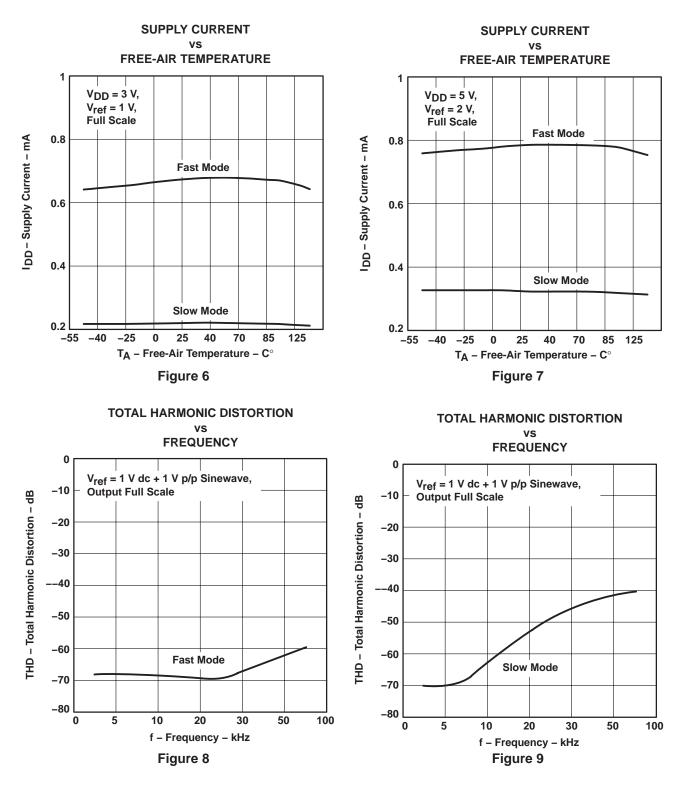
TYPICAL CHARACTERISTICS





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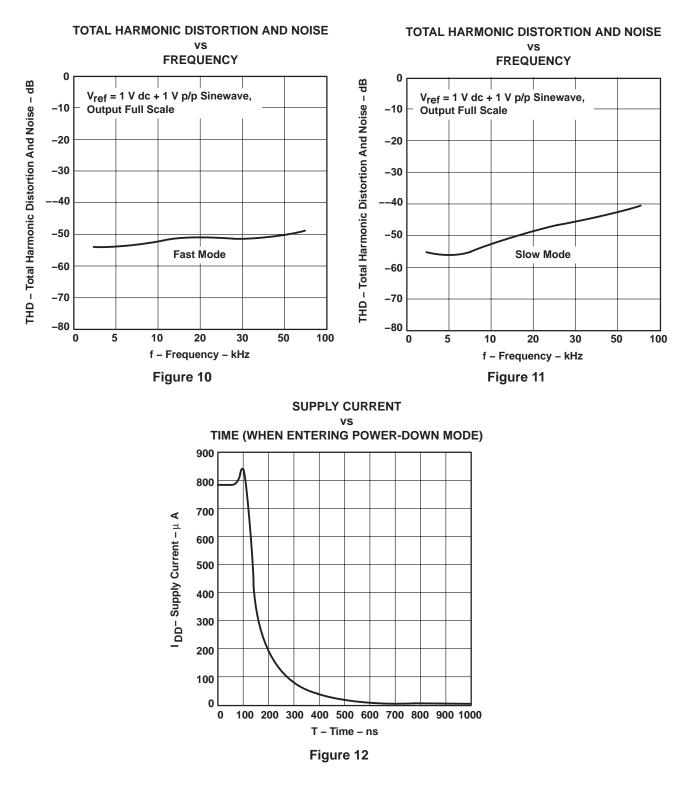
TYPICAL CHARACTERISTICS





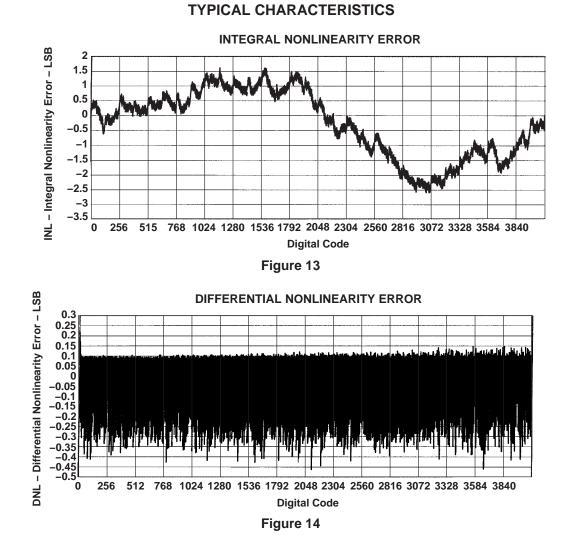
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TYPICAL CHARACTERISTICS





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APPLICATION INFORMATION

general function

The TLV5616 is a 12-bit single supply DAC based on a resistor string architecture. The device consists of a serial interface, speed and power-down control logic, a reference input buffer, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by external reference) is given by:

where REF is the reference voltage and CODE is the digital input value within the range of 0_{10} to 2^{n-1} , where n = 12 (bits). The 16-bit data word, consisting of control bits and the new DAC value, is illustrated in the *data format* section. A power-on reset initially resets the internal latches to a defined state (all bits zero).

serial interface

Explanation of data transfer: First, the device has to be enabled with \overline{CS} set to low. Then, a falling edge of FS starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or FS rises, the content of the shift register is moved to the DAC latch which updates the voltage output to the new level.

The serial interface of the TLV5616 can be used in two basic modes:

- Four wire (with chip select)
- Three wire (without chip select)

Using chip select (four wire mode), it is possible to have more than one device connected to the serial port of the data source (DSP or microcontroller). The interface is compatible with the TMS320 family. Figure 15 shows an example with two TLV5616s connected directly to a TMS320 DSP.

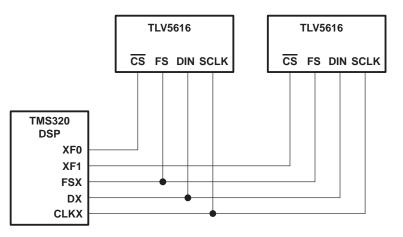


Figure 15. TMS320 Interface



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APPLICATION INFORMATION

serial interface (continued)

If there is no need to have more than one device on the serial bus, then \overline{CS} can be tied low. Figure 16 shows an example of how to connect the TLV5616 to a TMS320, SPI, or Microwire port using only three pins.

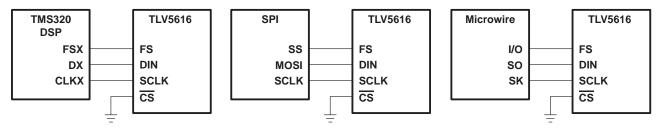


Figure 16. Three-Wire Interface

Notes on SPI and Microwire: Before the controller starts the data transfer, the software has to generate a falling edge on the I/O pin connected to FS. If the word width is 8 bits (SPI and Microwire), two write operations must be performed to program the TLV5616. After the write operation(s), the DAC output is updated automatically on the next positive clock edge following the sixteenth falling clock edge.

serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$f_{SCLKmax} = \frac{1}{t_{wH(min)} + t_{wL(min)}} = 20 \text{ MHz}$$

The maximum update rate is:

$$f_{UPDATEmax} = \frac{1}{16 \left(t_{wH(min)} + t_{wL(min)}\right)} = 1.25 \text{ MHz}$$

The maximum update rate is a theoretical value for the serial interface, since the settling time of the TLV5616 has to be considered also.

data format

The 16-bit data word for the TLV5616 consists of two parts:

	Control bits	(D15 D12)
--	--------------	-----------

• New DAC value (D11...D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Х	SPD	PWR	Х	New DAC value (12 bits)											

X: don't care

SPD: Speed control bit. $1 \rightarrow fast mode$ $0 \rightarrow slow mode$

PWR: Power control bit. $1 \rightarrow \text{power down} \quad 0 \rightarrow \text{normal operation}$

In power-down mode, all amplifiers within the TLV5616 are disabled.



APPLICATION INFORMATION

TLV5616 interfaced to TMS320C203 DSP

hardware interfacing

Figure 17 shows an example how to connect the TLV5616 to a TMS320C203 DSP. The serial interface of the TLV5616 is ideally suited to this configuration, using a maximum of four wires to make the necessary connections. In applications where only one synchronous serial peripheral is used, the interface can be simplified even further by pulling \overline{CS} low all the time as shown in the figure.

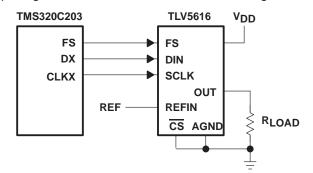


Figure 17. TLV5616 to DSP Interface

software

No setup procedure is needed to access the TLV5616. The output voltage can be set using just a single command.

out data_addr, SDTR

where data_addr points to an address location holding the control bits and the 12 data bits providing the output voltage data. SDTR is the address of the transmit FIFO of the synchronous serial port.

The following code shows how to use the timer of the TMS320C203 as a time base to generate a voltage ramp with the TLV5616.

A timer interrupt is generated every 205 μ s. The corresponding interrupt service routine increments the output code (stored at 0x0064) for the DAC, adds the DAC control bits to the four most significant bits, and writes the new code to the TLV5616. The resulting period of the saw waveform is:

 $\pi = 4096 \times 205 \text{ E-6 s} = 0.84 \text{ s}$

```
*******
;* Title : Ramp generation with TLV5616
;* Version : 1.0
;* DSP
       : TI TMS320C203
;* © (1998) Texas Instruments Incorporated
;----- I/O and memory mapped regs ------
    .include "regs.asm"
 ----- vectors ------
                          _____
     .ps
           0h
     b
            start
     b
           INT1
     b
            INT23
     b
            TIM ISR
```



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APPLICATION INFORMATION

```
;* Main Program
1000h
    .ps
    .entry
start:
; disable interrupts
                    ; disable maskable interrupts
    setc INTM
           #0ffffh, IFR
    splk
           #0004h, IMR
    splk
; set up the timer to interrupt ever 205uS
          #0000h, 60h
    splk
           #00FFh, 61h
    splk
    out
          61h, PRD
           60h, TIM
    out
          #0c2fh, 62h
    splk
           62h, TCR
    out
; Configure SSP to use internal clock, internal frame sync and burst mode
        #0CC0Eh, 63h
    splk
           63h, SSPCR
    out
           #0CC3Eh, 63h
    splk
           63h, SSPCR
    out
           #0000h, 64h ; set initial DAC value
    splk
; enable interrupts
           INTM
                   ; enable maskable interrupts
    clrc
; loop forever!
    idle
next:
                    ;wait for interrupt
      b
           next
; all else fails stop here
                    ; hang there
done: b done
;* Interrupt Service Routines
INT1:
      ret
                    ;do nothing and return
INT23:
       ret
                    ;do nothing and return
TIM_ISR:
                   ; restore counter value to ACC
       lacl
          64h
                   ; increment DAC value
       add
           #1h
           #0FFFh
       and
                    ; mask 4 MSBs
                    ; store 12 bit counter value
       sacl 64h
                    ; set DAC control bits
           #4000h
       or
       sacl 65h
                    ; store DAC value
       out 65h, SDTR ; send data
                   ; re-enable interrupts
       clrc intm
       ret
.END
```



APPLICATION INFORMATION

TLV5616 interfaced to MCS51[®] microcontroller

hardware interfacing

Figure 18 shows an example of how to connect the TLV5616 to an MCS51[®] compatible microcontroller. The serial DAC input data and external control signals are sent via I/O port 3 of the controller. The serial data is sent on the RxD line, with the serial clock output on the TxD line. P3.4 and P3.5 are configured as outputs to provide the chip select and frame sync signals for the TLV5616.

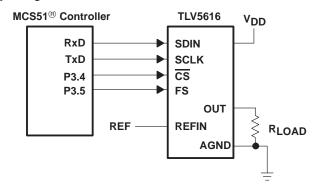


Figure 18. TLV5616 to MCS51[®] Controller Interface

software

The example program puts out a sine wave on the OUT pin.

The on-chip timer is used to generate interrupts at a fixed frequency. The related interrupt service routine fetches and writes the next sample to the DAC. The samples are stored in a lookup table, which describes one full period of a sine wave.

The serial port of the controller is used in mode 0, which transmits 8 bits of data on RxD, accompanied by a synchronous clock on TxD. Two writes concatenated together are required to write a complete word to the TLV5616. The CS and FS signals are provided in the required fashion through control of I/O port 3, which has bit addressable outputs.

```
*****
;* Title : Ramp generation with TLV5616
;* Version : 1.0
                                                                            *
;* MCU : INTEL MCS51<sup>®</sup>
;* © (1998) Texas Instruments Incorporated
; Program function declaration
;---
NAME
     GENSINE
MAIN
     SEGMENT
                 CODE
ISR
     SEGMENT
                 CODE
SINTBL SEGMENT
                 CODE
VAR1
     SEGMENT
                 DATA
STACK SEGMENT
                 IDATA
; Code start at address 0, jump to start
   ____
  CSEG AT 0
```

```
MCS is a registered trademark of Intel Corporation
```



TLV5616C, TLV5616I 2.7-V TO 5.5-V LOW POWER 12-BIT DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN SLAS152D – DECEMBER 1997 – REVISED APRIL 2004

APPLICATION INFORMATION

COUC III	the timer0 interru	npt vector
CSEG A		
		mp vector for timer 0 interrupt is 000Bh
Define	program variables	
RSEG	VAR1	
	otr: DS 1	
Interru	pt service routine	for timer 0 interrupts
RSEG	ISR	
imer0isr	`:	
PUSH PUSH	PSW ACC	
CLR CLR		; set CSB low ; set FS low
; roll	ling_ptr, rolls rour n interrupt (at the DPTR,#sinevals	<pre>vals as 32 samples of msb, lsb pairs (64 bytes). The pointe nd the table of samples incrementing by 2 bytes (1 sample) end of this routine). ; set DPTR to the start of the table of sine signal values ; ACC loaded with the pointer into the sine table</pre>
MOV	A, rorring_ptr	; ACC loaded with the pointer into the sine table
MOVC ORL MOV	А, #ООН	; get msb from the table ; set control bits ; send out msb of data word
ORL MOV	A, #00H SBUF,A rolling_ptr; move r A	; set control bits
ORL MOV MOVA,1 INC	A, #00H SBUF,A rolling_ptr; move r A A,@A+DPTR	; set control bits ; send out msb of data word olling pointer in to ACC ; increment ACC holding the rolling pointer
ORL MOV INC MOVC SB_TX: JNB CLR MOV	A, #00H SBUF,A rolling_ptr; move r A A,@A+DPTR TI, MSB_TX TI	; set control bits ; send out msb of data word rolling pointer in to ACC ; increment ACC holding the rolling pointer ; which is the lsb of this sample, now in ACC ; wait for transmit to complete ; clear for new transmit
ORL MOV MOVA, 1 INC MOVC ASB_TX: JNB CLR MOV ASB_TX: JNB SETB CLR MOV INC INC ANL	A, #00H SBUF,A rolling_ptr; move r A,@A+DPTR TI, MSB_TX TI SBUF,A TI, LSB_TX T1 TI A,rolling_ptr A A,#03FH	<pre>; set control bits ; send out msb of data word olling pointer in to ACC ; increment ACC holding the rolling pointer ; which is the lsb of this sample, now in ACC ; wait for transmit to complete ; clear for new transmit ; and send out the lsb ; wait for lsb transmit to complete ; set FS = 1 ; clear for new transmit ; load ACC with rolling pointer ; increment the ACC twice, to get next sample ; wrap back round to 0 if >64</pre>
ORL MOV MOVA, 1 INC MOVC ISB_TX: JNB CLR MOV SETB CLR MOV INC INC ANL MOV	A, #00H SBUF,A rolling_ptr; move r A A,@A+DPTR TI, MSB_TX TI SBUF,A TI, LSB_TX T1 TI A,rolling_ptr A A,#03FH rolling_ptr,A	<pre>; set control bits ; send out msb of data word olling pointer in to ACC ; increment ACC holding the rolling pointer ; which is the lsb of this sample, now in ACC ; wait for transmit to complete ; clear for new transmit ; and send out the lsb ; wait for lsb transmit to complete ; set FS = 1 ; clear for new transmit ; load ACC with rolling pointer ; increment the ACC twice, to get next sample ; wrap back round to 0 if >64 ; move value held in ACC back to the rolling pointer</pre>
ORL MOV MOVA, 1 INC MOVC ISB_TX: JNB CLR MOV LSB_TX: JNB SETB CLR MOV INC INC ANL	A, #00H SBUF,A rolling_ptr; move r A,@A+DPTR TI, MSB_TX TI SBUF,A TI, LSB_TX T1 TI A,rolling_ptr A A,#03FH	<pre>; set control bits ; send out msb of data word olling pointer in to ACC ; increment ACC holding the rolling pointer ; which is the lsb of this sample, now in ACC ; wait for transmit to complete ; clear for new transmit ; and send out the lsb ; wait for lsb transmit to complete ; set FS = 1 ; clear for new transmit ; load ACC with rolling pointer ; increment the ACC twice, to get next sample ; wrap back round to 0 if >64</pre>



TLV5616C, TLV5616I 2.7-V TO 5.5-V LOW POWER 12-BIT DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN SLAS152D – DECEMBER 1997 – REVISED APRIL 2004

APPLICATION INFORMATION

DS	STACK 10h	; 16 Byte Stack!
;; Main Pr	ogram	
RSEG	MAIN	
start: MOV	SP,#STACK-1 ;	first set Stack Pointer
CLR MOV MOV MOV	тно,#освн ;	set serial port 0 to mode 0 set timer 0 to mode 2 - auto-reload set TH0 for 16.67 kHs interrupts
SETB SETB		set FS = 1 set CSB = 1
SETB SETB		enable timer 0 interrupts enable all interrupts
MOV SETB	rolling_ptr,A TR0	; set rolling pointer to 0 ; start timer 0
always: SJMP RET	-	; while(1) !
; Table o	f 32 sine wave s	amples used as DAC data
, RSEG sinevals:	SINTBL	
DW	01000H	
DW	0903EH	
DW	05097H	
DW	0305CH	
DW	0B086H	
DW	070CAH	
DW	OFOEOH	
DW	0F06EH	
DW	0F039H	
DW	0F06EH	
DW	OFOEOH	
DW	070CAH	
DW	0B086H	
DW	0305CH	
DW	05097H	
DW	0903EH	
DW	01000H	
DW	06021H	
DW	0A0E8H	
DW	0C063H	
DW	040F9H	
DW	080B5H	
DW	0009FH	
DW	00051H	
DW	00026H	
DW	00051H	
DW	0009FH	
DW	080B5H	
DW	040F9H	
DW	0C063H	
DW	0A0E8H	
DW	06021H	
END		



SLAS152D - DECEMBER 1997 - REVISED APRIL 2004

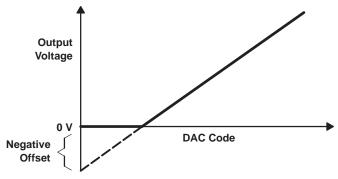
APPLICATION INFORMATION

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 19.





This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

power-supply bypassing and ground management

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane, making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1- μ F ceramic-capacitor bypass should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 20 shows the ground plane layout and bypassing technique.

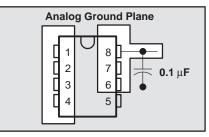


Figure 20. Power-Supply Bypassing



APPLICATION INFORMATION

definitions of specifications and terminology

integral nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

zero-scale error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

gain error (E_G)

Gain error is the error in slope of the DAC transfer function.

signal-to-noise ratio + distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

spurious free dynamic range (SFDR)

SFDR is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental signal and is expressed in decibels.





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TLV5616CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
TLV5616CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
TLV5616CDGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	GLevel-1-260C-UNLIM	Purchase Samples
TLV5616CDGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	GLevel-1-260C-UNLIM	Purchase Samples
TLV5616CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TLV5616CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TLV5616CP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
TLV5616CPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
TLV5616ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TLV5616IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TLV5616IDGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	GLevel-1-260C-UNLIM	Request Free Samples
TLV5616IDGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	GLevel-1-260C-UNLIM	Request Free Samples
TLV5616IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	GLevel-1-260C-UNLIM	Purchase Samples
TLV5616IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	GLevel-1-260C-UNLIM	Purchase Samples
TLV5616IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TLV5616IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TLV5616IP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
TLV5616IPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:



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ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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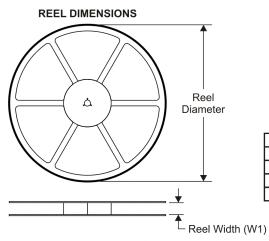
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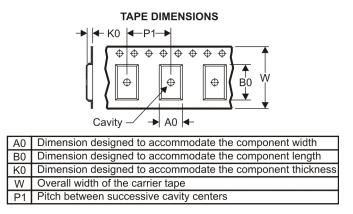
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All	dimensions are nominal												
	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	TLV5616CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
	TLV5616IDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
	TLV5616IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

27-Jan-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5616CDR	SOIC	D	8	2500	346.0	346.0	29.0
TLV5616IDGKR	MSOP	DGK	8	2500	346.0	346.0	29.0
TLV5616IDR	SOIC	D	8	2500	346.0	346.0	29.0

P(R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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