

Data sheet acquired from Harris Semiconductor

# CD54HC280, CD74HC280, CD54HCT280

# High-Speed CMOS Logic 9-Bit Odd/Even Parity Generator/Checker

November 1997 - Revised October 2003

#### **Features**

- Typical Propagation Delay = 17ns at  $V_{CC}$  = 5V,  $C_L$  = 15pF,  $T_A$  = 25°C
- · Replaces LS180 Types
- Easily Cascadable
- Fanout (Over Temperature Range)
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL}$  = 30%,  $N_{IH}$  = 30% of  $V_{CC}$  at  $V_{CC}$  = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V<sub>IL</sub>= 0.8V (Max), V<sub>IH</sub> = 2V (Min)
  - CMOS Input Compatibility,  $I_I \le 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

## Description

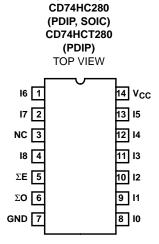
The 'HC280 and 'HCT280 are 9-bit odd/even parity, generator checker devices. Both even and odd parity outputs are available for checking or generating parity for words up to nine bits long. Even parity is indicated ( $\Sigma E$  output is high) when an even number of data inputs is high. Odd parity is indicated ( $\Sigma O$  output is high) when an odd number of data inputs is high. Parity checking for words larger than 9 bits can be accomplished by tying the  $\Sigma E$  output to any input of an additional HC/HCT280 parity checker.

## **Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC280F3A	-55 to 125	14 Ld CERDIP
CD54HCT280F3A	-55 to 125	14 Ld CERDIP
CD74HC280E	-55 to 125	14 Ld PDIP
CD74HC280MT	-55 to 125	14 Ld SOIC
CD74HC280M96	-55 to 125	14 Ld SOIC
CD74HCT280E	-55 to 125	14 Ld PDIP

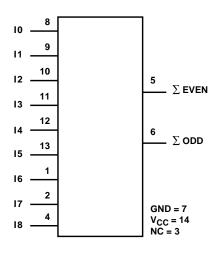
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

#### **Pinout**



CD54HC280, CD54HCT280 (CERDIP)

## Functional Diagram



### CD54HC280, CD74HC280, CD54HCT280, CD74HCT280

# **Absolute Maximum Ratings**

## 

#### **Thermal Information**

Thermal Resistance (Typical, Note1)	$\theta_{JA}$ (oC/W)
E (PDIP) Package	. 80
M (SOIC) Package	
Maximum Junction Temperature	
Maximum Storage Temperature Range	65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC - Lead Tips Only)	

#### **Operating Conditions**

Temperature Range, $T_A$ 55°C to 125°C Supply Voltage Range, $V_{CC}$
HC Types2V to 6V
HCT Types
DC Input or Output Voltage, V <sub>I</sub> , V <sub>O</sub>
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## **DC Electrical Specifications**

			ST ITIONS			25°C		-40°C T	O 85°C	-55°C T	O 125°C	
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES												
High Level Input	V <sub>IH</sub>	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output	∨он	V <sub>IH</sub> or	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
Voltage CMOS Loads		V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output		,	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Voltage TTL Loads			-5.2	6	5.48	ı	-	5.34	-	5.2	-	V
Low Level Output	V <sub>OL</sub>	V <sub>IH</sub> or	0.02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads		$V_{IL}$	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
000 20000			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output	1		4	4.5	-	-	0.26	-	0.33	-	0.4	V
Voltage TTL Loads			5.2	6	-	-	0.26	Ī	0.33	-	0.4	V
Input Leakage Current	lι	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μА
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μА

# CD54HC280, CD74HC280, CD54HCT280, CD74HCT280

# DC Electrical Specifications (Continued)

			ST ITIONS			25°C		-40°C TO 85°C		-55°C T	O 125 <sup>0</sup> C	
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HCT TYPES												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	Voн	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V <sub>CC</sub> to GND	0	5.5	-	-	±0.1	-	±1	-	±1	μА
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μА
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μА

#### NOTE:

## **HCT Input Loading Table**

INPUT	UNIT LOADS						
All	1						

NOTE: Unit Load is  $\Delta l_{CC}$  limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

# **Switching Specifications** Input $t_r$ , $t_f = 6ns$

		TEST		25 <sup>0</sup> C		-40°C TO 85°C	-55°C TO 125°C	
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	TYP	MAX	MAX	MAX	UNITS
HC TYPES								
Propagation Delay, Any Input to $\Sigma O$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	200	250	300	ns
			4.5	-	40	50	60	ns
			6	-	34	43	51	ns
		C <sub>L</sub> = 15pF	5	17	-	-	-	ns
Propagation Delay,	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	200	250	300	ns
Any Input to ΣE			4.5	-	40	50	60	ns
			6	-	34	43	51	ns
		C <sub>L</sub> = 15pF	5	17	-	-	-	ns

<sup>2.</sup> For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

# CD54HC280, CD74HC280, CD54HCT280, CD74HCT280

## Switching Specifications Input $t_r$ , $t_f$ = 6ns (Continued)

		TEST		25	°C	-40°C TO 85°C	-55°C TO 125°C	
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	TYP	MAX	MAX	MAX	UNITS
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	75	95	110	ns
			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Input Capacitance	C <sub>I</sub>	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	-	5	58	-	-	-	pF
HCT TYPES								•
Propagation Delay,	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	45	56	68	ns
Any Input to ΣO		C <sub>L</sub> = 15pF	5	19	-	-	-	ns
Propagation Delay,	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	42	53	63	ns
Any Input to ΣE		C <sub>L</sub> = 15pF	5	18	-	-	-	ns
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	4.5	-	15	19	22	ns
Input Capacitance	C <sub>IN</sub>	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	-	5	58	-	-	-	pF

#### NOTES:

- 3. C<sub>PD</sub> is used to determine the dynamic power consumption, per package.
   4. P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> f<sub>i</sub> (C<sub>PD</sub> + C<sub>L</sub>) where f<sub>i</sub> = Input Frequency, f<sub>O</sub> = Output Frequency, C<sub>L</sub> = Output Load Capacitance, V<sub>CC</sub> = Supply Voltage.

# Test Circuits and Waveforms

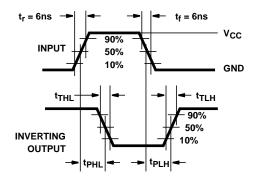


FIGURE 1. HC TRANSITION TIMES AND PROPAGATION **DELAY TIMES, COMBINATION LOGIC** 

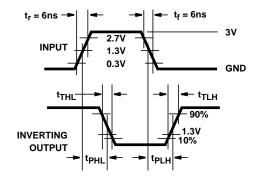


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION **DELAY TIMES, COMBINATION LOGIC** 



5-Sep-2011

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
8607701CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
CD54HC280F3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
CD54HCT280F3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
CD74HC280E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC280EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC280M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC280M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC280M96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC280MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC280MTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC280MTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT280E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT280EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



## PACKAGE OPTION ADDENDUM

5-Sep-2011

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL. Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF CD54HC280, CD54HCT280, CD74HC280, CD74HCT280:

Military: CD54HC280, CD54HCT280

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

# PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





Α	0	Dimension designed to accommodate the component width
В	0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
٧	٧	Overall width of the carrier tape
ГР	1	Pitch between successive cavity centers

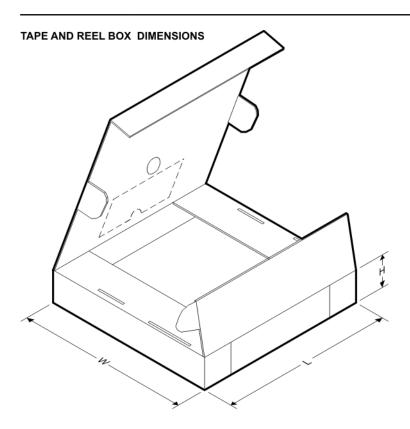
## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC280M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC280MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC280M96	SOIC	D	14	2500	346.0	346.0	33.0
CD74HC280MT	SOIC	D	14	250	346.0	346.0	33.0

# 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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