

16-CHANNEL LED DRIVER WITH DOT CORRECTION AND GRAYSCALE PWM CONTROL

FEATURES

- Qualified for Automotive Applications
- 16 Channels
- 12-Bit (4096 Steps) Grayscale PWM Control
- Dot Correction: 6 Bit (64 Steps)
- Drive Capability (Constant-Current Sink): 0 mA to 60 mA
- LED Power Supply Voltage up to 17 V
- $V_{CC} = 3.0\text{ V to }5.5\text{ V}$
- Serial Data Interface
- Controlled In-Rush Current
- 30-MHz Data Transfer Rate
- CMOS Level I/O
- Error Information
 - LOD: LED Open Detection
 - TEF: Thermal Error Flag

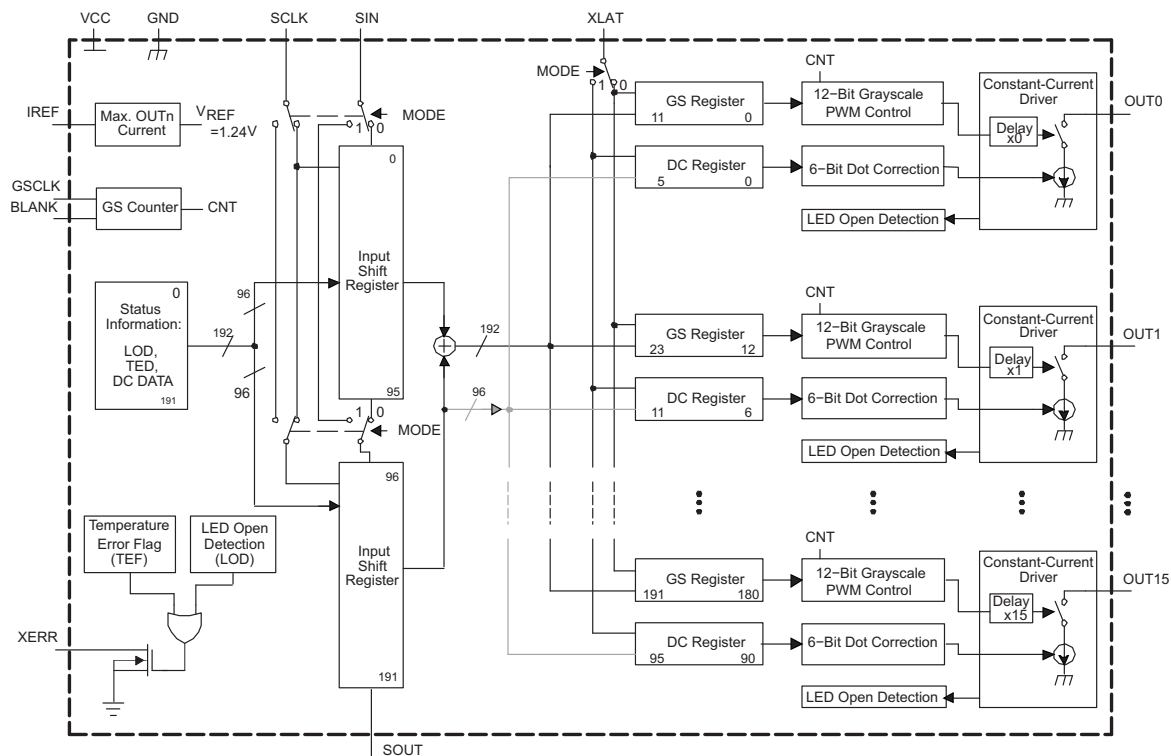
APPLICATIONS

- Monocolor, Multicolor, Full-Color LED Displays
- LED Signboards
- Display Back-Lighting

DESCRIPTION

The TLC5941 is a 16-channel, constant-current sink, LED driver. Each channel has an individually adjustable 4096-step grayscale PWM brightness control and a 64-step constant-current sink (dot correction). The dot correction adjusts the brightness variations between LED channels and other LED drivers. Both grayscale control and dot correction are accessible via a serial interface. A single external resistor sets the maximum current value of all 16 channels.

The TLC5941 features two error information circuits. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an overtemperature condition.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

T _J	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	PowerPAD™ HTSSOP – PWP	Reel of 2000	TLC5941QPWRQ1	TLC5941Q

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
 (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

V _I	Input voltage range ⁽²⁾	V _{CC}	–0.3 V to 6 V
I _O	Output current (dc)		90 mA
V _I	Input voltage range	V _(BLANK) , V _(SCLK) , V _(XLAT) , V _(MODE) , V _(SIN) , V _(GSCLK) , V _(IREF) , V _(TEST)	–0.3 V to V _{CC} + 0.3 V
V _O	Output voltage range	V _(SOUT) , V _(XERR)	–0.3 V to V _{CC} + 0.3 V
		V _(OUT0) to V _(OUT15)	–0.3 V to 18 V
T _{J(max)}	Operating junction temperature		150°C
T _{stg}	Storage temperature range		–55°C to 150°C
θ _{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾		31.58°C/W

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
 (2) All voltage values are with respect to network ground terminal.
 (3) The package thermal impedance is calculated in accordance with JESD 51-7.
 (4) With PowerPAD soldered on PCB with 2-oz trace of copper. See TI application report [SLMA002](http://www.ti.com/lit/zip/SLSMA002) for further information.

DISSIPATION RATINGS

PACKAGE	POWER RATING T _A = 25°C	DERATING FACTOR ABOVE T _A = 25°C	POWER RATING T _A = 85°C	POWER RATING T _A = 125°C
28-pin HTSSOP with thermal pad soldered ⁽¹⁾	3958 mW	31.67 mW/°C	2058 mW	791 mW
28-pin HTSSOP without thermal pad soldered	2026 mW	16.21 mW/°C	1053 mW	405 mW

- (1) The PowerPAD is soldered to the PCB with a 2-oz. copper trace. See application report [SLMA002](http://www.ti.com/lit/zip/SLSMA002) for further information.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
DC Characteristics				
V_{CC}	Supply voltage	3	5.5	V
V_O	Voltage applied to output (OUT0–OUT15)		17	V
V_{IH}	High-level input voltage	$0.8 V_{CC}$	V_{CC}	V
V_{IL}	Low-level input voltage	GND	$0.2 V_{CC}$	V
I_{OH}	High-level output current	$V_{CC} = 5\text{ V at SOUT}$	–1	mA
I_{OL}	Low-level output current	$V_{CC} = 5\text{ V at SOUT, XERR}$	1	mA
I_{OLC}	Constant output current	OUT0 to OUT15	60	mA
T_J	Operating junction temperature	–40	125	°C
AC Characteristics				
$f_{(SCLK)}$	Data shift clock frequency	SCLK	30	MHz
$f_{(GSCLK)}$	Grayscale clock frequency	GSCLK	30	MHz
t_{wh0}/t_{wl0}	SCLK pulse duration	SCLK = H/L (see Figure 12)	16	ns
t_{wh1}/t_{wl1}	GSCLK pulse duration	GSCLK = H/L (see Figure 12)	16	ns
t_{wh2}	XLAT pulse duration	XLAT = H (see Figure 12)	20	ns
t_{wh3}	BLANK pulse duration	BLANK = H (see Figure 12)	20	ns
t_{su0}	Setup time	SIN to SCLK↑ (see Figure 12)	5	ns
t_{su1}	Setup time	SCLK↓ to XLAT↑ (see Figure 12)	10	ns
t_{su2}	Setup time	MODE↑↓ to SCLK↑ (see Figure 12)	10	ns
t_{su3}	Setup time	MODE↑↓ to XLAT↑ (see Figure 12)	10	ns
t_{su4}	Setup time	BLANK↓ to GSCLK↑ (see Figure 12)	10	ns
t_{su5}	Setup time	XLAT↑ to GSCLK↑ (see Figure 12)	30	ns
t_{h0}	Hold time	SCLK↑ to SIN (see Figure 12)	3	ns
t_{h1}	Hold time	XLAT↓ to SCLK↑ (see Figure 12)	10	ns
t_{h2}	Hold time	SCLK↑ to MODE↑↓ (see Figure 12)	10	ns
t_{h3}	Hold time	XLAT↓ to MODE↑↓ (see Figure 12)	10	ns
t_{h4}	Hold time	GSCLK↑ to BLANK↑ (see Figure 12)	10	ns

ELECTRICAL CHARACTERISTICS

$V_{CC} = 3\text{ V to }5.5\text{ V}$, $T_J = -40^\circ\text{C to }125^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1\text{ mA}$, SOUT	$V_{CC} - 0.5$			V
V_{OL}	Low-level output voltage	$I_{OL} = 1\text{ mA}$, SOUT	0.5			V
I_i	Input current	$V_i = V_{CC}$ or GND, BLANK, TEST, GSCLK, SCLK, SIN, XLAT	-1			μA
		$V_i = \text{GND}$, MODE pin	-1			
		$V_i = V_{CC}$, MODE pin	50			
I_{CC}	Supply current	No data transfer, all output OFF, $V_O = 1\text{ V}$, $R_{(IREF)} = 10\text{ k}\Omega$	0.9		6	mA
		No data transfer, all output OFF, $V_O = 1\text{ V}$, $R_{(IREF)} = 1.3\text{ k}\Omega$	5.2		12	
		Data transfer 30 MHz, all output ON, $V_O = 1\text{ V}$, $R_{(IREF)} = 1.3\text{ k}\Omega$	16		25	
		Data transfer 30 MHz, all output ON, $V_O = 1\text{ V}$, $R_{(IREF)} = 640\ \Omega$	30		60	
$I_{O(LC)}$	Constant output current	All output ON, $V_O = 1\text{ V}$, $R_{(IREF)} = 640\ \Omega$	54	61	69	mA
I_{ikg}	Leakage output current	All output OFF, $V_O = 15\text{ V}$, $R_{(IREF)} = 640\ \Omega$, OUT0 to OUT15	0.1			μA
$\Delta I_{O(LC0)}$	Constant sink current error	All output ON, $V_O = 1\text{ V}$, $R_{(IREF)} = 640\ \Omega$, OUT0 to OUT15, $T_A = -20^\circ\text{C to }85^\circ\text{C}^{(1)}$	± 1		± 4	%
		All output ON, $V_O = 1\text{ V}$, $R_{(IREF)} = 640\ \Omega$, OUT0 to OUT15 ⁽¹⁾	± 1		± 8	
$\Delta I_{O(LC1)}$	Constant sink current error	Device to device, averaged current from OUT0 to OUT15, $R_{(IREF)} = 1920\ \Omega$ (20 mA) ⁽²⁾	-2, 0.4		± 4	%
$\Delta I_{O(LC2)}$	Line regulation	All output ON, $V_O = 1\text{ V}$, $R_{(IREF)} = 640\ \Omega$, OUT0 to OUT15, $V_{CC} = 3\text{ V to }5.5\text{ V}^{(3)}$	± 1		± 4	%/V
$\Delta I_{O(LC3)}$	Load regulation	All output ON, $V_O = 1\text{ V to }3\text{ V}$, $R_{(IREF)} = 640\ \Omega$, OUT0 to OUT15 ⁽⁴⁾	± 2		± 6	%/V
$T_{(TEF)}$	Thermal error flag threshold	Junction temperature ⁽⁵⁾	150		170	$^\circ\text{C}$
$V_{(LED)}$	LED open detection threshold		0.3		0.4	V
$V_{(IREF)}$	Reference voltage output	$R_{(IREF)} = 640\ \Omega$	1.20	1.25	1.29	V

- (1) The deviation of each output from the average of OUT0-15 constant current. It is calculated by [Equation 1](#) in [Table 1](#).
- (2) The deviation of average of OUT1-OUT15 constant current from the ideal constant-current value. It is calculated by [Equation 2](#) in [Table 1](#). The ideal current is calculated by [Equation 3](#) in [Table 1](#).
- (3) The line regulation is calculated by [Equation 4](#) in [Table 1](#).
- (4) The load regulation is calculated by [Equation 5](#) in [Table 1](#).
- (5) Not tested. Specified by design.

Table 1. Test Parameter Equations

$\Delta(\%) = \frac{I_{OUTn} - I_{OUTavg_0-15}}{I_{OUTavg_0-15}} \times 100$	(1)
$\Delta(\%) = \frac{I_{OUTavg} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}} \times 100$	(2)
$I_{OUT(IDEAL)} = 31.5 \times \left(\frac{1.24V}{R_{IREF}} \right)$	(3)
$\Delta(\%/V) = \frac{(I_{OUTn} \text{ at } V_{CC} = 5.5V) - (I_{OUTn} \text{ at } V_{CC} = 3.0V)}{(I_{OUTn} \text{ at } V_{CC} = 3.0V)} \times \frac{100}{2.5}$	(4)
$\Delta(\%/V) = \frac{(I_{OUTn} \text{ at } V_{OUTn} = 3.0V) - (I_{OUTn} \text{ at } V_{OUTn} = 1.0V)}{(I_{OUTn} \text{ at } V_{OUTn} = 1.0V)} \times \frac{100}{2.0}$	(5)

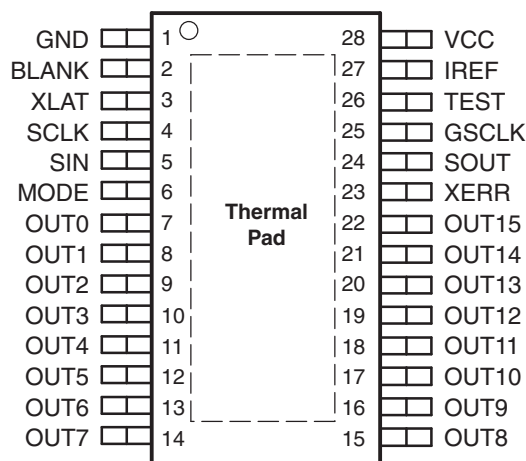
SWITCHING CHARACTERISTICS

V_{CC} = 3 V to 5.5 V, C_L = 15 pF, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t _{r0}	Rise time			16	ns	
t _{r1}	Rise time		10	30	ns	
t _{f0}	Fall time			16	ns	
t _{f1}	Fall time		10	30	ns	
t _{pd0}	Propagation delay time			30	ns	
t _{pd1}	Propagation delay time			60	ns	
t _{pd2}	Propagation delay time			1000	ns	
t _{pd3}	Propagation delay time			60	ns	
t _{pd4}	Propagation delay time			1000	ns	
t _d	Output delay time		20	30	ns	
t _{on_err}	Output on-time error	t _{outon} – t _{gsclk} (see Figure 12), GS _n = 01h, GSCLK = 11 MHz	10	–50	–90	ns

DEVICE INFORMATION

**PWP PACKAGE
(TOP VIEW)**



TERMINAL FUNCTION

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BLANK	2	I	Blank all outputs. When BLANK = H, all OUTn outputs are forced OFF. GS counter is also reset. When BLANK = L, OUTn are controlled by grayscale PWM control.
GND	1	G	Ground
GSCLK	25	I	Reference clock for grayscale PWM control
IREF	27	I/O	Reference current terminal
MODE	6	I	Input mode-change pin. When MODE = GND, the device is in GS mode. When MODE = VCC, the device is in DC mode.
OUT0	7	O	Constant-current output
OUT1	8	O	Constant-current output
OUT2	9	O	Constant-current output
OUT3	10	O	Constant-current output
OUT4	11	O	Constant-current output
OUT5	12	O	Constant-current output
OUT6	13	O	Constant-current output
OUT7	14	O	Constant-current output
OUT8	15	O	Constant-current output
OUT9	16	O	Constant-current output
OUT10	17	O	Constant-current output
OUT11	18	O	Constant-current output
OUT12	19	O	Constant-current output
OUT13	20	O	Constant-current output
OUT14	21	O	Constant-current output
OUT15	22	O	Constant-current output
SCLK	4	I	Serial data shift clock
SIN	5	I	Serial data input
SOUT	24	O	Serial data output
TEST	26	I	Test. Must be connected to VCC.
VCC	28	I	Power supply voltage
XERR	23	O	Error output. Open-drain. Goes L when LOD or TEF is detected.
XLAT	3	I	Level triggered latch signal. When XLAT = high, the TLC5941 writes data from the input shift register to either GS register (MODE = low) or DC register (MODE = high). When XLAT = low, the data in the GS or DC registers is held constant and does not change.

PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

Resistor values are equivalent resistance and not tested.

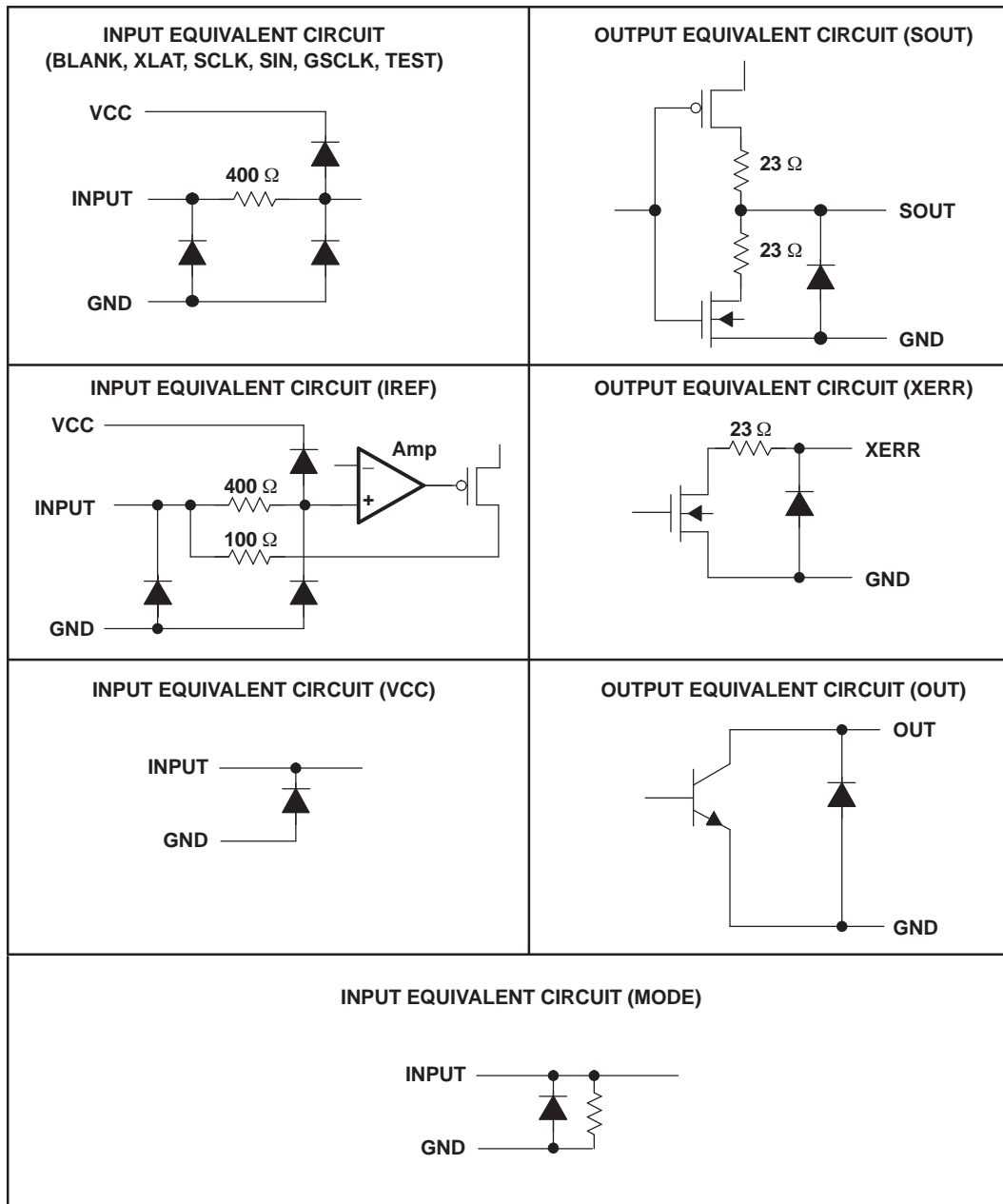


Figure 1. Input and Output Equivalent Circuits

PARAMETER MEASUREMENT INFORMATION (continued)

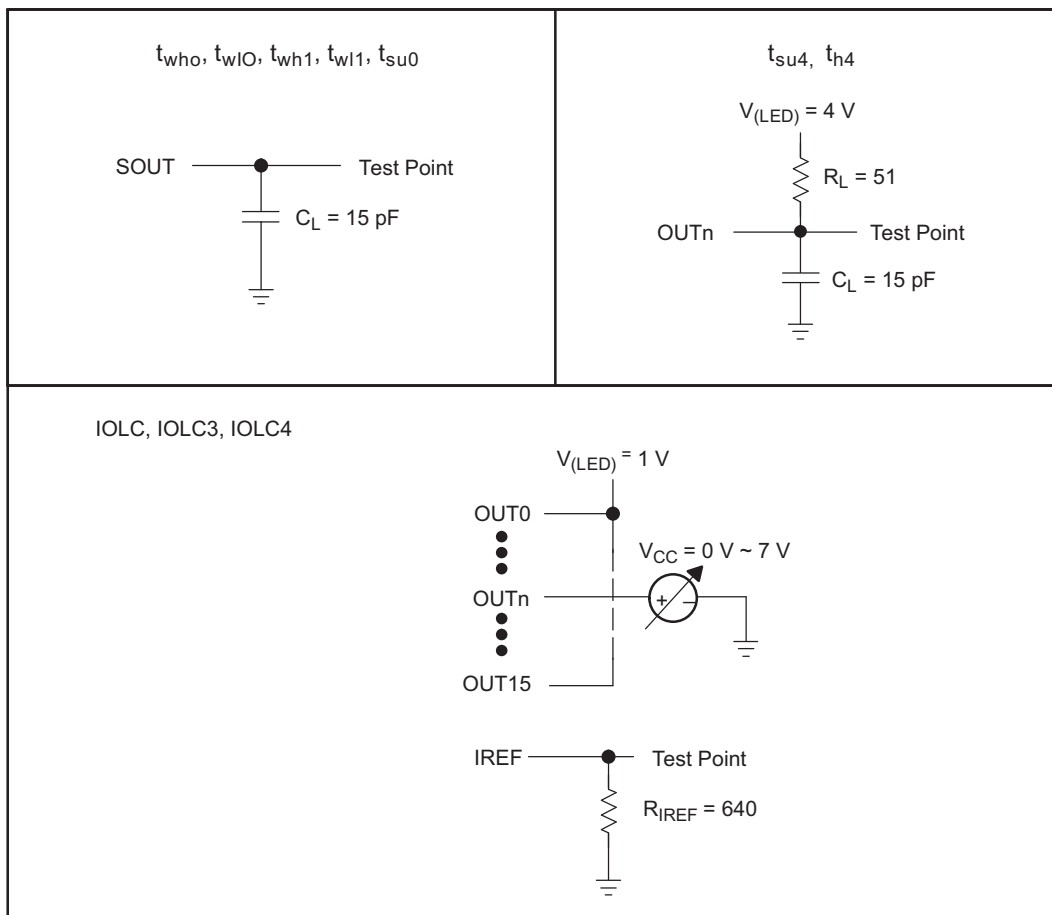


Figure 2. Parameter Measurement Circuits

Typical Characteristics

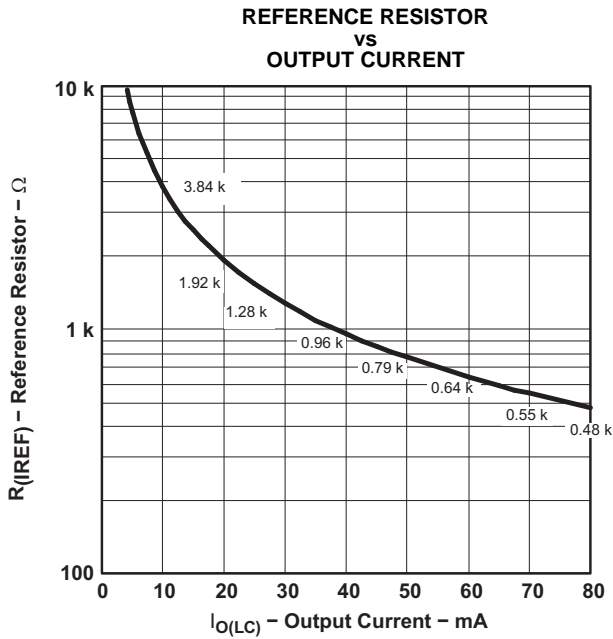


Figure 3.

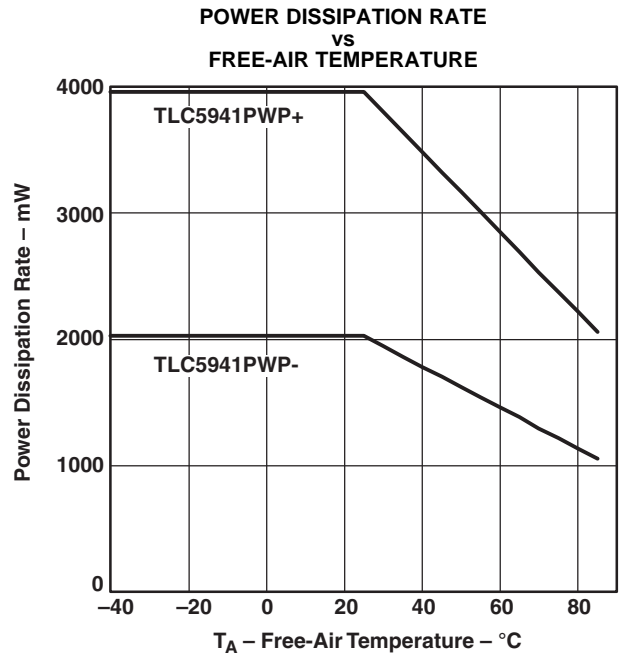


Figure 4.

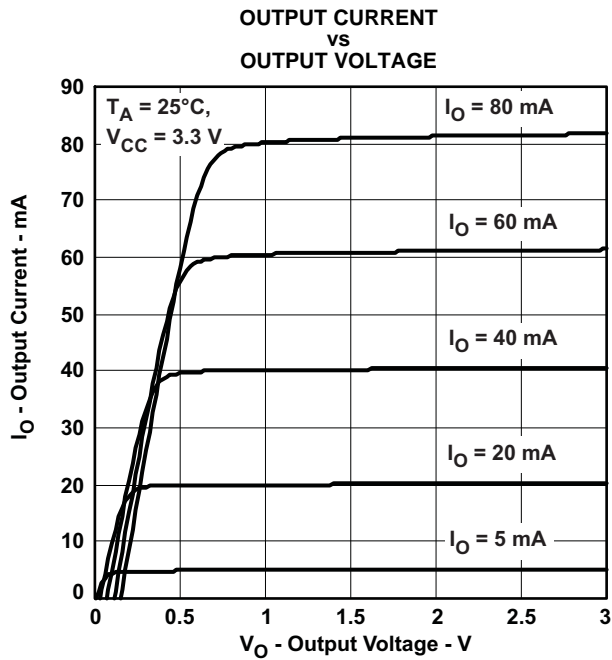


Figure 5.

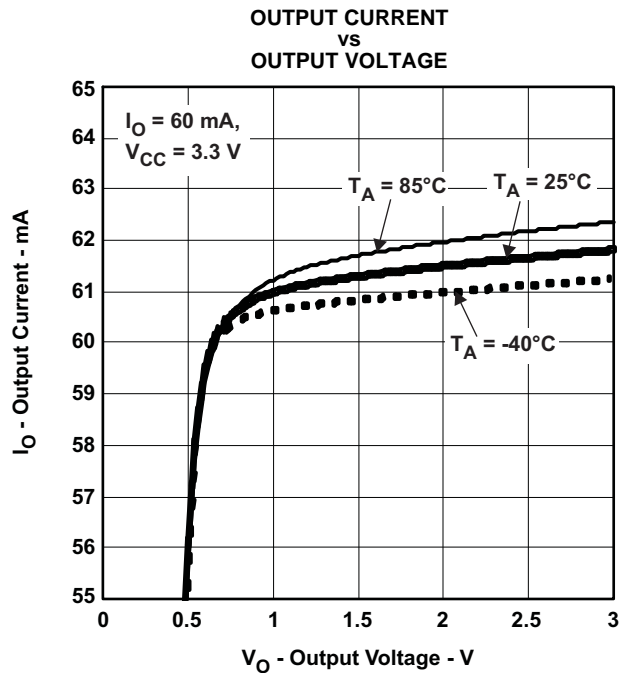


Figure 6.

Typical Characteristics (continued)

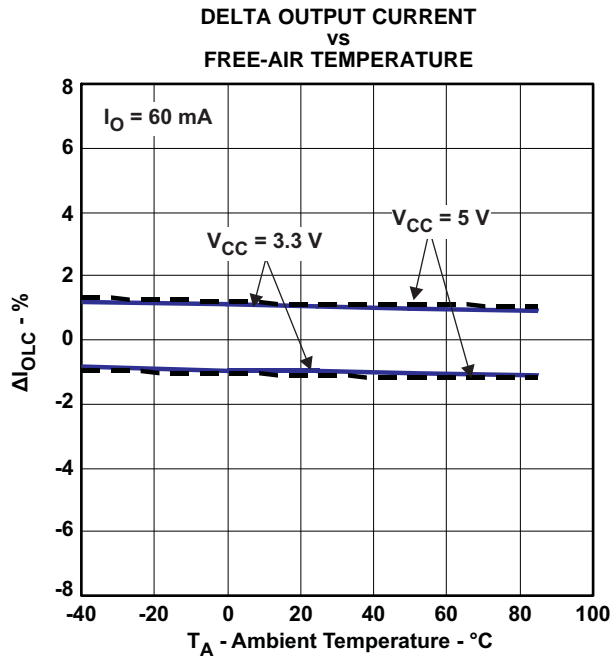


Figure 7.

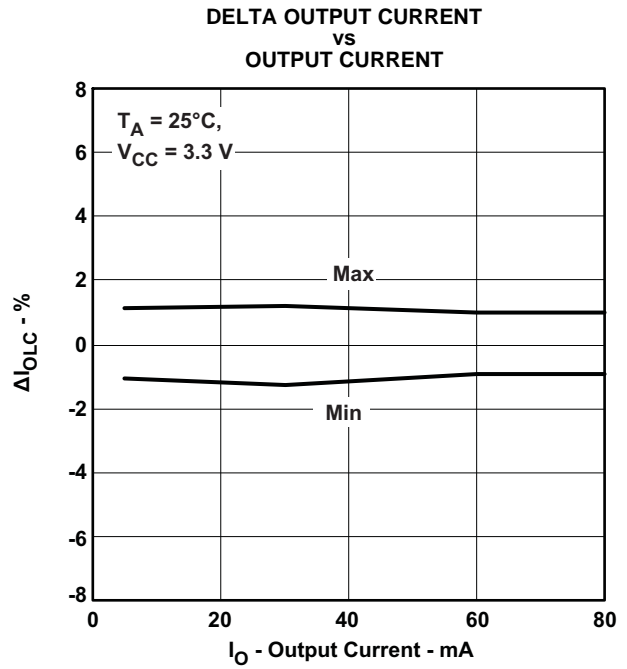


Figure 8.

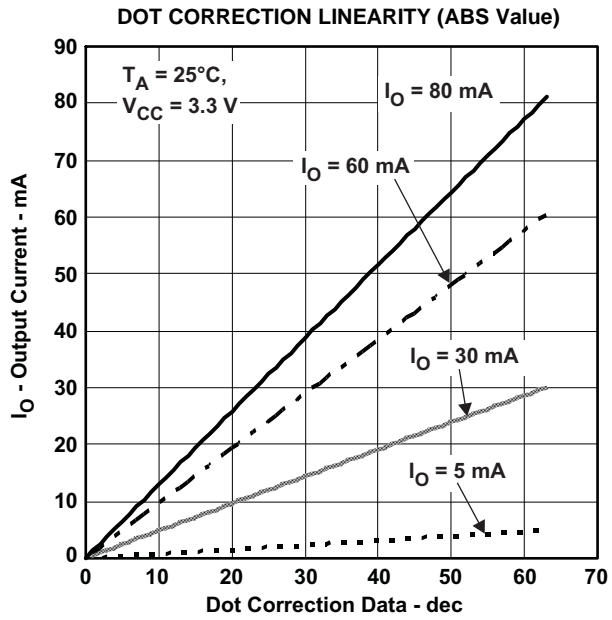


Figure 9.

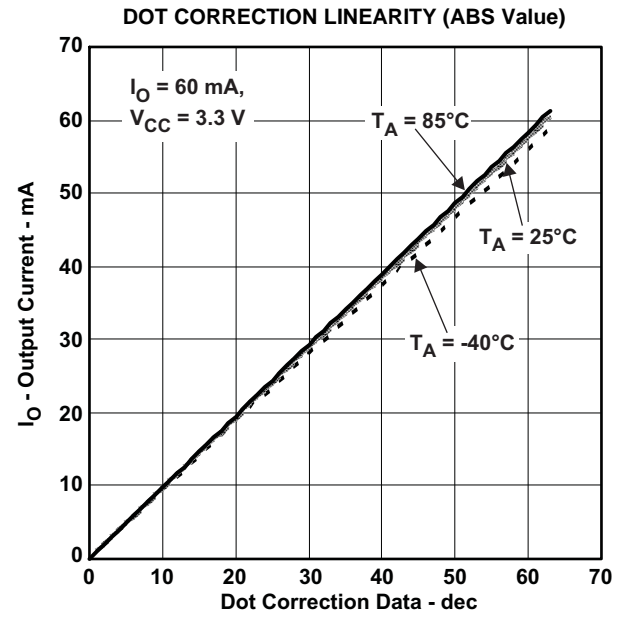


Figure 10.

Typical Characteristics (continued)

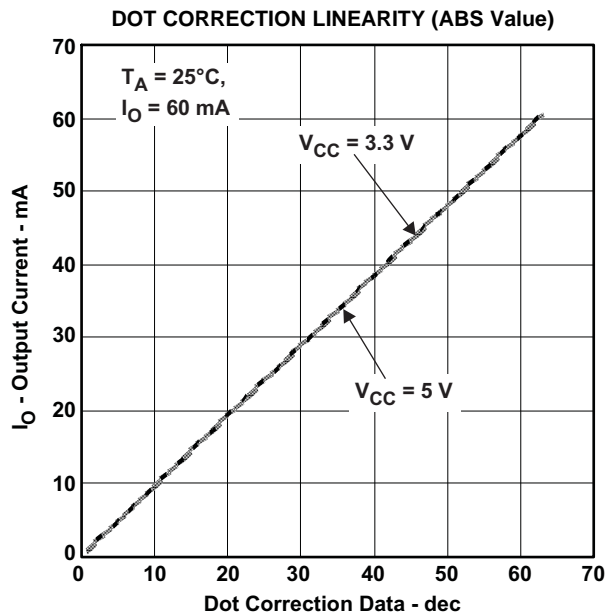


Figure 11.

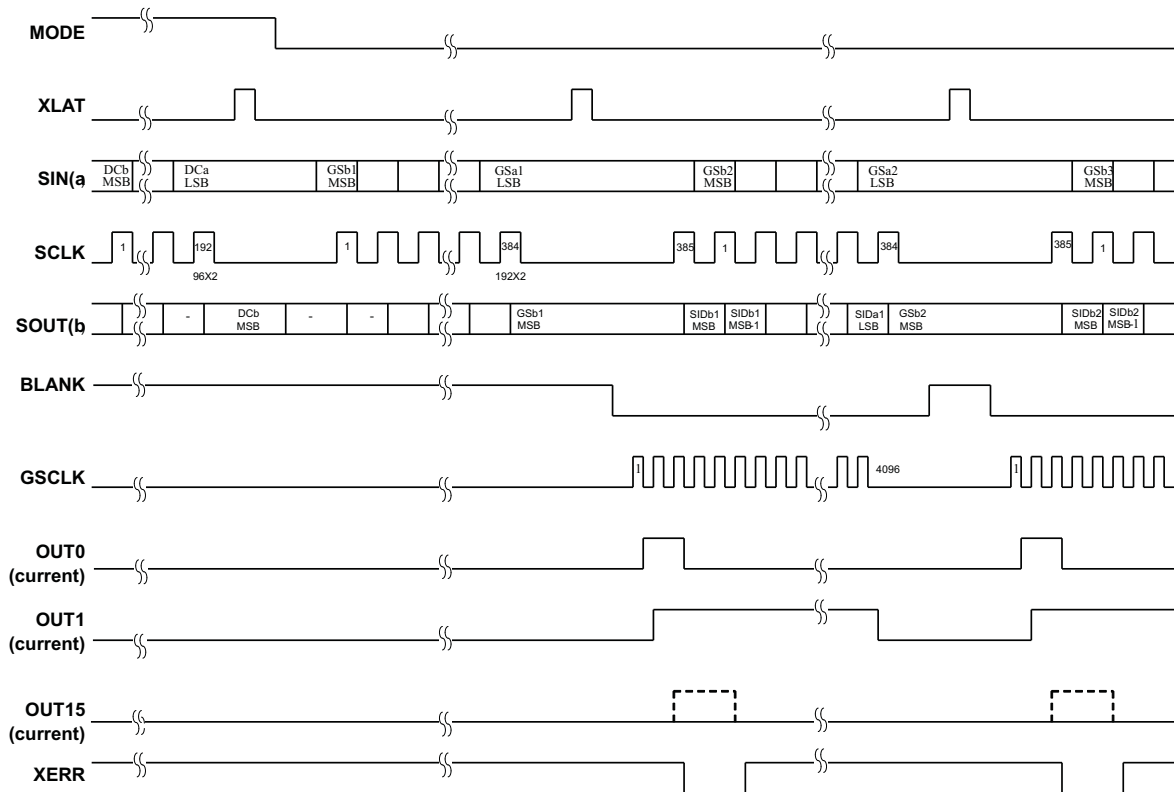


Figure 14. Timing Chart for Two Cascaded TLC5941 Devices

ERROR INFORMATION OUTPUT

The open-drain output XERR is used to report both of the TLC5941 error flags, TEF and LOD. During normal operating conditions, the internal transistor connected to the XERR pin is turned off. The voltage on XERR is pulled up to V_{CC} through an external pullup resistor. If TEF or LOD is detected, the internal transistor is turned on, and XERR is pulled to GND. Because XERR is an open-drain output, multiple ICs can be ORed together and pulled up to V_{CC} with a single pullup resistor. This reduces the number of signals needed to report a system error (see Figure 22).

To differentiate LOD and TEF signal from XERR pin, LOD can be masked out with BLANK = HIGH.

Table 2. XERR Truth Table

ERROR CONDITION		ERROR INFORMATION		SIGNALS	
TEMPERATURE	OUTn VOLTAGE	TEF	LOD	BLANK	XERR
$T_J < T_{(TEF)}$	Don't Care	L	X	H	H
$T_J > T_{(TEF)}$	Don't Care	H	X		L
$T_J < T_{(TEF)}$	$OUTn > V_{(LED)}$	L	L	L	H
	$OUTn < V_{(LED)}$	L	H		L
$T_J > T_{(TEF)}$	$OUTn > V_{(LED)}$	H	L		L
	$OUTn < V_{(LED)}$	H	H		L

TEF: THERMAL ERROR FLAG

The TLC5941 provides a temperature error flag (TEF) circuit to indicate an overtemperature condition of the IC. If the junction temperature exceeds the threshold temperature (160 = C typical), TEF becomes H and XERR pin goes to low level. When the junction temperature becomes lower than the threshold temperature, TEF becomes L and XERR pin becomes high impedance. TEF status can also be read out from the TLC5941 status register.

LOD: LED OPEN DETECTION

The TLC5941 has an LED-open detection circuit that detects broken or disconnected LED's. The LED open detector pulls the XERR pin to GND when an open LED is detected. XERR and the corresponding error bit in the Status Information Data is only active under the following open LED conditions.

1. OUTn is on and the time tpd2 (1 μ s typical) has passed.
2. The voltage of OUTn is < 0.3V (typical)

The LOD status of each output can be also read out from the SOUT pin. See the [STATUS INFORMATION OUTPUT](#) section for details. The LOD error bits are latched into the Status Information Data when XLAT returns to a low after a high. Therefore, the XLAT pin must be pulsed high then low while XERR is active in order to latch the LOD error into the Status Information Data for subsequent reading via the serial shift register.

DELAY BETWEEN OUTPUTS

The TLC5941 has graduated delay circuits between outputs. These circuits can be found in the constant current driver block of the device (see the functional block diagram). The fixed-delay time is 20ns (typical), OUT0 has no delay, OUT1 has 20ns delay, and OUT2 has 40-ns delay, etc. The maximum delay is 300 ns from OUT0 to OUT15. The delay works during switch on and switch off of each output channel. These delays prevent large inrush currents which reduces the bypass capacitors when the outputs turn on.

OUTPUT ENABLE

All OUTn channels of the TLC5941 can be switched off with one signal. When BLANK is set high, all OUTn channels are disabled, regardless of logic operations of the device. The grayscale counter is also reset. When BLANK is set low, all OUTn channels work under normal conditions. If BLANK goes low and then back high again in less than 300 ns, all outputs programmed to turn on still turn on for either the programmed number of grayscale clocks, or the length of time that the BLANK signal was low, which ever is lower. For example, if all outputs are programmed to turn on for 1 ms, but the BLANK signal is only low for 200 ns, all outputs still turn on for 200 ns, even though some outputs are turning on after the BLANK signal has already gone high.

Table 3. BLANK Signal Truth Table

BLANK	OUT0 to OUT15
LOW	Normal condition
HIGH	Disabled

SETTING MAXIMUM CHANNEL CURRENT

The maximum output current per channel is programmed by a single resistor, $R_{(IREF)}$, which is placed between IREF pin and GND pin. The voltage on IREF is set by an internal band gap $V_{(IREF)}$ with a typical value of 1.24 V. The maximum channel current is equivalent to the current flowing through $R_{(IREF)}$ multiplied by a factor of 31.5. The maximum output current can be calculated by [Equation 6](#):

$$I_{\max} = \frac{V_{(IREF)}}{R_{(IREF)}} \times 31.5 \quad (6)$$

where:

$$V_{(IREF)} = 1.24 \text{ V}$$

$R_{(IREF)}$ = User-selected external resistor.

I_{\max} must be set between 5 mA and 60 mA. The output current may be unstable if I_{\max} is set lower than 5 mA. Output currents lower than 5 mA can be achieved by setting I_{\max} to 5 mA or higher and then using dot correction.

[Figure 3](#) shows the maximum output current I_O versus $R_{(IREF)}$. $R_{(IREF)}$ is the value of the resistor between IREF terminal to GND, and I_O is the constant output current of OUT0 to OUT15. A variable power supply may be connected to the IREF pin through a resistor to change the maximum output current per channel. The maximum output current per channel is 31.5 times the current flowing out of the IREF pin.

POWER DISSIPATION CALCULATION

The device power dissipation needs to be below the power dissipation rate of the device package to ensure correct operation. [Equation 7](#) calculates the power dissipation of device:

$$P_D = (V_{CC} \times I_{CC}) + \left(V_{OUT} \times I_{MAX} \times N \times \frac{DC_n}{63} \times d_{PWM} \right) \quad (7)$$

where:

V_{CC} : device supply voltage

I_{CC} : device supply current

V_{OUT} : TLC5941 OUTn voltage when driving LED current

I_{MAX} : LED current adjusted by $R_{(IREF)}$ Resistor

DC_n : maximum dot correction value for OUTn

N: number of OUTn driving LED at the same time

d_{PWM} : duty cycle defined by BLANK pin or GS PWM value

OPERATING MODES

The TLC5941 has two operating modes defined by MODE as shown in [Table 4](#). The GS and DC registers are set to random values that are not known just after power on. The GS and DC values must be programmed before turning on the outputs. Please note that when initially setting GS and DC data after power on, the GS data must be set before the DC data is set. Failure to set GS data before DC data may result in the first bit of GS data being lost. XLAT must be low when the MODE pin goes high-to-low or low-to-high to change back and forth between GS mode and DC mode.

Table 4. TLC5941 Operating Modes Truth Table

MODE	INPUT SHIFT REGISTER	OPERATING MODE
GND	192 bit	Grayscale PWM Mode
V_{CC}	96 bit	Dot Correction Data Input Mode

SETTING DOT CORRECTION

The TLC5941 has the capability to fine-adjust the output current of each channel (OUT0 to OUT15) independently. This is also called dot correction. This feature is used to adjust the brightness deviations of LEDs connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 6-bit word. The channel output can be adjusted in 64 steps from 0% to 100% of the maximum output current I_{max} . The TEST pin must be connected to VCC to ensure proper operation of the dot correction circuitry. Equation 8 determines the output current for each output n:

$$I_{OUTn} = I_{max} \times \frac{DCn}{63} \tag{8}$$

where:

I_{max} = the maximum programmable output current for each output.

DCn = the programmed dot correction value for output n (DCn = 0 to 63).

n = 0 to 15

Figure 15 shows the dot correction data packet format which consists of 6 bits x 16 channel, total 96 bits. The format is Big-Endian format. This means that the MSB is transmitted first, followed by the MSB-1, etc. The DC 15.5 in Figure 15 stands for the 5th-most significant bit for output 15.

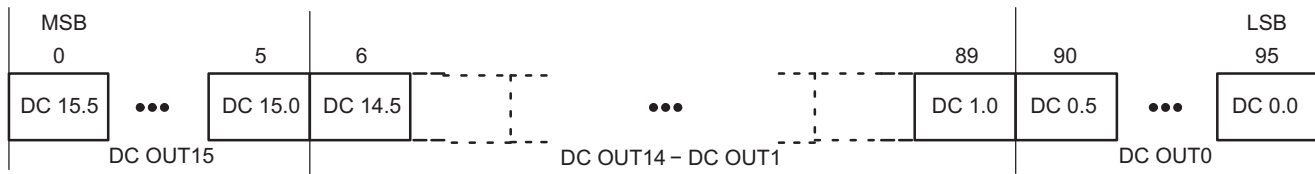


Figure 15. Dot Correction Data Packet Format

When MODE is set to VCC, the TLC5941 enters the dot correction data input mode. The length of input shift register becomes 96bits. After all serial data are shifted in, the TLC5941 writes the data in the input shift register to DC register when XLAT is high, and holds the data in the DC register when XLAT is low. The DC register is a level triggered latch of XLAT signal. Since XLAT is a level-triggered signal, SCLK and SIN must not be changed while XLAT is high. After XLAT goes low, data in the DC register is latched and does not change. BLANK signal does not need to be high to latch in new data. When XLAT goes high, the new dot-correction data immediately becomes valid and changes the output currents if BLANK is low. XLAT has setup time (tsu1) and hold time (th1) to SCLK as shown in Figure 12.

To input data into the dot correction register, MODE must be set to V_{CC} . The internal input shift register is then set to 96-bit width. After all serial data are clocked in, a rising edge of XLAT is used to latch the data into the dot correction register. Figure 16 shows the dc data input timing chart.

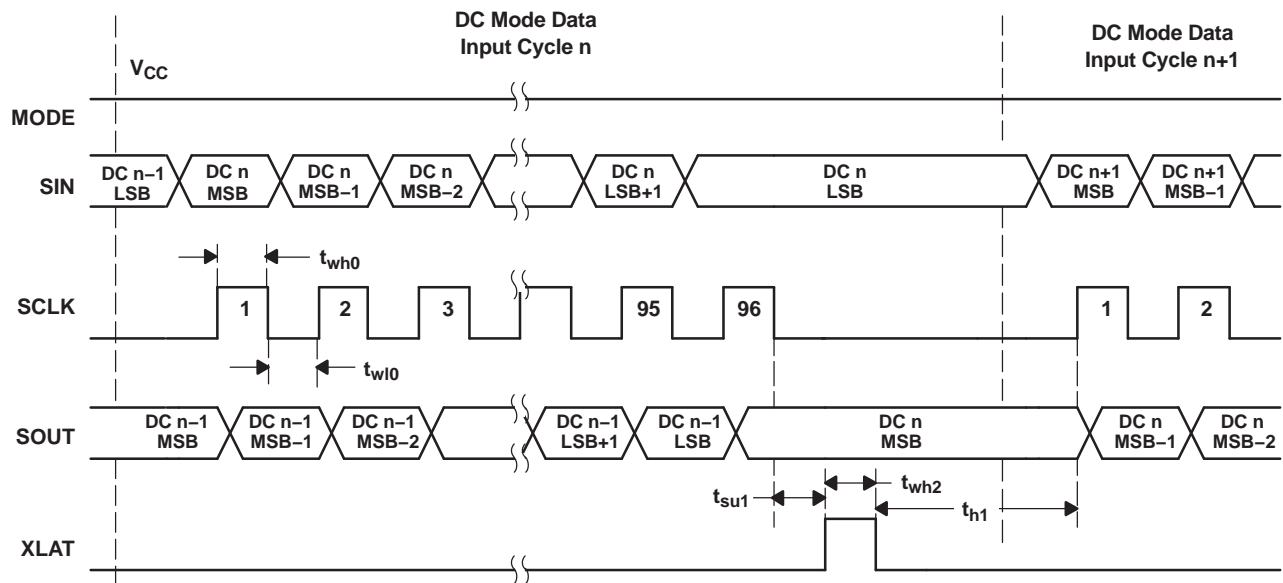


Figure 16. Dot Correction Data Input Timing Chart

SETTING GRAYSCALE

The TLC5941 can adjust the brightness of each channel OUTn using a PWM control scheme. The use of 12 bits per channel results in 4096 different brightness steps, from 0% to 100% brightness. Equation 9 determines the brightness level for each output n:

$$\text{Brightness in \%} = \frac{\text{GS}_n}{4095} \times 100 \tag{9}$$

where:

GSn = the programmed grayscale value for output n (GSn = 0 to 4095)

n = 0 to 15

Grayscale data for all OUTn

The input shift register enters grayscale data into the grayscale register for all channels simultaneously. The complete grayscale data format consists of 16 x 12 bit words, which forms a 192-bit wide data packet (see Figure 17). The data packet must be clocked in with the MSB first.



Figure 17. Grayscale Data Packet Format

When MODE is set to GND, the TLC5941 enters the grayscale data input mode. The device switches the input shift register to 192-bit width. After all data is clocked in, a rising edge of the XLAT signal latches the data into the grayscale register (see Figure 18). New grayscale data immediately becomes valid at the rising edge of the XLAT signal; therefore, new grayscale data should be latched at the end of a grayscale cycle when BLANK is high. The first GS data input cycle after dot correction requires an additional SCLK pulse after the XLAT signal to complete the grayscale update cycle. All GS data in the input shift register is replaced with status information data (SID) after updating the grayscale register.

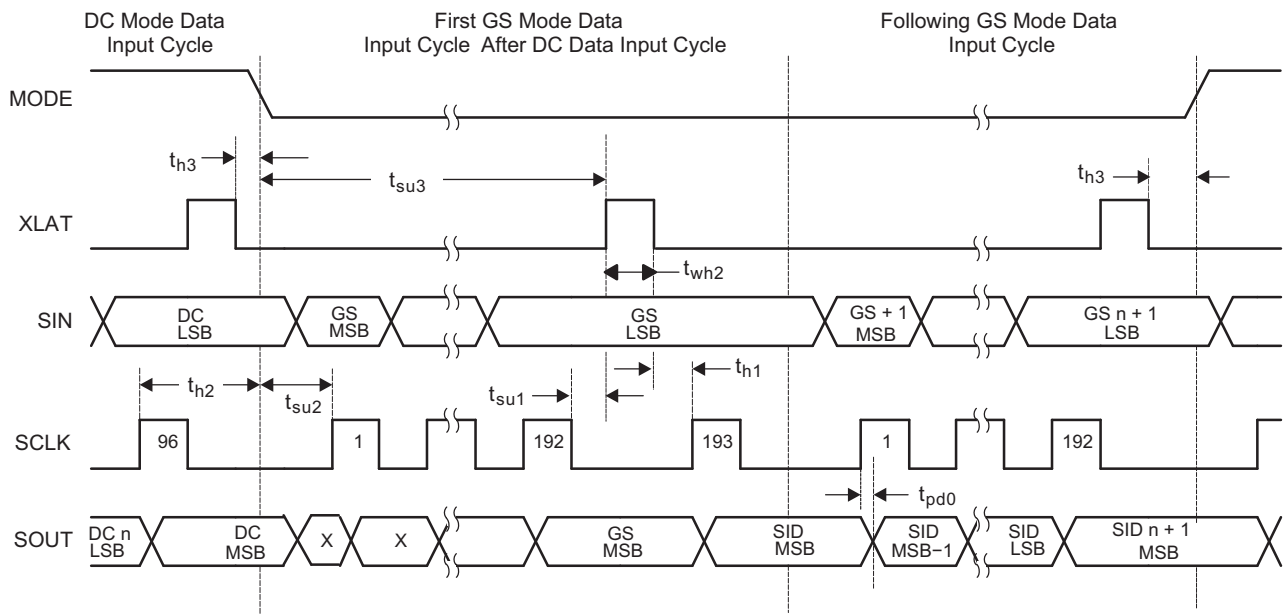


Figure 18. Grayscale Data Input Timing Chart

STATUS INFORMATION OUTPUT

The TLC5941 does have a status information register, which can be accessed in grayscale mode (MODE = GND). After the XLAT signal latches the data into the GS register, the input shift register data is replaced with status information data (SID) of the device (see [Figure 18](#)). LOD, TEF, and dot-correction register data can be read out at the SOUT pin. The status information data packet is 192 bits wide. Bits 0 – 15 contain the LOD status of each channel. Bit 16 contains the TEF status. Bits 24 – 119 contain the data of the dot-correction register. The remaining bits are reserved. The complete status information data packet is shown in [Figure 19](#).

SOUT outputs the MSB of the SID at the same time the SID are stored in the SID register, as shown in [Figure 20](#). The next SCLK pulse, which will be the clock for receiving the MSB of the next grayscale data, transmits MSB-1 of SID. If output voltage is < 0.3 V (typical) when the output sink current turns on, LOD status flag becomes active. The LOD status flag is an internal signal which pulls XERR pin down to low when the LOD status flag becomes active. The delay time, tpd2 (1 μs maximum), is from the time of turning on the output sink current to the time LOD status flag becomes valid. The timing for each channels LOD status to become valid is shifted by the 30-ns (maximum), channel-to-channel turn-on time. After the first GSCLK goes high, OUT0 LOD status is valid; tpd3 + tpd2 = 60 nS + 1 μs = 1.06 μs. OUT1 LOD status is valid; tpd3 + td + tpd2 = 60 ns + 30 ns + 1 μs = 1.09 μs. OUT2 LOD status is valid; tpd3 + 2*td + tpd2 = 1.12 μs, and so on. It takes 1.51μs maximum (tpd3 + 15*td + tpd2) from the first GSCLK rising edge until all LOD become valid; *tsuLOD* must be > 1.51 μs (see [Figure 20](#)) to ensure that all LOD data are valid.

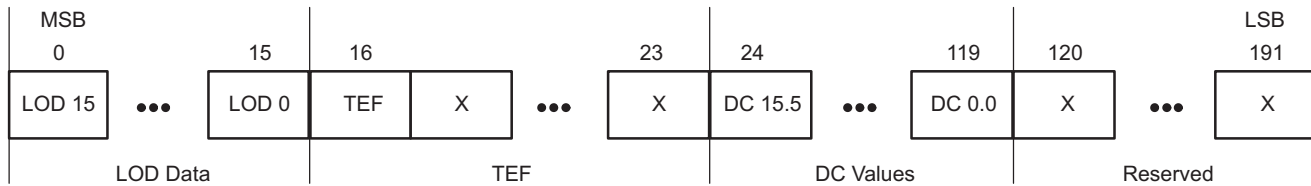


Figure 19. Status Information Data Packet Format

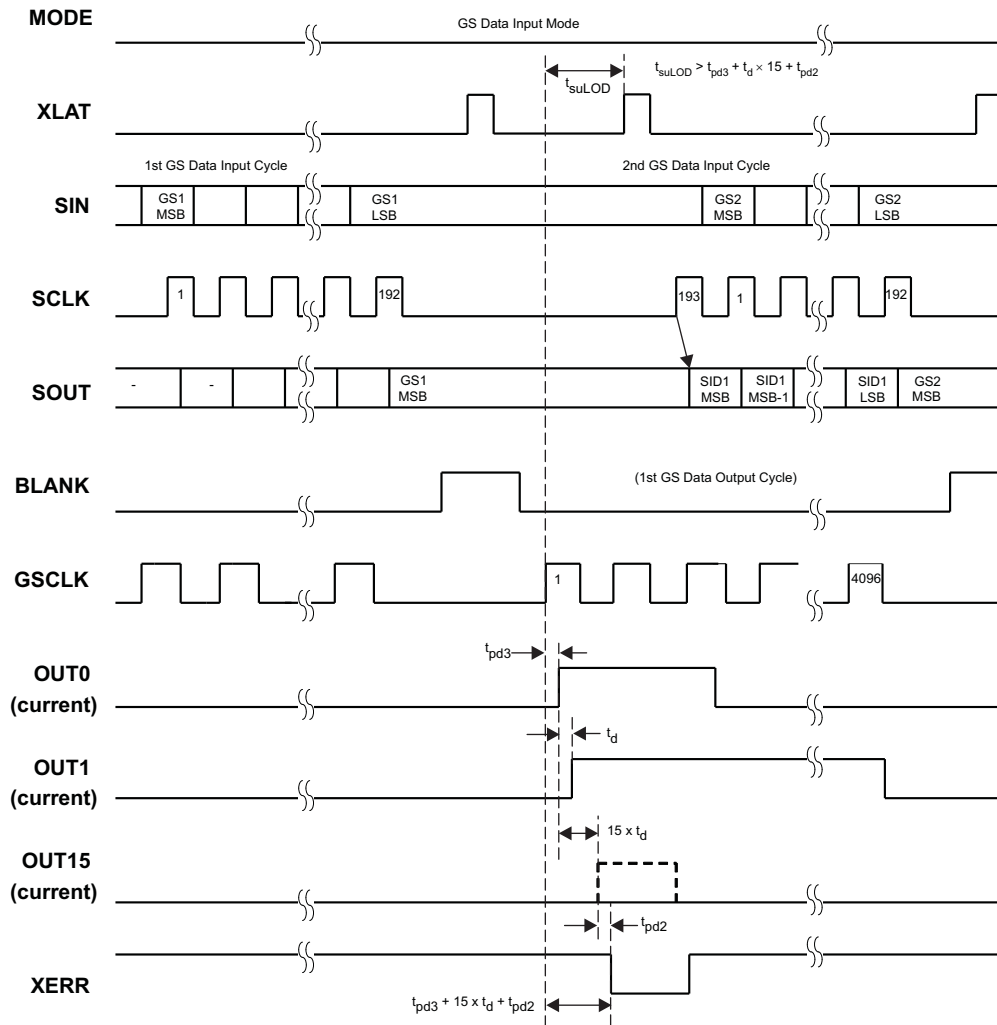


Figure 20. Readout Status Information Data (SID) Timing Chart

The LOD status of each output can be read out from the SOUT pin. The LOD error bits are latched into the Status Information Data when XLAT returns to a low after a high. Therefore, the XLAT pin must be pulsed high then low while XERR is active in order to latch the LOD error into the Status Information Data for subsequent reading via the serial shift register.

GRAYSCALE PWM OPERATION

The grayscale PWM cycle starts with the falling edge of BLANK. The first GSCLK pulse after BLANK goes low increases the grayscale counter by one and switches on all OUTn with grayscale value not zero. Each following rising edge of GSCLK increases the grayscale counter by one. The TLC5941 compares the grayscale value of each output OUTn with the grayscale counter value. All OUTn with grayscale values equal to the counter values are switched off. A BLANK=H signal after 4096 GSCLK pulses resets the grayscale counter to zero and completes the grayscale PWM cycle (see Figure 21). When the counter reaches a count of FFFh, the counter stops counting and all outputs turn off. Pulling BLANK high before the counter reaches FFFh immediately resets the counter to zero.

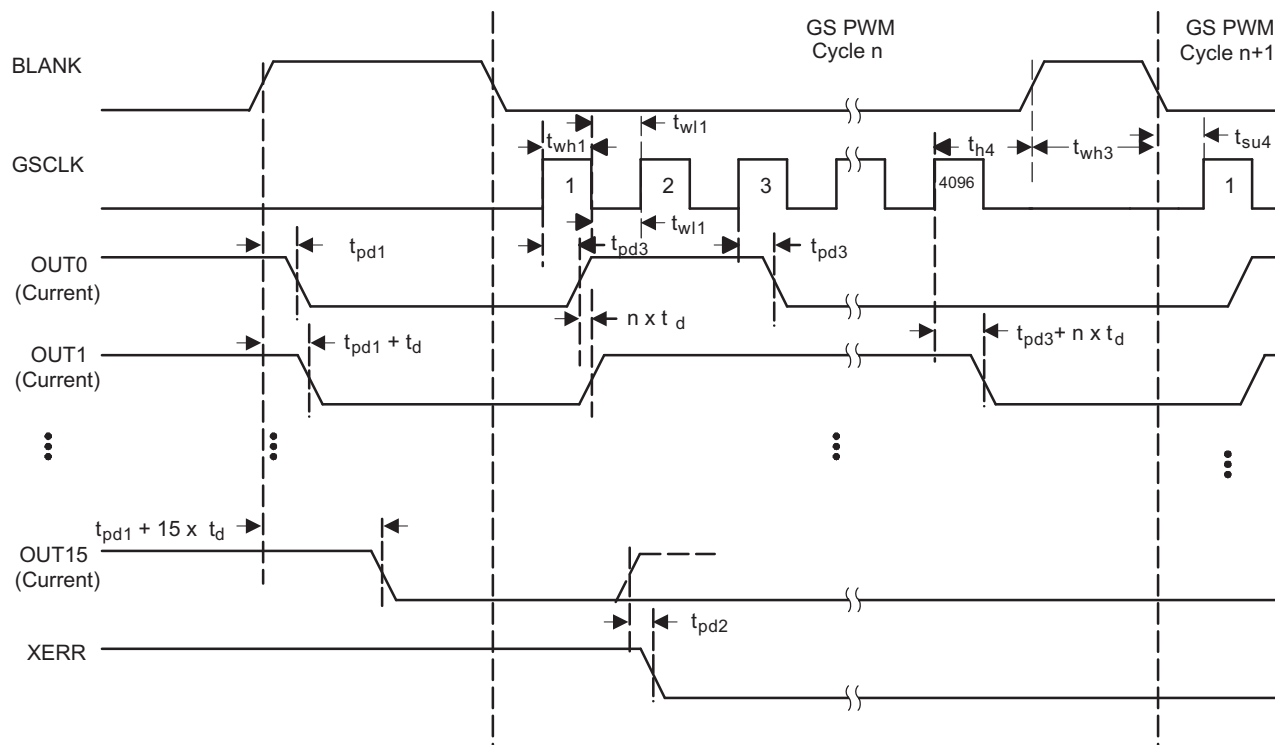


Figure 21. Grayscale PWM Cycle Timing Chart

Output On Time

The amount of time that each output is turned on is a function of the grayscale clock frequency and the programmed grayscale PWM value. The on-time of each output can be calculated using Equation 10.

$$T_{on_n} = \frac{GS_n}{f_{(GSCLK)}} + t_{on_err} \quad (10)$$

Where

- T_{on_n} is the time that OUTn turns on and sinks current
- GS_n is OUTn's programmed grayscale PWM value between 0 and 4095
- t_{on_err} is the Output on time error defined in the Switching Characteristics Table

When using Equation 10 with very high GSCLK frequencies and very low grayscale PWM values, the resulting T_{on} time may be negative. If T_{on} is negative, the output does not turn on. For example, using $f_{(GSCLK)} = 30$ MHz, $GS_n = 1$, and the typical $t_{on_err} = 50$ nS, Equation 10 calculates that OUTn turns on for -16.6 nS. This output may not turn on under these conditions. Increasing the PWM value or reducing the GSCLK clock frequency ensures turn-on.

SERIAL DATA TRANSFER RATE

Figure 22 shows a cascading connection of n TLC5941 devices connected to a controller, building a basic module of an LED display system. There is no TLC5941 limitation to the maximum number of ICs that can be cascaded. The maximum number of cascading TLC5941 devices depends on the application system and is in the range of 40 devices. Equation 11 calculates the minimum frequency needed:

$$f_{(GSCLK)} = 4096 \times f_{(update)}$$

$$f_{(SCLK)} = 193 \times f_{(update)} \times n \tag{11}$$

where:

$f_{(GSCLK)}$: minimum frequency needed for GSCLK

$f_{(SCLK)}$: minimum frequency needed for SCLK and SIN

$f_{(update)}$: update rate of whole cascading system

n : number cascaded of TLC5941 device

Application Example

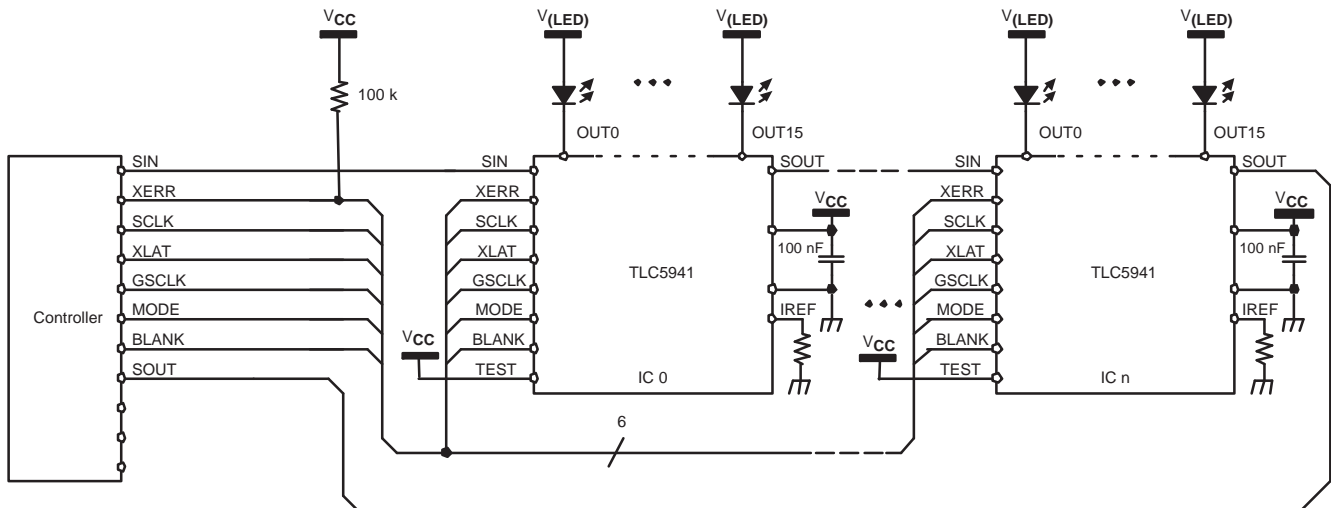


Figure 22. Cascading Devices

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLC5941QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TLC5941-Q1 :

- Catalog: [TLC5941](#)

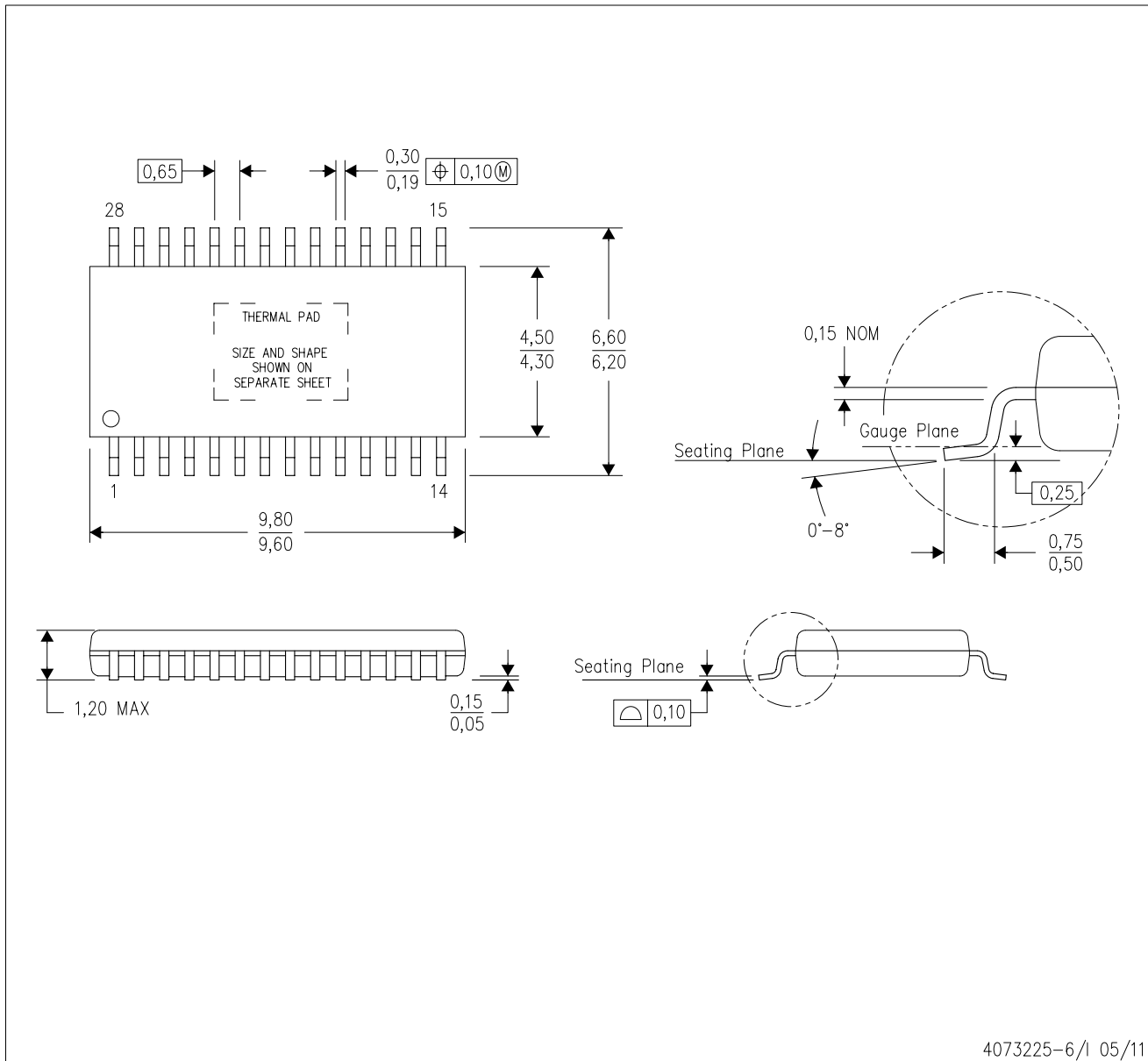
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

MECHANICAL DATA

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

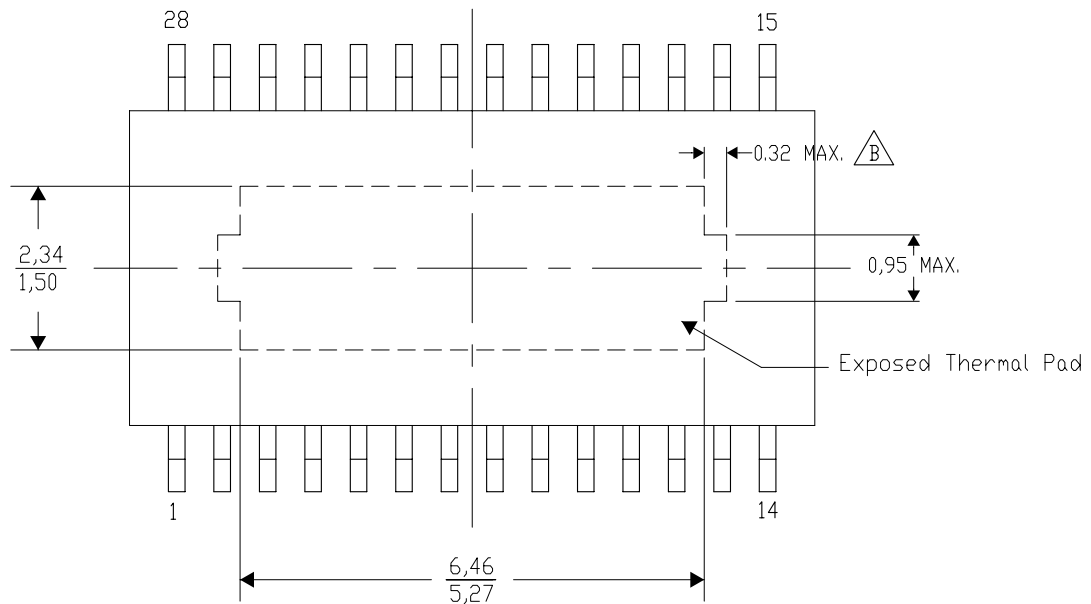
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

4206332-36/Y 10/11

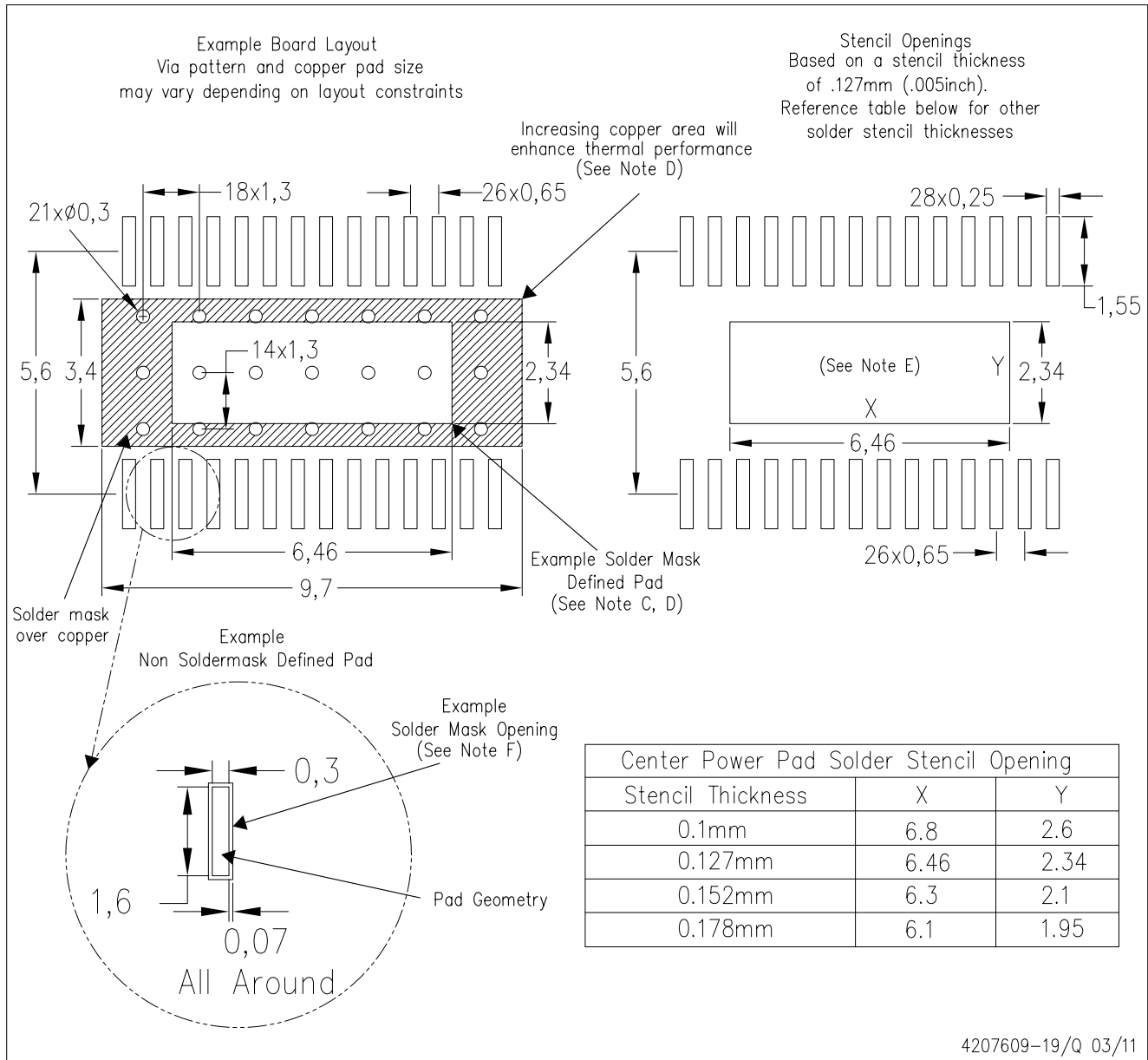
NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



4207609-19/Q 03/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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