Data sheet acquired from Harris Semiconductor SCHS195C

January 1998 - Revised October 2003

High-Speed CMOS Logic 4x4 Register File

Features

- Simultaneous and Independent Read and Write Operations
- Expandable to 512 Words of n-Bits
- Three-State Outputs
- · Organized as 4 Words x 4 Bits Wide
- Buffered Inputs
- Typical Read Time = 16ns for 'HC670 V_{CC} = 5V, C_L = 15pF, T_A = 25 $^{\rm o}$ C
- Fanout (Over Temperature Range)
 - Standard Outputs...... 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range ...-55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility,
 V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, $I_I \le 1\mu A$ at V_{OL} , V_{OH}

Description

The 'HC670 and CD74HCT670 are 16-bit register files organized as 4 words x 4 bits each. Read and write address and enable inputs allow simultaneous writing into one location while reading another. Four data inputs are provided to store the 4-bit word. The write address inputs (WA0 and WA1) determine the location of the stored word in the register. When write enable (\overline{WE}) is low the word is entered into the address location and it remains transparent to the data. The outputs will reflect the true form of the input data. When (\overline{WE}) is high data and address inputs are inhibited. Data acquisition from the four registers is made possible by the read address inputs (RA1 and RA0). The addressed word appears at the output when the read enable (\overline{RE}) is low. The output is in the high impedance state when the (\overline{RE}) is high. Outputs can be tied together to increase the word capacity to 512 x 4 bits.

Ordering Information

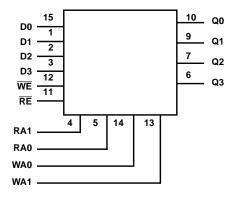
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC670F3A	-55 to 125	16 Ld CERDIP
CD74HC670E	-55 to 125	16 Ld PDIP
CD74HC670M	-55 to 125	16 Ld SOIC
CD74HC670MT	-55 to 125	16 Ld SOIC
CD74HC670M96	-55 to 125	16 Ld SOIC
CD74HCT670E	-55 to 125	16 Ld PDIP
CD74HCT670M	-55 to 125	16 Ld SOIC
CD74HCT670MT	-55 to 125	16 Ld SOIC
CD74HCT670M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

CD54HC670 (CERDIP) CD74HC670, CD74HCT670 (PDIP, SOIC) TOP VIEW 16 V_{CC} D1 1 15 D0 D2 2 D3 3 14 WA0 13 WA1 RA1 4 12 WE RA0 5 11 RE Q3 6 10 Q0 Q2 [7 GND 8 9 Q1

Functional Diagram



WRITE MODE SELECT TABLE

OPERATING	INP	INTERNAL LATCHES	
MODE	WE	D _N	(NOTE 1)
Write Data	L	L	L
	L	Н	Н
Data Latched	Н	Х	No Change

NOTE:

READ MODE SELECT TABLE

	INP	UTS	
OPERATING MODE	RE	INTERNAL LATCHES (NOTE 2)	OUTPUT Q _N
Read	L	L	L
	L	Н	Н
Disabled	Н	Х	(Z)

- 2. The selection of the "internal latches" by Read Address (RA0 and RA1) are not constrained by \overline{WE} or \overline{RE} operation.
 - H = High Voltage Level
 - L = Low Voltage Level
 - X= Don't Care
 - Z = High Impedance "Off" State

^{1.} The Write Address (WA0 and WA1) to the "internal latches" must be stable while \overline{WE} is LOW for conventional operation.

Absolute Maximum Ratings

DC Supply Voltage, V _{CC} 0.5V to 7V
DC Input Diode Current, I _{IK}
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ±20mA
DC Output Diode Current, I _{OK}
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$
DC Drain Current, per Output, IO
For $-0.5V < V_O < V_{CC} + 0.5V$ ±35mA
DC Output Source or Sink Current per Output Pin, IO
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$
DC V _{CC} or Ground Current, I _{CC}

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
E (PDIP) Package	67
M (SOIC) Package	73
Maximum Junction Temperature	
Maximum Storage Temperature Range6	5 ⁰ C to 150 ⁰ C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range, T _A
Supply Voltage Range, V _{CC}
HC Types2V to 6V
HCT Types
DC Input or Output Voltage, V _I , V _O
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		TES CONDI		V _{CC}	25°C			-40°C 1	O 85°C	-55°C TO 125°C		
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(S)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES					-	-		-				
High Level Input	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output	VoH	VOH VIH OT VIL	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
Voltage CMOS Loads			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
omeo Edudo			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output	7		-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
112 20000			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
omeo Edudo			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output	7		-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	II	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μΑ

DC Electrical Specifications (Continued)

		TES CONDI	_	V _{CC}		25°C		-40°C 1	O 85°C	-55°C T	O 125°C	
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Quiescent Device Current	Icc	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μΑ
Three- State Leakage Current		V _{IL} or V _{IH}	V _O = V _{CC} or GND	6	-	-	±0.5	-	±5.0	-	±10	μА
HCT TYPES			•		•							
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{ОН}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lį	V _{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	μΑ
Quiescent Device Current	Icc	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μА
Three- State Leakage Current		V _{IL} or V _{IH}	V _O = V _{CC} or GND	5.5	-	-	±0.5	-	±5.0	-	±10	μА
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 4)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μА

NOTE:

HCT Input Loading Table

INPUT	UNIT LOADS
WE	0.3
WA0	0.2
WA1	0.4
RE	1.5
DATA	0.15
RA0	0.4
RA1	0.7

NOTE: Unit Load is Δl_{CC} limit specific in DC Electrical Specifications Table, e.g., 360µA max. at $25^{0}C.$

^{4.} For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

Prerequisite for Switching Specifications

				25°C		-40	°C TO 85	5°C	-55 ⁰	°C TO 12	5°C	
PARAMETER	SYMBOL	V _{CC} (V)	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
HC TYPES							•					
Setup Time	t _{SU} , t _h	2	60	-	-	75	-	-	90	-	-	ns
Data to $\overline{\text{WE}}$ Write to $\overline{\text{WE}}$		4.5	12	-	-	15	-	-	18	-	-	ns
		6	10	-	-	13	-	-	15	-	-	ns
Hold Time	t _H , t _W	2	5	-	-	5	-	-	5	-	-	ns
Data to WE Write to WE		4.5	5	-	-	5	-	-	5	-	-	ns
		6	5	-	-	5	-	-	5	-	-	ns
Pulse Width WE	t _W	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
Latch Time WE to RA0,	t _{LATCH}	2	100	-	-	125	-	-	150	-	-	ns
RA1		4.5	20	-	-	25	-	-	30	-	-	ns
		6	17	-	-	21	-	-	26	-	-	ns
HCT TYPES	•			•			•			•		
Setup Time Data to WE	t _{SU} , t _h	4.5	12	-	-	15	-	-	18	-	-	ns
Hold Time Data to WE Write to WE	t _H , t _W	4.5	5	-	-	5	-	-	5	-	-	ns
Setup Time Write to WE	t _{SU}	4.5	18	-	-	23	-	-	27	-	-	ns
Pulse Width WE	t _W	4.5	20	-	-	25	-	-	30	-	-	ns
Latch Time WE to RA0, RA1	^t LATCH	4.5	25	-	-	31	-	-	38	-	-	ns

Switching Specifications $C_L = 50pF$, Input t_r , $t_f = 6ns$

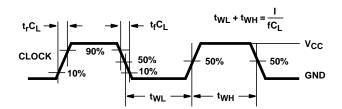
		TEST			25°C		_	С ТО °С		C TO 5°C	
PARAMETER	SYMBOL	CONDITIONS	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES											
Propagation Delay	t _{PLH} , t _{PHL}	$C_L = 50pF$									
Reading Any Word			2	-	-	195	-	245	-	295	ns
			4.5	-	-	39	-	49	-	59	ns
		C _L = 15pF	5	-	16	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	33	-	42	-	50	ns
Write Enable to Output	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	43	-	54	-	64	ns

Switching Specifications $C_L = 50 pF$, Input t_r , $t_f = 6 ns$ (Continued)

		TEST			25°C		-40 ⁰ 85	C TO °C			
PARAMETER	SYMBOL	CONDITIONS	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Data to Output	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	256	-	315	-	375	ns
			4.5	-	-	50	-	63	-	+	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	43	-	54	-	64	ns
Output Disable Time	t _{PLZ} , t _{PHZ}	$C_L = 50pF$	2	-	-	150	-	190	-	225	ns
			4.5	1	-	30	-	38	1	45	ns
		C _L = 15pF	5	1	12	-	1	-	-	-	ns
		$C_L = 50pF$	6	ı	-	26	ı	33	ı	38	ns
Output Enable Time	t _{PZL} , t _{PZH}	$C_L = 50pF$	2	1	-	150	-	190	1	225	ns
			4.5	-	-	30	-	38	-	45	ns
		$C_L = 15pF$	5	ı	12	-	ı	-	ı	-	ns
		$C_L = 50pF$	6	1	-	26	-	33	1	38	ns
Output Transition Time	t _{THL} , t _{TLH}	$C_L = 50pF$	2	1	-	75	1	95	-	110	ns
			4.5	ı	-	15	ı	19	ı	22	ns
			6	-	-	13	-	10	-	19	ns
Input Capacitance	Cl	$C_L = 50pF$	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	CO	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 5, 6)	C _{PD}	C _L = 15pF	5	-	59	-	-	-	-	-	pF
HCT TYPES					<u> </u>			<u> </u>		<u> </u>	
Propagation Delay Reading Any Word	t _{PHL} , t _{PLH}	C _L = 50pF	4.5	-	-	40	-	50	-	53	ns
		C _L = 15pF	5	-	17	-	-	-	-	-	ns
Write Enable to Output	t _{PHL} , t _{PLH}	C _L = 50pF	4.5	-	-	50	-	63	-	75	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
Data to Output	t _{PHL} , t _{PLH}	C _L = 50pF	4.5	-	-	50	-	63	-	75	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
Output Disable Time	t _{PLZ} , t _{PHZ}	C _L = 50pF	4.5	-	-	35	-	44	-	53	ns
		C _L = 15pF	5	-	14	-	-	-	-	-	ns
Output Enable Time	t _{PZL} , t _{PZH}	C _L = 50pF	4.5	-	-	38	-	48	-	57	ns
		C _L = 15pF	5	-	16	-	-	-	-	-	ns
Output Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C _l	C _L = 50pF	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	CO	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 5, 6)	C _{PD}	C _L = 15pF	5	-	66	-	-	-	-	-	pF

- 5. $\ensuremath{C_{PD}}$ is used to determine the dynamic power consumption, per output.
- 6. P_D = C_{PD} V_{CC}² f_i + Σ C_L V_{CC}² f_O where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V $_{CC}$ to 90% V $_{CC}$ in accordance with device truth table. For f $_{MAX}$, input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

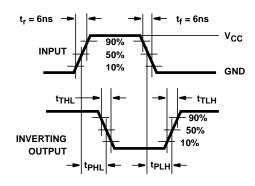


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

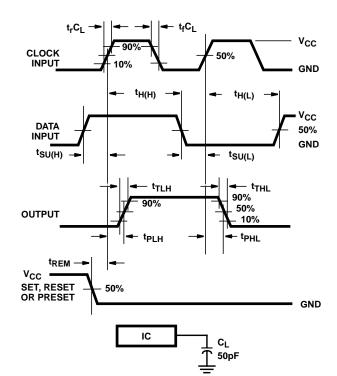
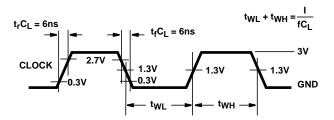


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS



NOTE: Outputs should be switching from 10% V $_{CC}$ to 90% V $_{CC}$ in accordance with device truth table. For f $_{MAX}$, input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

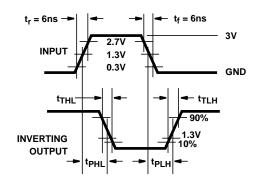


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

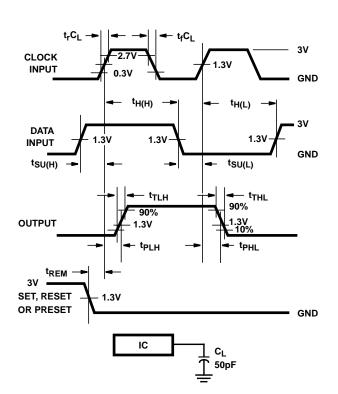
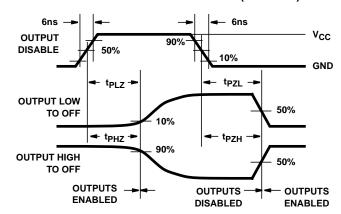


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Test Circuits and Waveforms (Continued)



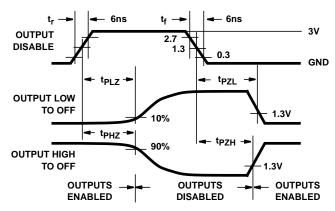
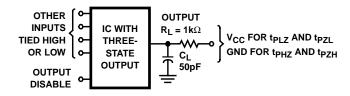


FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT



28-Aug-2010

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CD74HC670E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
CD74HC670EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
CD74HC670M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD74HC670M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
CD74HC670M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
CD74HC670M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
CD74HC670ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD74HC670MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD74HC670MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD74HC670MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD74HC670MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD74HCT670E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
CD74HCT670EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
CD74HCT670M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
CD74HCT670ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
CD74HCT670MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office

⁽¹⁾ The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.



PACKAGE OPTION ADDENDUM

28-Aug-2010

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC670M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC670M96	SOIC	D	16	2500	333.2	345.9	28.6

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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