

SN74LVC1GU04

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SCES215U-APRIL 1999-REVISED JUNE 2011

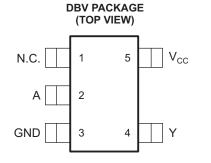
SINGLE INVERTER GATE

Check for Samples: SN74LVC1GU04

FEATURES

- Available in the Texas Instruments NanoFree[™] Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- **Unbuffered Output**
- Max t_{pd} of 3.7 ns at 3.3 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V

- I_{off} Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78. Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

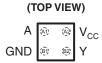


See mechanical drawings for dimensions. N.C. - No internal connection





YZV PACKAGE



		CKA VIEW	
N.C.	1	6	V _{cc}
А	2	5	N.C.
GND	3	4	Y

DCK PACKAGE

(TOP VIEW)

2

3

5

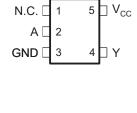
4

N.C.

GND [

A | |

 $\Box V_{cc}$



DRL PACKAGE

(TOP VIEW)



Table 1. YZP PACKAGE TERMINAL ASSIGNMENTS

	1	2
Α	DNU	V _{CC}
В	А	No ball
С	GND	Y

Table 2. YZV PACKAGE TERMINAL ASSIGNMENTS

	1	2
Α	А	V _{CC}
В	GND	Y

DESCRIPTION/ORDERING INFORMATION

This single inverter gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1GU04 contains one inverter with an unbuffered output and performs the Boolean function $Y = \overline{A}$.

NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet. NanoFree is a trademark of Texas Instruments.

SN74LVC1GU04

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STRUMENTS

XAS

ORDERING INFORMATION

T _A	PACKAGE	(1) (2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Real of 2000	SN74LVC1GU04YZPR	CD_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZV (Pb-free)		SN74LVC1GU04YZVR	ĊD
	µQFN – DSF	Reel of 5000	SN74LVC1GU04DSFR	CD
–40°C to 85°C	QFN – DRY	Reel of 5000	SN74LVC1GU04DRYR	CD
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1GU04DBVR	CU4
	SOT (SOT-23) - DBV	Reel of 250	SN74LVC1GU04DBVT	- 004_
		Reel of 3000	SN74LVC1GU04DCKR	CD
	SOT (SC-70) – DCK	Reel of 250	SN74LVC1GU04DCKT	- CD_
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1GU04DRLR	CD_

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free). YZV: The actual top-side marking is on two lines. Line 1 has four characters to denote year, month, day, and assembly/test site. Line 2 has two characters which show the family and function code. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

Table 3. FUNCTION TABLE

INPUT A	OUTPUT Y
Н	L
L	н

LOGIC DIAGRAM (POSITIVE LOGIC) DBV,DSF,DRY, DCK, DRL, and YZP PACKAGE



YZV PACKAGE





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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			RATING	UNIT
V _{CC}	Supply voltage range		-0.5 to 6.5	V
VI	Input voltage range ⁽²⁾			V
Vo	Voltage range applied to any output in the high or low state ^{(2) (3)}		-0.5 to V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0	-50	mA
I _{OK}	Output clamp current	V _O < 0	-50	mA
lo	Continuous output current		±50	mA
	Continuous current through V_{CC} or GND		±100	mA
		DBV package	206	
		DCK package	252	
		DRL package	142	
θ_{JA}	Package thermal impedance ⁽⁴⁾	YZP package	132	°C/W
		YZV package	116	
		DSF package	300	1
		DRY package	234	1
T _{stg}	Storage temperature range		-65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	5.5	V
V_{IH}	High-level input voltage	I _O = −100 μA	0.75 × V _{CC}		V
V_{IL}	Low-level input voltage	I _O = 100 μA		$0.25 \times V_{CC}$	V
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
		$V_{CC} = 2.3 V$		-8	
I _{OH}	High-level output current	N 2 N		–16	mA
		V _{CC} = 3 V		-24	
		$V_{CC} = 4.5 V$		-32	
		V _{CC} = 1.65 V		4	
		$V_{CC} = 2.3 V$		8	
I _{OL}	Low-level output current	$\mathcal{V} = 2\mathcal{V}$		16	mA
		$V_{CC} = 3 V$		24	
		$V_{CC} = 4.5 V$		32	
T _A	Operating free-air temperature		-40	85	°C

 All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT			
		I _{OH} = −100 μA	1.65 V to 5.5 V	V _{CC} - 0.1						
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2						
N/	N 0.V	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V			
V _{OH}	$V_{IL} = 0 V$	I _{OH} = -16 mA	2.1/	2.4			V			
		I _{OH} = -24 mA	3 V	2.3						
		I _{OH} = -32 mA	4.5 V	3.8						
		I _{OL} = 100 μA	1.65 V to 5.5 V			0.1				
	V _{IH} = V _{CC}	$I_{OL} = 4 \text{ mA}$	1.65 V			0.45				
N/		I _{OL} = 8 mA	2.3 V			0.3	V			
V _{OL}		I _{OL} = 16 mA	2.1/			0.4				
		I _{OL} = 24 mA	mA 3 V			0.55				
		I _{OL} = 32 mA	4.5 V			0.55				
II A input	$V_1 = 5.5 V \text{ or GND}$		0 to 5.5 V			±5	μA			
I _{CC}	$V_{I} = 5.5 V \text{ or GND},$	I _O = 0	1.65 V to 5.5 V			10	μA			
C _i	$V_{I} = V_{CC}$ or GND		3.3 V		7		pF			

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (See Figure 1)

PARAMETER	FROM (INPUT)	TO (INPUT)	V _{CC} = ±0.1		V _{CC} = ±0.2		V _{CC} = ±0.3		V _{CC} = ±0.5		UNIT
	(INPUT)	(INPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	А	Y	1.3	5	1	4	1.1	3.7	1	3	ns

Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	$V_{CC} = 2.5 V$	$V_{CC} = 3.3 V$	$V_{CC} = 5 V$		
PARAMETER	FARAMETER	TEST CONDITIONS	ТҮР	TYP	TYP	TYP	UNIT	
C_{pd}	Power dissipation capacitance	f = 10 MHz	9	11	13	27	pF	

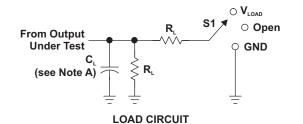


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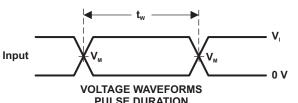
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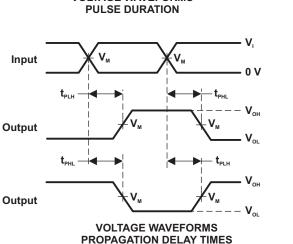
PARAMETER MEASUREMENT INFORMATION



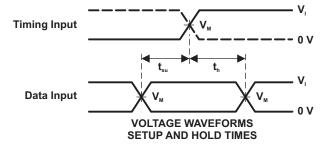
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	VLOAD
t_{PHZ}/t_{PZH}	GND

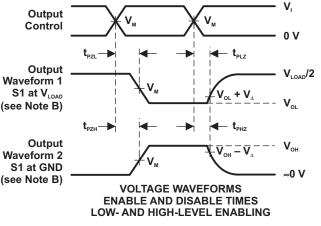
N N	INF	PUTS	V	V	•		N
V _{cc}	V	t,/t,	V _M	VLOAD	C	R	V
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V
$2.5 V \pm 0.2 V$	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5 V \pm 0.5 V$	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V





INVERTING AND NONINVERTING OUTPUTS





NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z₀ = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PHZ} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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21-Oct-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74LVC1GU04DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	· · · · · ·
74LVC1GU04DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1GU04DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1GU04DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1GU04DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1GU04DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1GU04DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1GU04DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1GU04DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1GU04DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1GU04DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1GU04DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1GU04DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1GU04DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1GU04DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1GU04DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1GU04YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	



21-Oct-2011

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LVC1GU04YZVR	ACTIVE	DSBGA	YZV	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

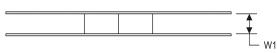
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TEXAS INSTRUMENTS





TAPE AND REEL INFORMATION

TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

B0

K0

P1

w

Pin1

A0

*All dimensions are nominal						
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)
SN74LVC1GU04DBVR	SOT-23	DBV	5	3000	178.0	9.2
SN74LVC1GU04DBVR	SOT-23	DBV	5	3000	178.0	9.0
SN74LVC1GU04DBVT	SOT-23	DBV	5	250	178.0	9.0

Denie	Туре	Drawing		0.4	Diameter (mm)	Width W1 (mm)	(mm)	(mm)	(mm)	(mm)	(mm)	Quadrant
SN74LVC1GU04DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1GU04DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1GU04DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1GU04DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1GU04DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1GU04DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1GU04DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1GU04DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1GU04DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1GU04DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1GU04DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1GU04DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1GU04DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1GU04YZPR	DSBGA	YZP	5	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1GU04YZVR	DSBGA	YZV	4	3000	180.0	8.4	1.02	1.02	0.63	4.0	8.0	Q1

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PACKAGE MATERIALS INFORMATION

14-Mar-2012



*All dimensions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1GU04DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1GU04DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1GU04DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1GU04DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1GU04DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1GU04DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74LVC1GU04DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1GU04DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1GU04DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74LVC1GU04DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1GU04DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74LVC1GU04DRYR	SON	DRY	6	5000	180.0	180.0	30.0
SN74LVC1GU04DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74LVC1GU04YZPR	DSBGA	YZP	5	3000	220.0	220.0	34.0
SN74LVC1GU04YZVR	DSBGA	YZV	4	3000	220.0	220.0	34.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

D. Falls within JEDEC MO-178 Variation AA.



DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.

- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.



LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



NOTES:

All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. Α. B. This drawing is subject to change without notice.

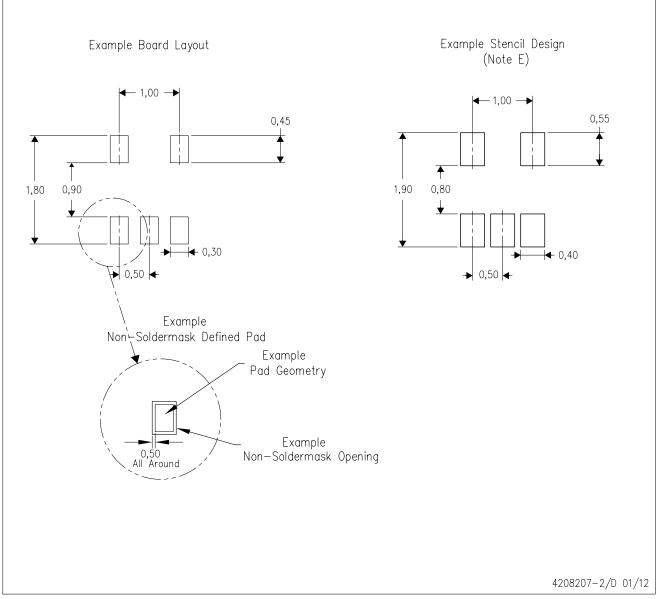
🖄 Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.





DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

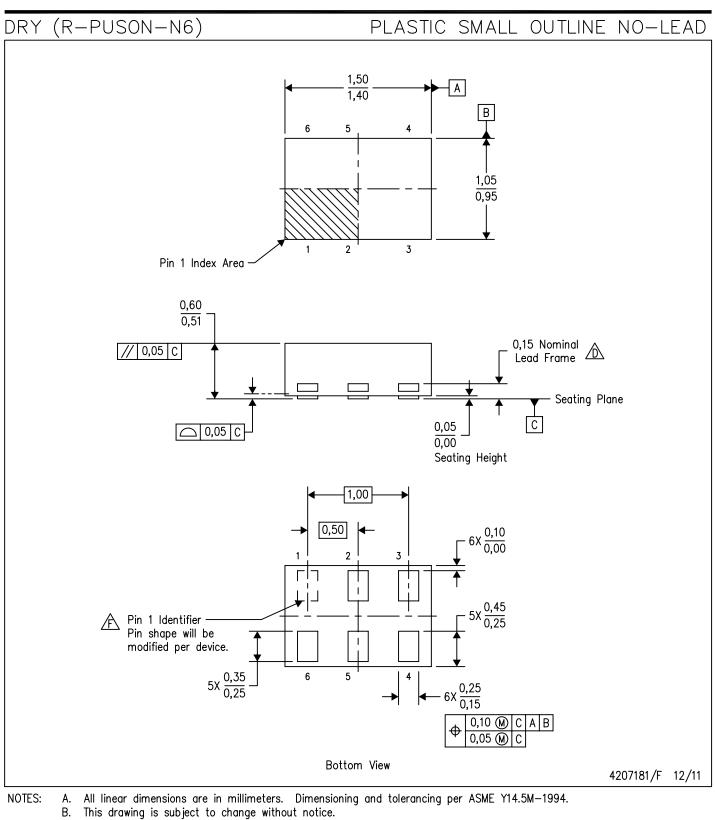


NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



MECHANICAL DATA

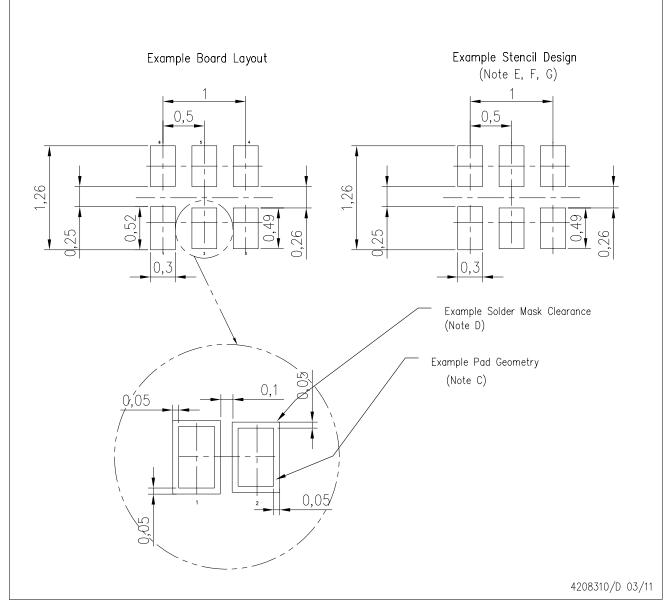


- C. SON (Small Outline No-Lead) package configuration.
- Δ The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
- E. This package complies to JEDEC MO-287 variation UFAD.
- 🖄 See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.



DRY (S-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



MECHANICAL DATA



- - B. This drawing is subject to change without notice.
 C. SON (Small Outline No-Lead) package configuration.
 D. This package complies to JEDEC M0-287 variation X2AAF.





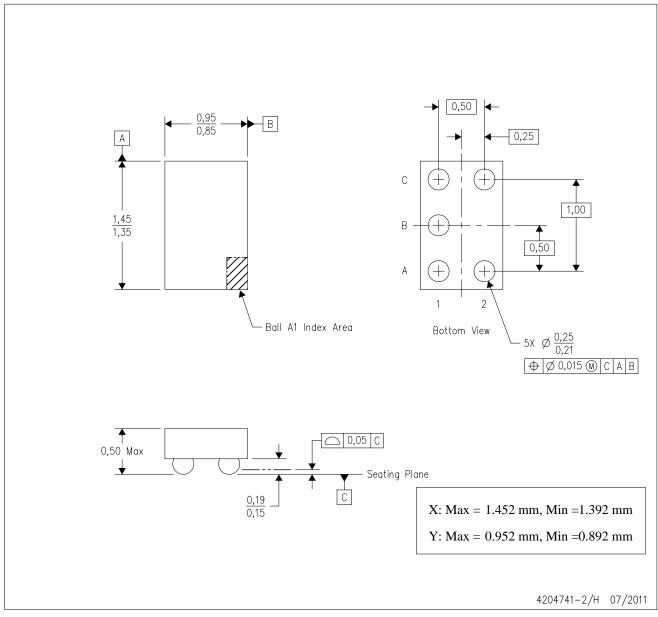
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- H. Component placement force should be minimized to prevent excessive paste block deformation.



YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

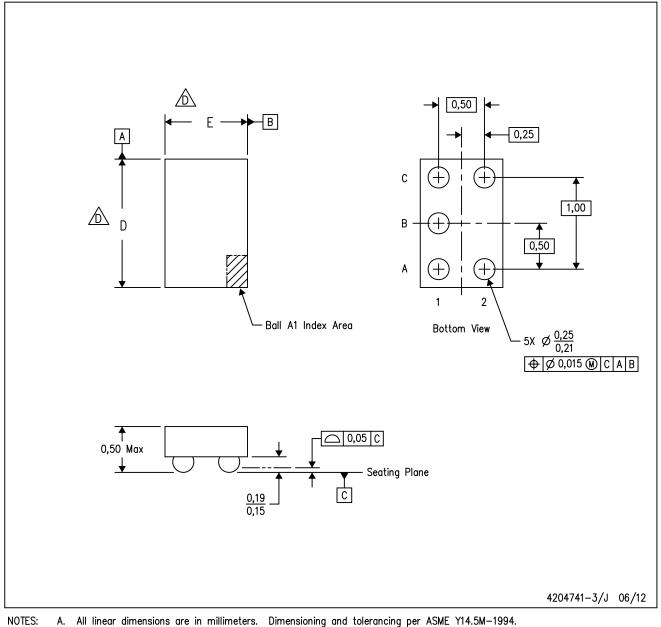
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. This package is a Pb-free solder ball design. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.



YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



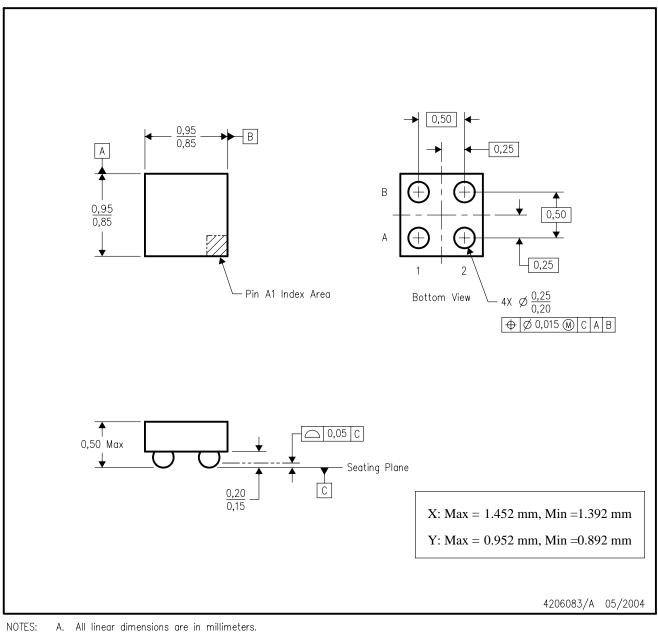
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
- E. This package is a Pb-free solder ball design. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.



YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package contains lead-free balls. Refer to the 4 YEV package (drawing 4206082) for tin-lead (SnPb) balls.

NanoFree is a trademark of Texas Instruments.



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