SN54AC374, SN74AC374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS543E - OCTOBER 1995 - REVISED OCTOBER 2003

- 2-V to 6-V V_{CC} Operation
- Inputs Accept Voltages to 6 V
- Max t_{pd} of 9.5 ns at 5 V
- 3-State Noninverting Outputs Drive Bus Lines Directly
- Full Parallel Access for Loading

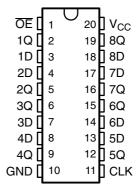
description/ordering information

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

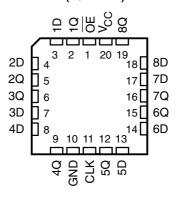
The eight flip-flops of the 'AC374 devices are D-type edge-triggered flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

SN54AC374 . . . J OR W PACKAGE SN74AC374 . . . DB, DW, N, NS, OR PW PACKAGE (TOP VIEW)



SN54AC374 . . . FK PACKAGE (TOP VIEW)



OE does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

ORDERING INFORMATION

T _A	PACKAG	Ε [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74AC374N	SN74AC374N
	0010 PW	Tube	SN74AC374DW	10074
	SOIC – DW	Tape and reel	SN74AC374DWR	AC374
-40°C to 85°C	SOP - NS	Tape and reel	SN74AC374NSR	AC374
	SSOP – DB	Tape and reel	SN74AC374DBR	AC374
	TOCOD DW	Tube	SN74AC374PW	10074
	TSSOP – PW	Tape and reel	SN74AC374PWR	AC374
	CDIP – J	Tube	SNJ54AC374J	SNJ54AC374J
-55°C to 125°C	CFP – W Tube		SNJ54AC374W	SNJ54AC374W
	LCCC - FK	Tube	SNJ54AC374FK	SNJ54AC374FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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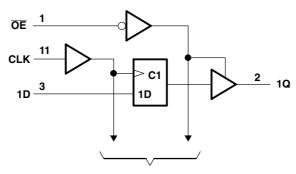
description/ordering information (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	↑	Н	Н
L	\uparrow	L	L
L	H or L	Χ	Q_0
Н	X	Χ	Z

logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		· · · · · · · · · · · · · · · · · · ·
Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		. $-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V _O (see Note 1)		. $-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)		±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CO}$		
Continuous output current, I_O ($V_O = 0$ to V_{CC})		
Continuous current through V _{CC} or GND		±200 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DB package	70°C/W
	DW package	58°C/W
	N package	69°C/W
	NS package	60°C/W
	PW package	83°C/W
Storage temperature range, $T_{stg}\dots\dots$		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 3)

			SN54A	C374	SN74A	C374	
			MIN	MAX	MIN	MAX	UNIT
V _{CC}	Supply voltage		2	6	2	6	V
		V _{CC} = 3 V	2.1		2.1		
V_{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15		3.15		V
		V _{CC} = 5.5 V	3.85		3.85		
		V _{CC} = 3 V		0.9		0.9	
V_{IL}	Low-level input voltage	$V_{CC} = 4.5V$		1.35		1.35	V
		V _{CC} = 5.5 V		1.65		1.65	
VI	Input voltage		0	V_{CC}	0	V_{CC}	V
Vo	Output voltage		0	V_{CC}	0	V_{CC}	V
		V _{CC} = 3 V		-12		-12	
I _{OH}	High-level output current	V _{CC} = 4.5 V		-24		-24	mA
		V _{CC} = 5.5 V		-24		-24	
		V _{CC} = 3 V		12		12	
I_{OL}	Low-level output current	V _{CC} = 4.5 V		24		24	mA
		V _{CC} = 5.5 V		24		24	
Δt/Δν	Input transition rise or fall rate	-		8		8	ns/V
T _A	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPITIONS	\ ,	T,	_A = 25°C	SN54AC37	4 SN	174AC374	
PARAMETER	TEST CONDITIONS	v _{cc}	MIN	TYP MAX	MIN MA	X N	IIN MAX	UNIT
		3 V	2.9		2.9	2	2.9	
	$I_{OH} = -50 \mu A$	4.5 V	4.4		4.4		4.4	
V		5.5 V	5.4		5.4		5.4	V
V _{OH}	$I_{OH} = -12 \text{ mA}$	3 V	2.56		2.4	2	46	V
		4.5 V	3.86		3.7	3	76	
	I _{OH} = -24 mA	5.5 V	4.86		4.7	4	76	
		3 V		0.1	(.1	0.1	
	I _{OL} = 50 μA	4.5 V		0.1	(.1	0.1	
.,		5.5 V		0.1	(.1	0.1	V
V _{OL}	I _{OL} = 12 mA	3 V		0.36	(.5	0.44	V
	J 04 mA	4.5 V		0.36	(.5	0.44	
	I _{OL} = 24 mA	5.5 V		0.36	(.5	0.44	
I _I	$V_I = V_{CC}$ or GND	5.5 V		±0.1		±1	±1	μΑ
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±0.25		±5	±2.5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		4		30	40	μΑ
C _i	$V_I = V_{CC}$ or GND	5 V		4.5				pF

SN54AC374, SN74AC374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

		$T_A = 2$	25°C	SN54A	C374	SN74A	C374	LIMIT
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f _{clock}	Clock frequency		60		60		60	MHz
t _w	Pulse duration, CLK high or low	5.5		6.5		6		ns
t _{su}	Setup time, data before CLK↑	5.5		6.5		6		ns
t _h	Hold time, data after CLK↑	1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

		$T_A = 2$	25°C	SN54A	C374	SN74A	C374	LINUT
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f _{clock}	Clock frequency		100		95		100	MHz
t _w	Pulse duration, CLK high or low	4		5		4.5		ns
t _{su}	Setup time, data before CLK↑	4		5		4.5		ns
t _h	Hold time, data after CLK↑	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

	_		_			ı		1		1
DADAMETED	то	то	T,	T _A = 25°C			C374	SN74A	C374	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
f _{max}			60	110		60		60		MHz
t _{PLH}	0114	•	3	11	13.5	3	16.5	1.5	15.5	
t _{PHL}	CLK	Q	2.5	10	12.5	3	15	2	14	ns
t _{PZH}	OF.	•	3	9.5	11.5	1	14	1.5	13	
t _{PZL}	ŌĒ	Q	3.5	9	11.5	1	14	1.5	13	ns
t _{PHZ}	OF.	Q	3	10.5	12.5	1	16	2	14.5	no
t_{PLZ}	ŌĒ	Q	2	8	11.5	1	13	1	12.5	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

	TO	ТО	T _A = 25°C			SN54AC374		SN74AC374		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
f _{max}			100	155		95		100		MHz
t _{PLH}	OLIV.	^	2.5	8	9.5	3	12	1.5	10.5	
t _{PHL}	CLK	Q	2	7	9	3	11	1.5	10	ns
t _{PZH}	0 5	0	2	7	8.5	1.5	10	1	9.5	
t _{PZL}	ŌĒ	Q	2	6.5	8.5	1.5	10.5	1	9.5	ns
t _{PHZ}	O.F.	Q	2	8	11	1.5	12.5	2	12.5	
t _{PLZ}	ŌĒ	ď	1.5	6.5	8.5	1.5	10.5	1	10	ns

operating characteristics, V_{CC} = 5 V, T_A = 25°C

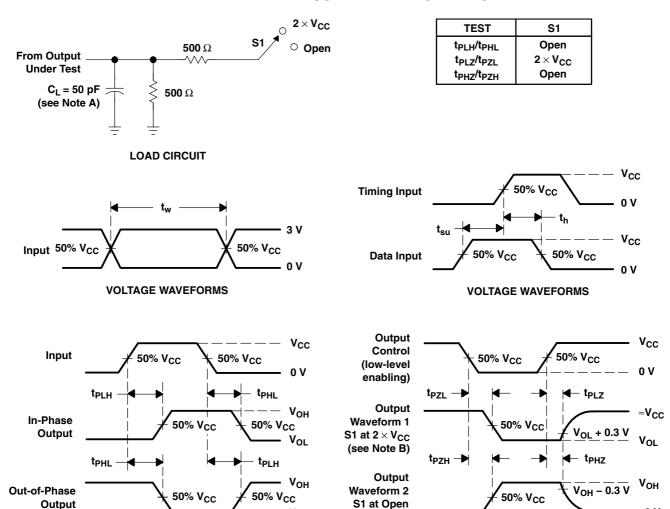
	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	$C_L = 50 \text{ pF}, \qquad f = 1 \text{ MHz}$	40	pF



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VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

VOLTAGE WAVEFORMS

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_{O} = 50 \Omega$, $t_{f} \leq 2.5 \text{ ns}$.

(see Note B)

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



23-Mar-2012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-87694012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8769401RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-8769401SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
5962-8769401VRA	ACTIVE	CDIP	J	20	20	TBD	A42	N / A for Pkg Type	
5962-8769401VSA	ACTIVE	CFP	W	20	25	TBD	Call TI	N / A for Pkg Type	
SN74AC374DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	
SN74AC374DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AC374NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AC374NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74AC374PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	
SN74AC374PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC374PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54AC374FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54AC374J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54AC374W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



PACKAGE OPTION ADDENDUM

23-Mar-2012

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OTHER QUALIFIED VERSIONS OF SN54AC374, SN54AC374-SP, SN74AC374:

● Catalog: SN74AC374, SN54AC374

Military: SN54AC374

Space: SN54AC374-SP

NOTE: Qualified Version Definitions:

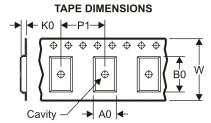
- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

PACKAGE MATERIALS INFORMATION

www.ti.com 5-May-2011

TAPE AND REEL INFORMATION





Α	0	Dimension designed to accommodate the component width
В	0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
٧	٧	Overall width of the carrier tape
ГР	1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All difficulties are notifical												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC374DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC374DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74AC374NSR	so	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74AC374PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

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*All dimensions are nominal

7 III GIITTOTTO GIO TIOTIMA										
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)			
SN74AC374DBR	SSOP	DB	20	2000	346.0	346.0	33.0			
SN74AC374DWR	SOIC	DW	20	2000	346.0	346.0	41.0			
SN74AC374NSR	SO	NS	20	2000	346.0	346.0	41.0			
SN74AC374PWR	TSSOP	PW	20	2000	346.0	346.0	33.0			

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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