

25-BIT CONFIGURABLE REGISTERED BUFFER WITH ADDRESS-PARITY TEST

FEATURES

- Member of the Texas Instruments Widebus+[™] Family
- Pinout Optimizes DDR2 DIMM PCB Layout
- Configurable as 25-Bit 1:1 or 14-Bit 1:2 **Registered Buffer**
- **Chip-Select Inputs Gate the Data Outputs from** Changing State and Minimizes System Power Consumption
- **Output Edge-Control Circuitry Minimizes** Switching Noise in an Unterminated Line

- Supports SSTL 18 Data Inputs •
- Differential Clock (CLK and CLK) Inputs ٠
- Supports LVCMOS Switching Levels on the Control and RESET Inputs
- Checks Parity on DIMM-Independent Data Inputs
- Able to Cascade with a Second • 74SSTUB32866A
- RESET Input Disables Differential Input **Receivers, Resets All Registers, and Forces** All Outputs Low, Except QERR

DESCRIPTION

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V VCC operation. In the 1:1 pinout configuration, only one device per DIMM is required to drive nine SDRAM loads. In the 1:2 pinout configuration, two devices per DIMM are required to drive 18 SDRAM loads.

All inputs are SSTL_18, except the reset (RESET) and control (Cn) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for unterminated DIMM loads and meet SSTL 18 specifications, except the open-drain error (QERR) output.

The 74SSTUB32866A operates from a differential clock (CLK and CLK). Data are registered at the crossing of CLK going high and CLK going low.

The 74SSTUB32866A accepts a parity bit from the memory controller on the parity bit (PAR IN) input, compares it with the data received on the DIMM-independent D-inputs (D2–D3, D5–D6, D8–D25 when C0 = 0 and C1 = 0: D2–D3. D5–D6. D8–D14 when C0 = 0 and C1 = 1; or D1-D6. D8-D13 when C0 = 1 and C1 = 1) and indicates whether a parity error has occurred on the open-drain QERR pin (active low). The convention is even parity; i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs, combined with the parity input bit. To calculate parity, all DIMM-independent data inputs must be tied to a known logic state.

When used as a single device, the C0 and C1 inputs are tied low. In this configuration, parity is checked on the PAR_IN input signal, which arrives one cycle after the input data to which it applies. Two clock cycles after the data are registered, the corresponding partial-parity-out (PPO) and QERR signals are generated.

When used in pairs, the C0 input of the first register is tied low, and the C0 input of the second register is tied high. The C1 input of both registers are tied high. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR IN input signal of the first device. Two clock cycles after the data are registered, the corresponding PPO and QERR signals are generated on the second device. The PPO output of the first register is cascaded to the PAR_IN of the second 74SSTUB32866A. The QERR output of the first 74SSTUB32866A is left floating, and the valid error information is latched on the QERR output of the second 74SSTUB32866A.

ORDERING INFORMATION

T _A PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	LFBGA–ZKE	Tape and reel	74SSTUB32866AZKER	SB866A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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DESCRIPTION (CONTINED)

If an error occurs and the QERR output is driven low, it stays latched low for a minimum of two clock cycles or until RESET is driven low. If two or more consecutive parity errors occur, the QERR output is driven low and latched low for a clock duration equal to the parity-error duration or until RESET is driven low. The DIMM-dependent signals (DCKE, DCS, DODT, and CSR) are not included in the parity-check computation.

The C0 input controls the pinout configuration of the 1:2 pinout from register-A configuration (when low) to register-B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high). C0 and C1 should not be switched during normal operation. They should be hard-wired to a valid low or high level to configure the register in the desired mode. In the 25-bit 1:1 pinout configuration, the A6, D6, and H6 terminals are driven low and are do-not-use (DNU) pins.

In the DDR2 RDIMM application, RESET is specified to be completely asynchronous with respect to CLK and CLK. Therefore, no timing relationship can be ensured between the two. When entering reset, the register is cleared, and the data outputs are driven low quickly, relative to the time required to disable the differential input receivers. However, when coming out of reset, the register becomes active quickly, relative to the time required to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of RESET until the input receivers are fully enabled, the design of the 74SSTUB32866A ensures that the outputs remain low, thus ensuring there will be no glitches on the output.

To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

The device supports low-power standby operation. When $\overrightarrow{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overrightarrow{\text{RESET}}$ is low, all registers are reset and all outputs are forced low, except $\overrightarrow{\text{QERR}}$. The LVCMOS $\overrightarrow{\text{RESET}}$ and Cn inputs always must be held at a valid logic high or low level.

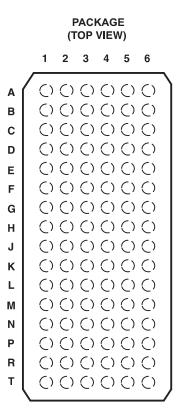
The device also supports low-power active operation by monitoring both system chip select (\overline{DCS} and \overline{CSR}) inputs and gates the Qn and PPO outputs from changing states when both \overline{DCS} and \overline{CSR} inputs are high. If either DCS or CSR input is low, the Qn and PPO outputs function normally. Also, if the internal low-power signal (LPS1) is high (one cycle after \overline{DCS} and \overline{CSR} go high), the device gates the \overline{QERR} output from changing states. If $\overline{LPS1}$ is low, the \overline{QERR} output functions normally. The \overline{RESET} input has priority over the \overline{DCS} and \overline{CSR} control and, when driven low, forces the Qn and PPO outputs low and forces the \overline{QERR} output high. If the \overline{DCS} control functionality is not desired, the \overline{CSR} input can be hard-wired to ground, in which case the setup-time requirement for \overline{DCS} is the same as for the other D data inputs. To control the low-power mode with \overline{DCS} only, the \overline{CSR} input should be pulled up to V_{CC} through a pullup resistor.

The two V_{REF} pins (A3 and T3) are connected together internally by approximately 150 Ω . However, it is necessary to connect only one of the two V_{REF} pins to the external V_{REF} power supply. An unused V_{REF} pin should be terminated with a V_{REF} coupling capacitor.

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Terminal Assignments for 1:1 Register-A (C0 = 0, C1 = 0)

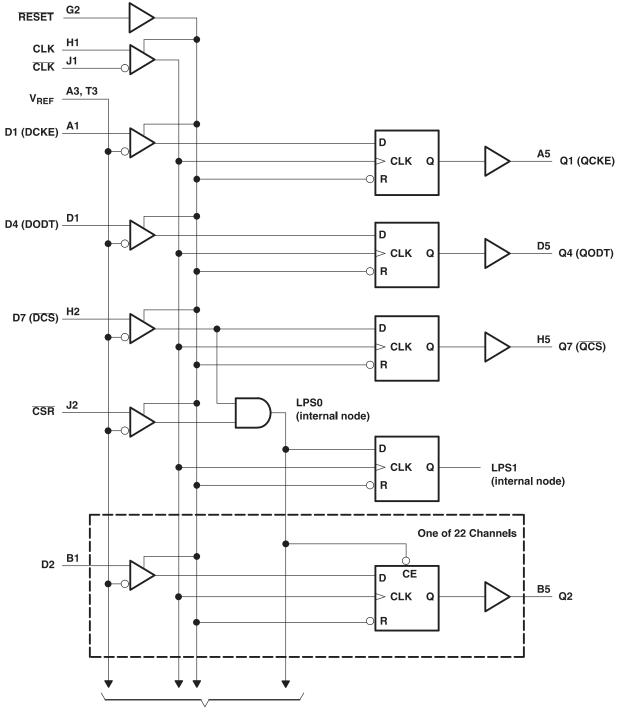
_	1	2	3	4	5	6
Α	D1 (DCKE)	PPO	V _{REF}	V _{CC}	Q1 (QCKE)	DNU
в	D2	D15	GND	GND	Q2	Q15
S	D3	D16	V _{CC}	V _{CC}	Q3	Q16
D	D4 (DODT)	QERR	GND	GND	Q4 (QODT)	DNU
Ε	D5	D17	V _{CC}	V _{CC}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	PAR_IN	RESET	V_{CC}	V _{CC}	C1	C0
Н	CLK	D7 (DCS)	GND	GND	Q7 (<u>QCS</u>)	DNU
J	CLK	CSR	V _{CC}	V _{CC}	NC	NC
κ	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V_{CC}	V _{cc}	Q9	Q20
М	D10	D21	GND	GND	Q10	Q21
Ν	D11	D22	V_{CC}	V _{CC}	Q11	Q22
Ρ	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V _{CC}	V _{CC}	Q13	Q24
Т	D14	D25	V_{REF}	V _{CC}	Q14	Q25

Each pin name in parentheses indicates the DDR2 DIMM signal name.

DNU - Do not use

NC - No internal connection

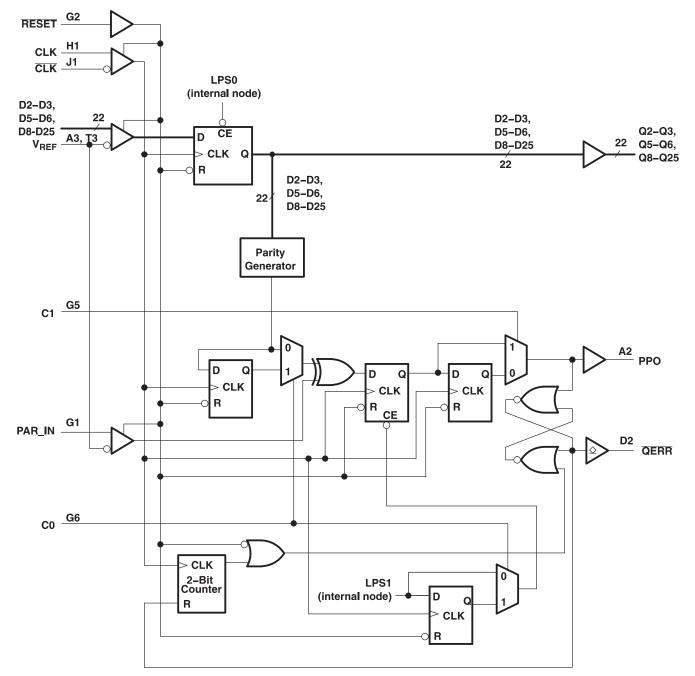
Logic Diagram for 1:1 Register Configuration (Positive Logic); C0 = 0, C1 = 0



To 21 Other Channels (D3, D5, D6, D8-D25)

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Parity Logic Diagram for 1:1 Register Configuration (Positive Logic); C0 = 0, C1 = 0



	PACKAGE (TOP VIEW)							
	1	2	3	4	5	6	_	
A	$\int c$) (`) ()	()	()	()		
в		$) \subset$	$) \bigcirc$	\bigcirc	\bigcirc	()		
с		$) \subset$	$) \bigcirc$	\bigcirc	\bigcirc	()		
D		$) \subset$	$) \bigcirc$	()	\bigcirc	()		
Е		$) \subset$	$) \bigcirc$	\bigcirc	\bigcirc	()		
F		$) \subset$	$) \bigcirc$	()	\bigcirc	()		
G		$) \subset$) ()	()	\bigcirc	()		
н		$) \subset$) ()	()	\bigcirc	()		
J		$) \subset$) ()	()	\bigcirc	()		
к) () ()	()	()	()		
L		$) \subset$) ()	()	()	()		
м		$) \subset$) ()	()	\bigcirc	()		
Ν) () ()	()	\bigcirc	()		
Р		$) \subset$	$) \bigcirc$	\bigcirc	()	()		
R		$) \subset$) ()	()	\bigcirc	()		
т		$) \subset$) ()	\bigcirc	\bigcirc	()		
	/						1	

	1	2	3	4	5	6
Α	D1 (DCKE)	PPO	V_{REF}	V _{CC}	Q1A (QCKEA)	Q1B (QCKEB)
в	D2	DNU	GND	GND	Q2A	Q2B
S	D3	DNU	V _{CC}	V _{CC}	Q3A	Q3B
D	D4 (DODT)	QERR	GND	GND	Q4A (QODTA)	Q4B(QODTB)
Е	D5	DNU	V _{CC}	V _{CC}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	PAR_IN	RESET	V _{CC}	V _{CC}	C1	CO
н	CLK	D7 (DCS)	GND	GND	Q7A (QCSA)	Q7B (QCSB)
J	CLK	CSR	V _{CC}	V _{CC}	NC	NC
κ	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{CC}	V _{CC}	Q9A	Q9B
М	D10	DNU	GND	GND	Q10A	Q10B
Ν	D11	DNU	V _{CC}	V _{CC}	Q11A	Q11B
Ρ	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{CC}	V _{CC}	Q13A	Q13B
T	D14	DNU	V_{REF}	V _{CC}	Q14A	Q14B

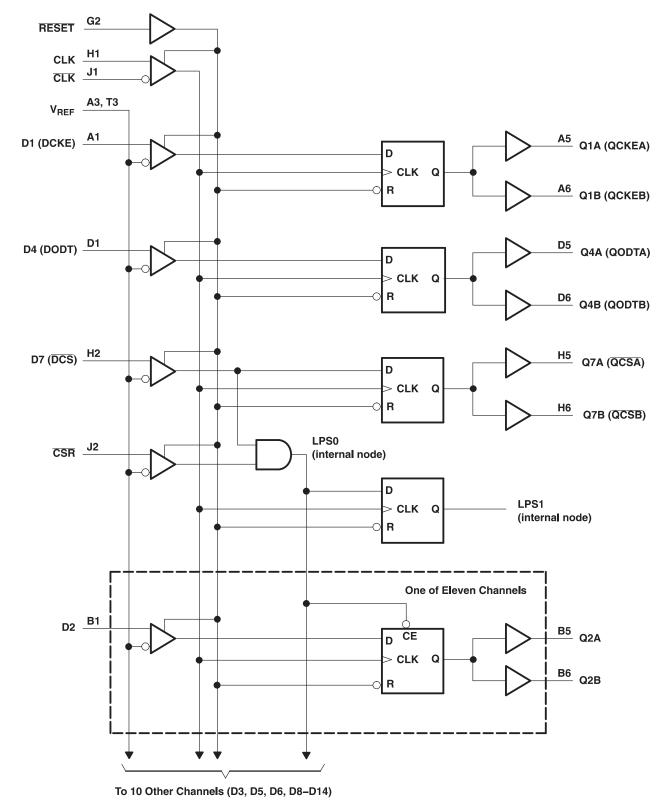
Each pin name in parentheses indicates the DDR2 DIMM signal name.

DNU - Do not use

NC - No internal connection

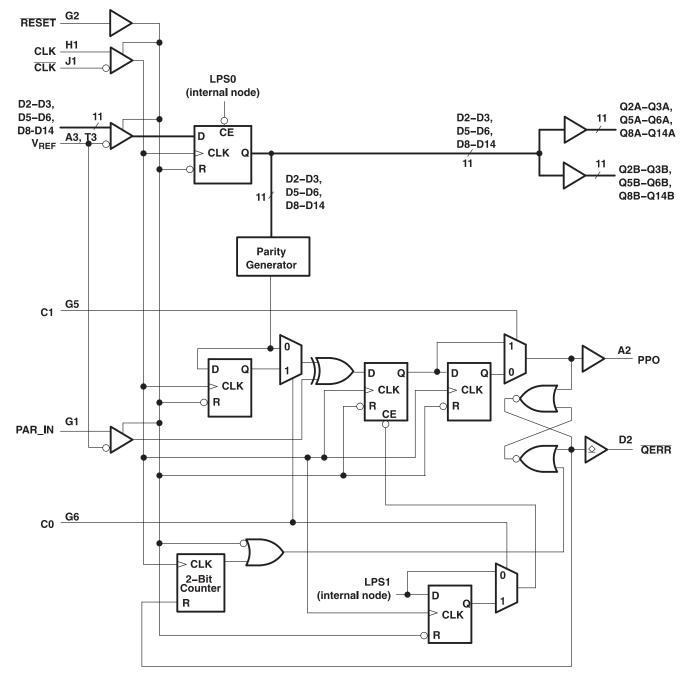
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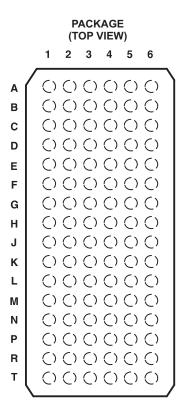
Logic Diagram for 1:2 Register-A Configuration (Positive Logic); C0 = 0, C1 = 1

Parity Logic Diagram for 1:2 Register-A Configuration (Positive Logic); C0 = 0, C1 = 1



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Terminal Assignments for 1:2 Register-b (C0 = 1, C1 = 1)

	1	2	3	4	5	6
Α	D1	PPO	V_{REF}	V _{CC}	Q1A	Q1B
В	D2	DNU	GND	GND	Q2A	Q2B
S	D3	DNU	V _{CC}	V _{CC}	Q3A	Q3B
D	D4	QERR	GND	GND	Q4A	Q4B
Е	D5	DNU	V _{CC}	V _{CC}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	PAR_IN	RESET	V _{CC}	V _{CC}	C1	CO
Н	CLK	D7 (DCS)	GND	GND	Q7A (QCSA)	Q7B (QCSB)
J	CLK	CSR	V _{CC}	V _{CC}	NC	NC
Κ	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{CC}	V _{CC}	Q9A	Q9B
Μ	D10	DNU	GND	GND	Q10A	Q10B
Ν	D11 (DODT)	DNU	V _{CC}	V _{CC}	Q11A (QODTA)	Q11B (QODTB)
Ρ	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{CC}	V _{CC}	Q13A	Q13B
Т	D14 (DCKE)	DNU	V_{REF}	V _{CC}	Q14A (QCKEA)	Q14B (QCKEB)

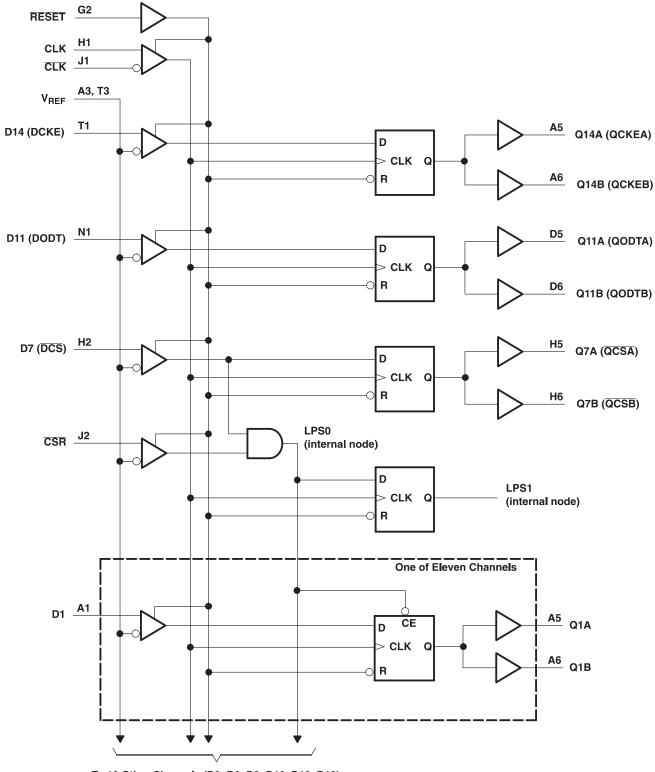
Each pin name in parentheses indicates the DDR2 DIMM signal name.

DNU - Do not use

NC - No internal connection

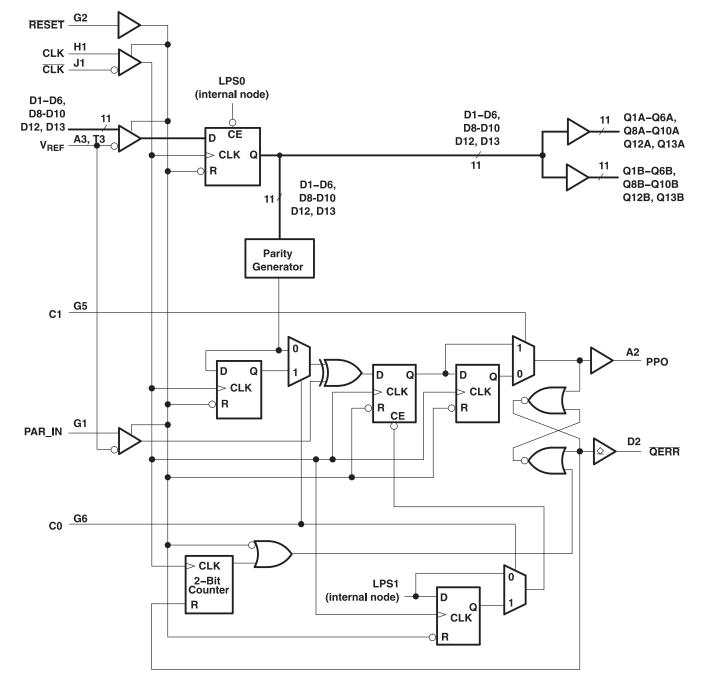


Logic Diagram for 1:2 Register-B Configuration C0 = 1, C1 = 1



To 10 Other Channels (D2-D6, D8-D10, D12-D13)





Parity Logic Diagram for 1:2 Register-b Configuration (Positive Logic); C0 = 1, C1 = 1



TERMINAL FUNCTIONS

TERMINAL NAME	DESCRIPTION	ELECTRICAL CHARACTERISTICS
GND	Ground	Ground input
V _{CC}	Power-supply voltage	1.8 V nominal
V _{REF}	Input reference voltage	0.9 V nominal
CLK	Positive master clock input	Differential input
CLK	Negative master clock input	Differential input
C0, C1	Configuration control input. Register A or Register B and 1:1 mode or 1:2 mode select.	LVCMOS inputs
RESET	Asynchronous reset input. Resets registers and disables V _{REF} , data, and clock differential-input receivers. When RESET is low, all Q outputs are forced low and the QERR output is forced high.	LVCMOS input
D1-D25	Data input. Clocked in on the crossing of the rising edge of CLK and the falling edge of CLK.	SSTL_18 inputs
CSR, DCS	Chip select inputs. Disables D1–D25 ⁽¹⁾ outputs switching when both inputs are high	SSTL_18 inputs
DODT	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL_18 input
DCKE	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL_18 input
PAR_IN	Parity input. Arrives one clock cycle after the corresponding data input. Pulldown resistor of typical $150k\Omega$ to GND.	SSTL_18 input pulldown
Q1-Q25 ⁽²⁾	Data outputs that are suspended by the DCS and CSR control.	1.8 V CMOS outputs
PPO	Partial parity out. Indicates odd parity of inputs D1–D25. (1)	1.8 V CMOS output
QCS	Data output that will not be suspended by the DCS and CSR control	1.8 V CMOS output
QODT	Data output that will not be suspended by the DCS and CSR control	1.8 V CMOS output
QCKE	Data output that will not be suspended by the DCS and CSR control	1.8 V CMOS output
QERR	Output error bit. Timing is determined by the device mode.	Open-drain output
NC	No internal connection	
DNU	Do not use. Inputs are in standby-equivalent mode, and outputs are driven low.	

 (2) Data outputs = Q2, Q3, Q5, Q6, Q8-Q25 when C0 = 0 and C1 = 0 Data outputs = Q2, Q3, Q5, Q6, Q8-Q14 when C0 = 0 and C1 = 1 Data outputs = Q1-Q6, Q8-Q10, Q12, Q13 when C0 = 1 and C1 = 1.

FUNCTION TABLE

	INPUTS							
RESET	DCS	CSR	CLK	CLK	Dn	Qn		
Н	L	Х	↑	\downarrow	L	L		
Н	L	Х	Ť	\downarrow	Н	Н		
Н	Х	L	↑	\downarrow	L	L		
Н	Х	L	↑	\downarrow	Н	н		
Н	н	н	↑	\downarrow	х	Q ₀		
Н	Х	Х	L or H	L or H	х	Q ₀		
L	X or Floating	L						

FUNCTION TABLE

	INPUTS					
RESET	CLK	CLK	DCKE, DCS, DODT	QCKE, QCS, QODT		
Н	1	\downarrow	Н	Н		
Н	↑	\downarrow	L	L		
н	L orH	L orH	Х	Q ₀		
L	X or Floating	X or Floating	X or Floating	L		

			INP	UTS			OL	ITPUTS	
RESET	RESET CLK CLK DCS CSR		Σ OF INPUTS = H D1-D25 ⁽¹⁾	PAR_IN ⁽²⁾	PPO	QERR ⁽³⁾			
Н	↑	\downarrow	L	Х	Even	L	L	Н	
Н	1	\downarrow	L	Х	Odd	L	н	L	
н	↑	\downarrow	L	Х	Even	Н	н	L	
н	↑	\downarrow	L	Х	Odd	Н	L	Н	
Н	1	\downarrow	Н	L	Even	L	L	Н	
Н	1	\downarrow	Н	L	Odd	L	н	L	
Н	1	\downarrow	Н	L	Even	Н	н	L	
Н	↑	\downarrow	Н	L	Odd	Н	L	Н	
Н	1	\downarrow	Н	Н	Х	Х	PPO ₀	QERR 0	
н	L or H	L or H	Х	Х	Х	Х	PPO ₀	QERR 0	
L	X or Floating	X or Floating	X or Floating	X or Floating	Х	X or Floating	L	Н	

PARITY AND STANDBY FUNCTION

Data inputs = D2-D3, D5-D6, D8-D25 when C0 = 0 and C1 = 0
 Data inputs = D2-D3, D5-D6, D8-D14 when C0 = 0 and C1 = 1

Data inputs = D1-D6, D8-D10, D12, D13 when C0 = 1 and C1 = 1

(2) PAR_IN arrives one clock cycle (C0 = 0) or two clock cycles (C0 = 1) after the data to which it applies.

(3) This transition assumes that QERR is high at the crossing of CLK going high and CLK going low. If QERR goes low, it stays latched low for a minimum of two clock cycles or until RESET is driven low. If two or more consecutive parity errors occur, the QERR output is driven low and latched low for a clock duration equal to the parity duration or until RESET is driven low.

1:2 REGISTER-A MODE 1:2 REGISTER-B MODE 1:1 MODE CASCADED MODE INPUT-DATA (C0 = 0, C1 = 0)(C0 = 0, C1 = 1)(C0 = 1, C1 = 1)(Registers A and B) ERROR PPO QERR PPO QERR PPO QERR PPO QERR OCCURANCE⁽²⁾ DURATION⁽³⁾ DURATION⁽³⁾ DURATION(3) DURATION(3) DURATION⁽³⁾ DURATION⁽³⁾ DURATION⁽³⁾ DURATION⁽³⁾ n – 4 1 Cycle 2 Cycles 1 Cycle 2 Cycles 1 Cycle 2 Cycles 1 Cycle 2 Cycles n – 3 1 Cycle 2 Cycles 1 Cycle 2 Cycles 1 Cycle 2 Cycles 1 Cycle 2 Cycles n – 2 1 Cycle 2 Cycles 1 Cycle 2 Cycles 1 Cycle 2 Cycles 1 Cycle 2 Cycles LPM + 2 LPM + 2 LPM + 1 LPM + 1 LPM + 2 LPM + 2 LPM + 2 LPM + 2 n – 1 Cycles Cycles Cycle Cycle Cycles Cycles Cycles Cycles n Not detected Not detected

PARITY ERROR DETECT IN LOW-POWER MODE⁽¹⁾

(1) If a parity error occurs before the device enters the low-power mode (LPM), the behavior of PPO and QERR is dependent on the mode of the device and the position of the parity error occurrence. This table illustrates the low-power-mode effect on parity detect. The low-power mode is activated on the n clock cycle when DCS and CSR go high.

(2) The clock-edge position of a one cycle data-input error relative to the clock-edge (n) which initiates LPM at the DCS and CSR inputs.
 (3) If an error occurs, then QERR output may be driven low and the PPO output driven high. These columns show the clock duration for which the PPO signal will be high.



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

			VALUE	UNIT	
V_{CC}	Supply voltage range		-0.5 to 2.5	V	
VI	Input voltage range ^{(2) (3)}		-0.5 to V _{CC} + 0.5	V	
Vo	Output voltage range ^{(2) (3)}	–0.5 to V _{CC} + 0.5	V		
I _{IK}	Input clamp current, $(V_I < 0 \text{ or } V_I > V_{CC})$	±50	mA		
I _{OK}	Output clamp current, ($V_O < 0$ or $V_O > V_{CC}$)		±50	mA	
lo	Continuous output current ($V_0 = 0$ to V_{CC}	±50	mA		
I _{CCC}	Continuous current through each V_{CC} or	GND	±100	mA	
		No airflow	39.8		
D	Thermal impedance,	Airflow 150 ft/min	34.1		
R_{\thetaJA}	Thermal impedance, junction-to-ambiant ⁽⁴⁾	Airflow 250 ft/min	33.6	K/W	
		Airflow 500 ft/min	32.5		
$R_{\theta JB}$	Thermal resistance, junction-to-board ⁽⁴⁾	No airflow	14.5	1	
T _{stg}	Storage temperature range		-65 to 150	°C	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This value is limited to 2.5 V maximum.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage		1.7		1.9	V	
V _{REF}	Reference voltage		$0.49 imes V_{CC}$	$0.5\times V_{CC}$	$0.51 \times V_{CC}$	V	
V _{TT}	Termination voltage	V _{REF} –40 mV	V _{REF}	V _{REF} + 40 mV	V		
VI	Input voltage	nput voltage			VCC	V	
VIH	AC high-level input voltage	Data inputs, CSR, PAR_IN	V _{REF} + 250 mV			V	
VIL	AC low-level input voltage	Data inputs, CSR, PAR_IN			V _{REF} –250 mV	V	
VIH	DC high-level input voltage	Data inputs, CSR, PAR_IN	V _{REF} + 125 mV			V	
VIL	DC low-level input voltage	Data inputs, CSR, PAR_IN			V _{REF} -125 mV	V	
VIH	High-level input voltage	RESET, C _n	$0.65 imes V_{CC}$			V	
VIL	Low-level input voltage	RESET, C _n			$0.35 \times V_{CC}$	V	
VICR	Common-mode input voltage range	CLK, <u>CLK</u>	0.675		1.125	V	
V _{I(PP)}	Peak-to-peak input voltage	CLK, CLK	600			mV	
I _{OH}	High-level output current	Q outputs, PPO			-8	mA	
		Q outputs, PPO			8		
I _{OL}	Low-level output current	QERR output	30			mA	
T _A	Operating free-air temperature		-40		85	°C	

(1) The RESET and Cn inputs of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless RESET is low. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT
		I _{OH} = -100 μA		1.7V to 1.9V	V _{CC} -0.2			V
V _{OH}	Q outputs, PPO	I _{OH} = -6 mA		1.7V	1.3			V
		I _{OL} = 100 μA		1.7V to 1.9V			0.2	
V _{OL}	Q outputs, PPO	I _{OL} = 6 mA		1.7V			0.4	V
	QERR output	I _{OL} = 25 mA		1.7V			0.5	ĺ
		V _I = GND					5	
I _I	PAR_IN	$V_{I} = V_{CC}$		1.9V			25	μA
	All other inputs ⁽²⁾	$V_{I} = V_{CC}$ or GND					±5	
l _{oz}	QERR output	$VO = V_{CC}$ or GND		1.9V			±10	μA
	Static standby	RESET = GND					200	μA
I _{CC}	Static operating	$\overline{\text{RESET}} = V_{CC}, V_I = V_{IH(AC)} \text{ or } I_O = C$ $V_{IL(AC)}$		1.9V			40	mA
	Dynamic operating – clock only	$\label{eq:response} \begin{array}{l} \hline \textbf{RESET} = V_{CC}, \ V_l = V_{IH(AC)} \ or \\ V_{IL(AC)}, \ \textbf{CLK} \ \textbf{and} \ \textbf{CLK} \ \textbf{switching} \\ \hline \textbf{50\%} \ \textbf{duty} \ \textbf{cycle} \end{array}$	I _O = 0			45		μA/MH:
I _{CCD}	Dynamic operating – per each data input, 1:1 configuration	$\overline{\text{RESET}} = V_{CC}, V_{I} = V_{IH(AC)} \text{ or } V_{IL(AC)}, CLK \text{ and } CLK \text{ switching}$		1.8V		43		μA cloc MHz/
	Dynamic operating – per each data input, 1:2 configuration	50% duty cycle, one data input switching at one-half clock frequency, 50% duty cycle				60		D input
	Chip-select-enabled low-power active mode – clock only	$\label{eq:RESET} \begin{array}{l} \overline{\text{RESET}} = V_{CC}, \ V_{I} = V_{IH(AC)} \ \text{or} \\ V_{IL(AC)}, \ CLK \ \text{and} \ \overline{\text{CLK}} \ \text{switching} \\ 50\% \ \text{duty} \ \text{cycle} \end{array}$				45		μA/MH:
I _{CCDLP}	Chip-select-enabled low-power active mode - 1:1 configuration	$\overline{\text{RESET}} = V_{CC}, V_{I} = V_{IH(AC)} \text{ or } V_{IL(AC)}, CLK \text{ and } CLK \text{ switching } 50\% \text{ duty cycle, one data input } $	I _O = 0	1.8V		2		μA clock MHz/
	Chip-select-enabled low-power active mode – 1:2 configuration	switching at one-half clock frequency, 50% duty cycle				3		D input
	Data inputs, CSR, PAR_IN	$V_{I} = V_{REF} \pm 250 \text{ mV}$			2.5	3	3.5	-
Ci	CLK, CLK	$V_{ICR} = 0.9 \text{ V}, V_{I(PP)} = 600 \text{ mV}$		1.8V	2		3	
	RESET	$V_{I} = V_{CC}$ or GND				4		

(1) All typical values are at V_{CC} = 1.8 V, T_A = 25°C. (2) Each V_{REF} pin (A3 or T3) should be tested independently, with the other (untested) pin open.



TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2 and ⁽¹⁾

			V _{CC} = 1.8 V	± 0.1 V	UNIT
			MIN	MAX	UNIT
fclock	Clock freque	ency		410	MHz
tw	Pulse durati	on, CLK, CLK high or low	1		ns
tact	Differential i	nputs active time ⁽²⁾		10	ns
tinact	Differential i	nputs inactive time ⁽³⁾		15	ns
		$\overline{\text{DCS}}$ before $\text{CLK}\uparrow$, $\overline{\text{CLK}}\downarrow$, $\overline{\text{CSR}}$ high; $\overline{\text{CSR}}$ before $\text{CLK}\uparrow$, $\overline{\text{CLK}}\downarrow$, $\overline{\text{DCS}}$ high	600		
	Cotup time	DCS before CLK↑, CLK↓, CSR low	500		
t _{su}	Setup time	DODT, DCKE, and Data before $CLK\uparrow$, $\overline{CLK}\downarrow$	500		ps
		PAR_IN before CLK↑, CLK↓	500		
t _h	Hold time	DCS, DODT, DCKE, and Data after $CLK\uparrow$, $\overline{CLK}\downarrow$	400		20
		PAR_IN after CLK↑, CLK↓	400		ps

(1) All inputs slew rate is 1 V/ns \pm 20%.

(2)

 V_{REF} must be held at a valid input level, and data inputs must be held low for a minimum time of t_{act} max, after RESET is taken high. V_{REF} , data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max, after RESET is taken low. (3)

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		FROM	то	V _{CC} = 1.8 V ±	0.1 V		
	PARAMETER	(INPUT)	(OUTPUT)	MIN MA		UNIT	
f _{max}	See Figure 2			410		MHz	
t _{pdm}	Production test, See Figure 1	CLK and CLK	Q	0.4	0.7	ns	
t _{pd}	See Figure 5	CLK and CLK	PPO	0.6	1.6	ns	
t _{PLH}	See Firme 4	CLK and CLK	QERR	1.2	2.4		
t _{PHL}	See Figure 4		QERR	1	2.0	ns	
t _{RPHL} ⁽¹⁾	See Figure 2	RESET	Q		3		
t _{RPHL}	See Figure 5	RESEI	PPO		3	ns	
t _{RPLH}	See Figure 5	RESET	QERR		3	ns	

(1) Includes 350-ps test-load transmission-line delay.

OUTPUT SLEW RATES

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	то	V _{CC} = 1.8 V :	UNIT	
FARAMETER	FROM	10	MIN	MAX	UNIT
dV/dt_r	20%	80%	1	4	V/ns
dV/dt_f	80%	20%	1	4	V/ns
$dV/dt_{\Delta}^{(1)}$	20% or 80%	80% or 20%		1	V/ns

(1) Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).



PARAMETER MEASUREMENT INFORMATION

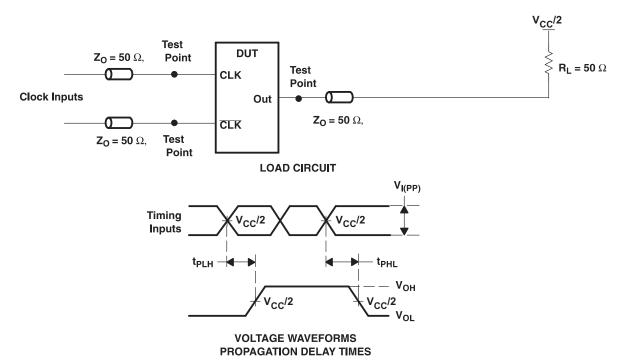


Figure 1. Output Load For Production Test

PROPAGATION DELAY (Design Goal as per JEDEC Specification)

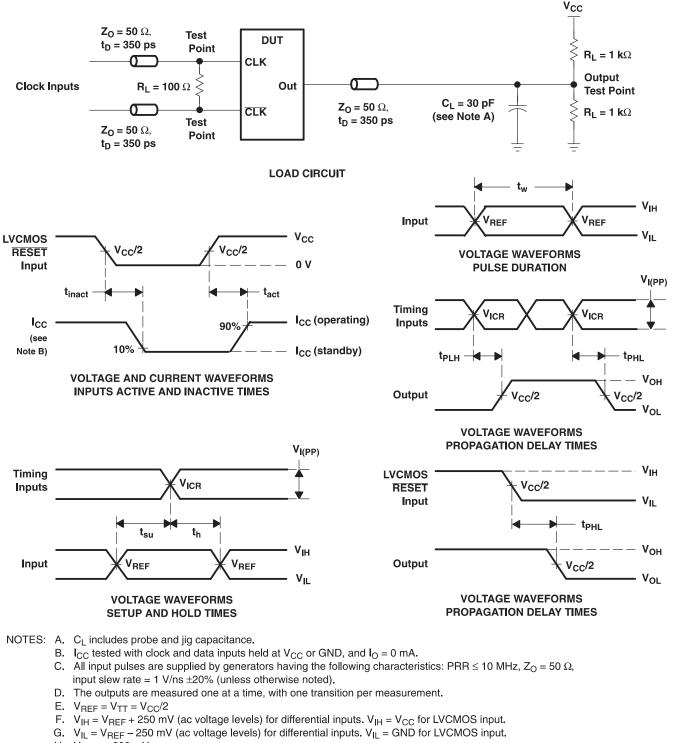
PARAMETER	FROM	то	V _{CC} = 1.8 V :	UNIT	
FARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	UNIT
t _{pdm} ⁽¹⁾	CLK and CLK	Q	1.1	1.5	ns
t _{pdmss} ⁽¹⁾	CLK and CLK	Q		1.6	ns

(1) Includes 350 psi test-load transmission delay line

74SSTUB32866A

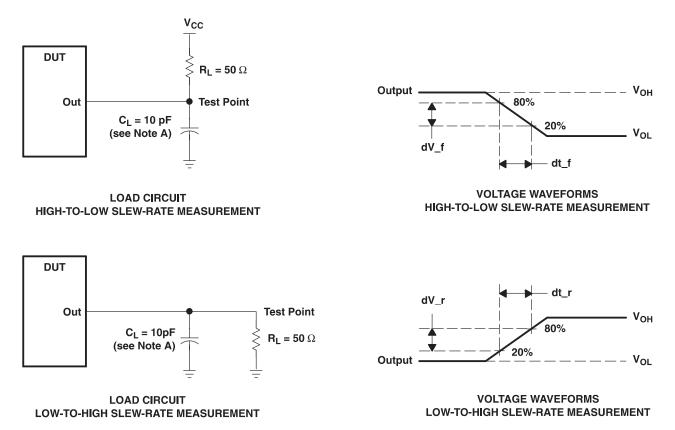
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- H. $V_{I(PP)} = 600 \text{ mV}$
- I. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Data Output Load Circuit and Voltage Waveforms



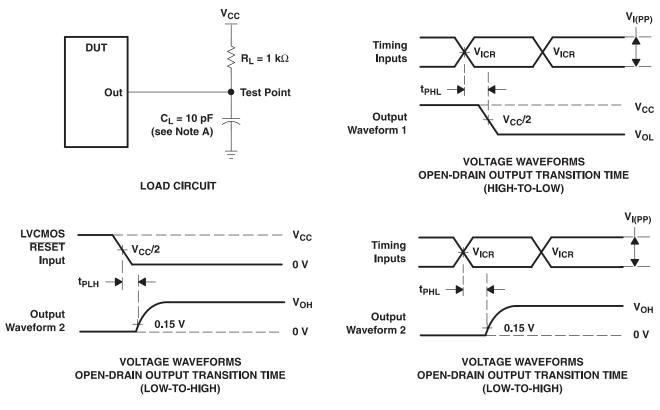
NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , input slew rate = 1 V/ns \pm 20% (unless otherwise specified).

Figure 3. Data Output Slew-Rate Measurement Information

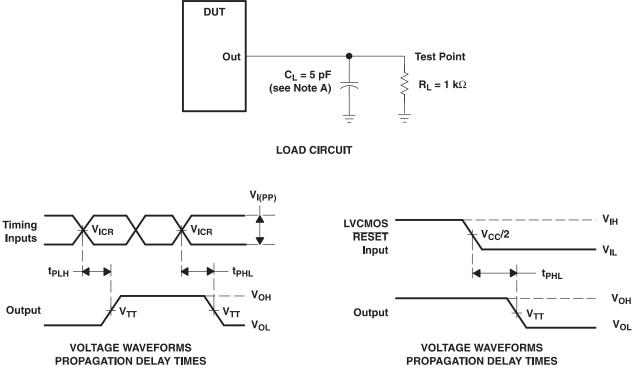
74SSTUB32866A

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- NOTES: A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , input slew rate = 1 V/ns ±20% (unless otherwise noted).
 - C. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 4. Error Output Load Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , input slew rate = 1 V/ns ±20% (unless otherwise noted).
- C. $V_{\text{REF}} = V_{\text{TT}} = V_{\text{CC}}/2$
- D. $V_{IH} = V_{REF} + 250 \text{ mV}$ (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
- E. $V_{IL} = V_{REF} 250 \text{ mV}$ (ac voltage levels) for differential inputs. $V_{IL} = GND$ for LVCMOS input.
- F. $V_{I(PP)} = 600 \text{ mV}$
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 5. Partial-Parity-Out Load Circuit and Voltage Waveforms



APPLICATION INFORMATION

The typical values below are for standard raw cards. Test equipment used was the JEDEC register validation board using pattern 0x43, 0x4F, and 0x5A.

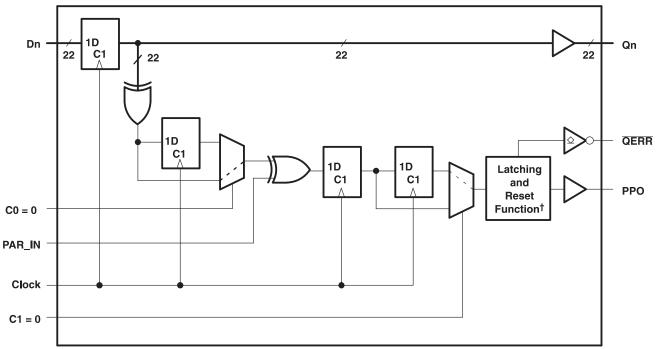
RAW CARD	t _{pd}	OVERSHOOT	
	MIN	MAX	
A/F (@800 MBit/s)	1.0 ns	1.5 ns	590 mV
B/G (@800 MBit/s)	1.2 ns	1.9 ns	590 mV
C/H (@800 MBit/s)	1.2 ns	1.9 ns	730 mV
J (@667 MBit/s)	1.3 ns	2.0 ns	340 mV

Table 1. Raw Card Values (1) (2)

(1) All values are valid under nominal conditions and minimum/maximum of typical signals on one typical DIMM.

(2) Measurements include all jitter and ISI effects.

74SSTUB32866A Used as a Single Device in the 1:1 Register Configuration; C0 = 0, C1 = 0

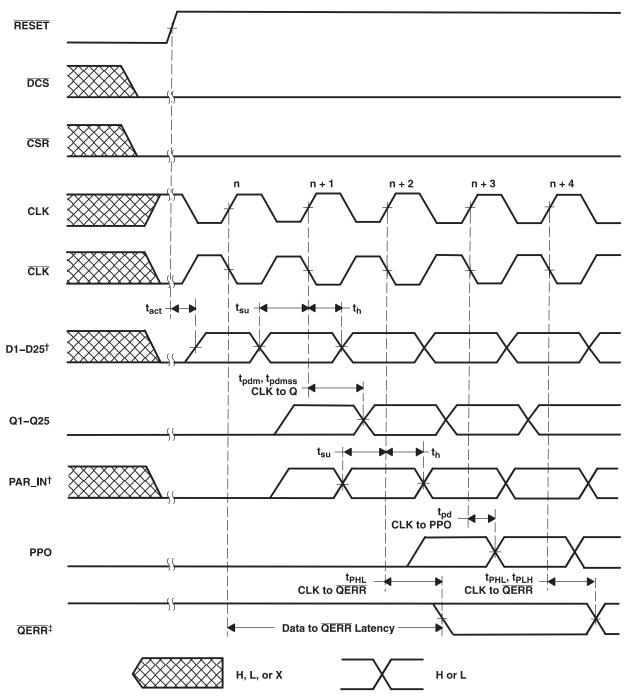


Register 1 of 1

[†] This function holds the error for two cycles. For details, see the parity logic diagram.



Timing Diagram for 74SSTUB32866A Used as a Single Device; C0 = 0, C1 = 0 (RESET Switches From L to H)

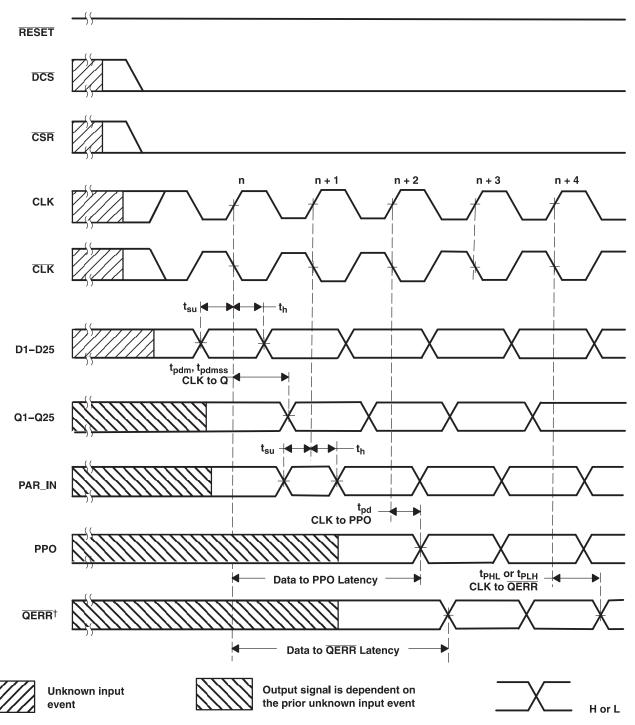


[†] After RESET is switched from low to high, all data and PAR_IN input signals must be set and held low for a minimum time of t_{act} max, to avoid false error.

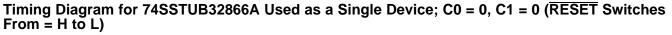
+If the data is clocked in on the n clock pulse, the QERR output signal will be generated on the n + 2 clock pulse, and it will be valid on the n + 3 clock pulse.

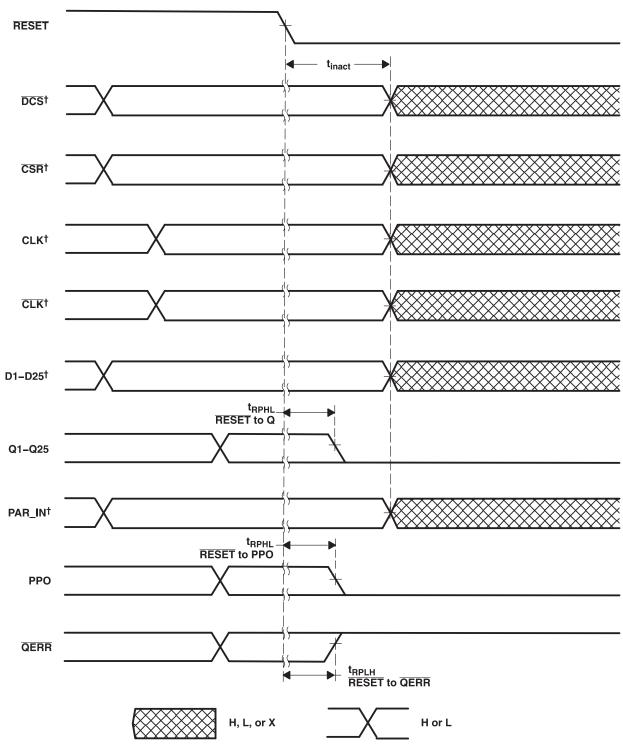


Timing Diagram for 74SSTUB32866A Used as a Single Device; C0 = 0, C1 = 0 (RESET = H)



⁺ If the data is clocked in on the n clock pulse, the QERR output signal will be generated on the n + 2 clock pulse, and it will be valid on n + 3 clock pulse. If an error occurs and the QERR output is driven low, it stays latched low for a minimum of two clock cycles or until RESET is driven low.



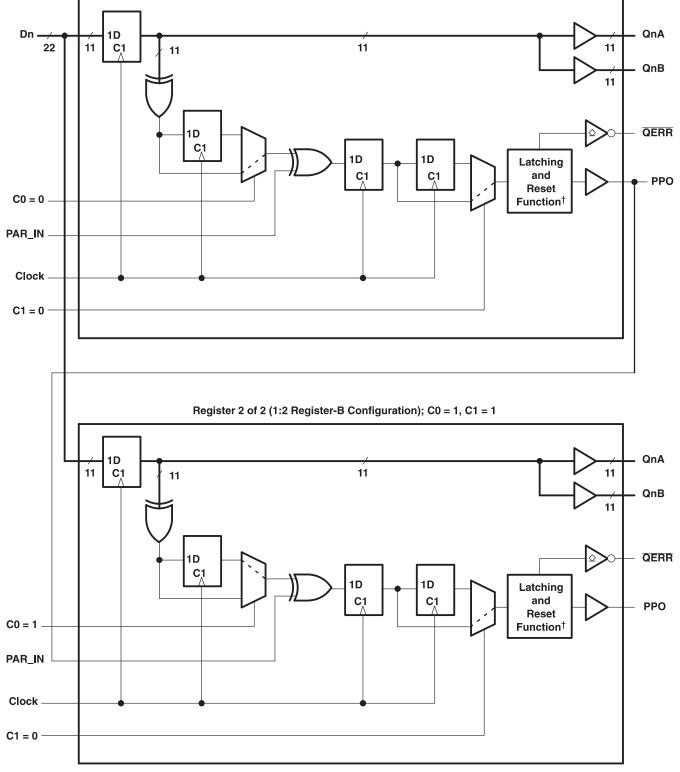


[†] After RESET is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of tinact max.



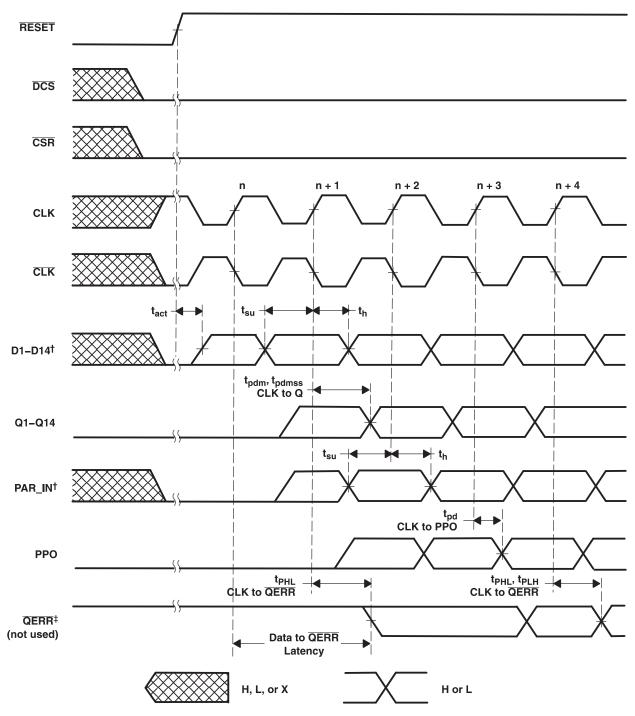
74SSTUB32866A Used in Pair in the 1:2 Register Configuration





[†] This function holds the error for two cycles. For details, see the parity logic diagram.

Timing Diagram for the First 74SSTUB32866A (1:2 Register-A Configuration) Device Used in Pair; C0 = 0, C1 = 1 (RESET Switches From L to H)

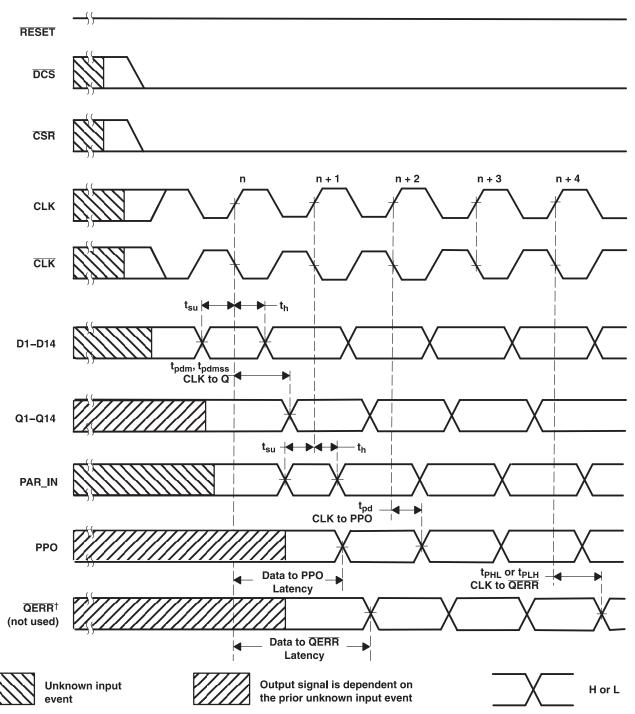


[†] After RESET is switched from low to high, all data and PAR_IN input signals must be set and held low for a minimum time of t_{act} max, to avoid false error.

[‡]If the data is clocked in on the n clock pulse, the QERR output signal will be generated on the n + 1 clock pulse, and it will be valid on the n + 2 clock pulse.

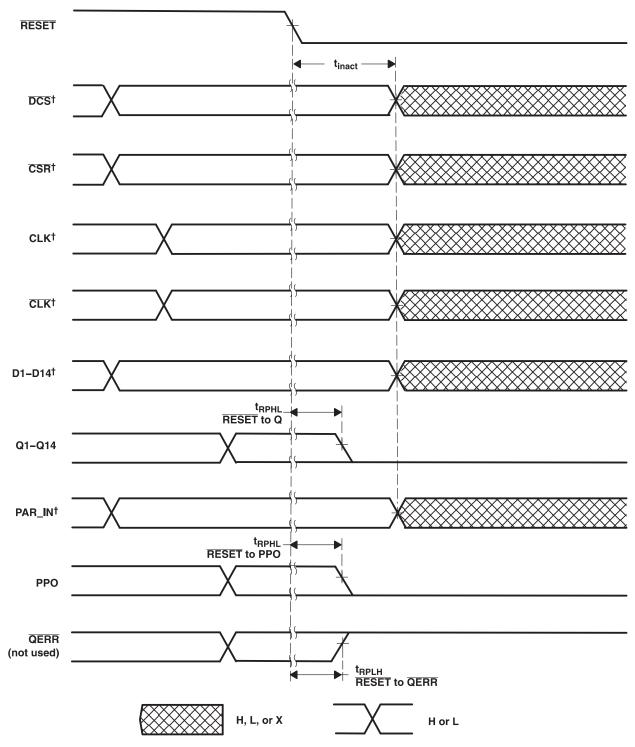


Timing Diagram for the First 74SSTUB32866A (1:2 Register-A Configuration) Device Used in Pair; C0 = 0, C1 = 1 (RESET = H)



[†] If the data is clocked in on the n clock pulse, the QERR output signal will be generated on the n + 1 clock pulse, and it will be valid on n + 2 clock pulse. If an error occurs and the QERR output is driven low, it stays latched low for a minimum of two clock cycles or until RESET is driven low.

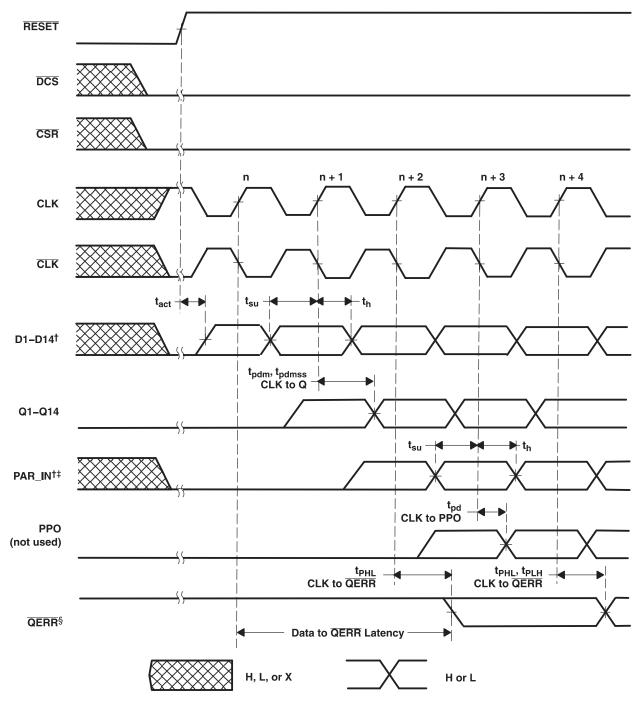
Timing Diagram for the First 74SSTUB32866A (1:2 Register-A Configuration) Device Used in Pair; C0 = 0, C1 = 1 (RESET = Switches From H to L)



⁺ After RESET is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of t_{inact} max.



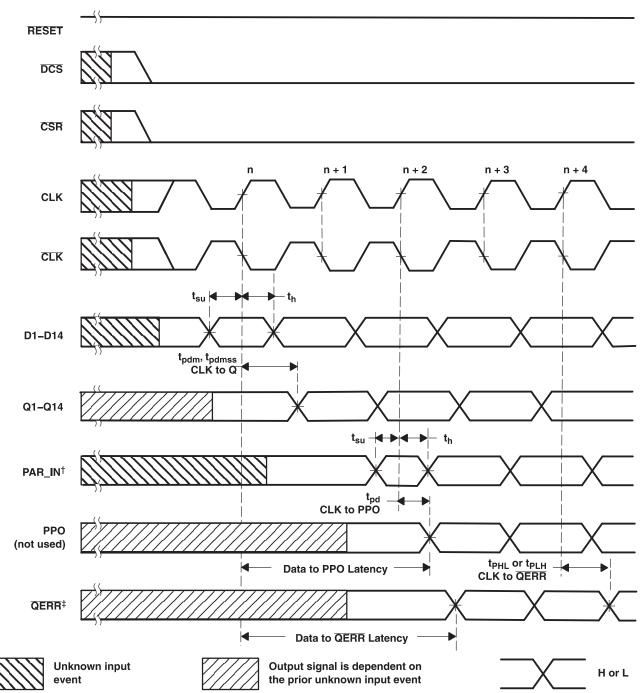
Timing Diagram for the Second 74SSTUB32866A (1:2 Register-B Configuration) Device Used in Pair; C0 = 1, C1 = 1 (RESET = Switches From L to H)



[†] After RESET is switched from low to high, all data and PAR_IN input signals must be set and held low for a minimum time of t_{act} max, to avoid false error.

[‡]PAR_IN is driven from PPO of the first SN74SSTUB32866 device.

§ If the data is clocked in on the n clock pulse, the QERR output signal will be generated on the n + 2 clock pulse, and it will be valid on the n + 3 clock pulse.

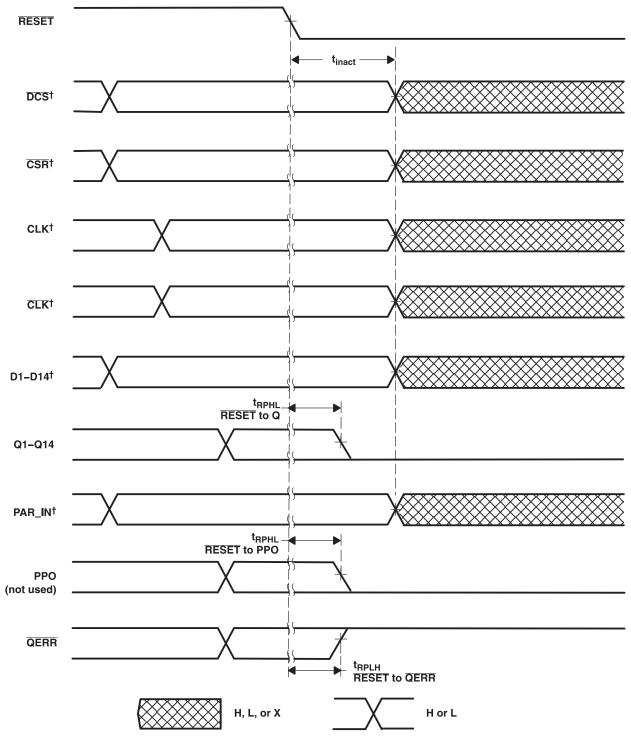


Timing Diagram for the Second 74SSTUB32866A (1:2 Register-B Configuration) Device Used in Pair; C0 = 1, C1 = 1 (RESET = H)

[†] PAR_IN is driven from PPO of the first SN74SSTUB32866 device.

[‡]If the data is clocked in on the n clock pulse, the QERR output signal will be generated on the n + 2 clock pulse, and it will be valid on n + 3 clock pulse. If an error occurs and the QERR output is driven low, it stays latched low for a minimum of two clock cycles or until RESET is driven low.

Timing Diagram for the Second 74SSTUB32866A (1:2 Register-B Configuration) Device Used in Pair; C0 = 1, C1 = 1 (RESET = Switches From H to L)



[†] After RESET is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of t_{inact} max.



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74SSTUB32866AZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TEXAS INSTRUMENTS





TAPE AND REEL INFORMATION

TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Busies	Dealers	Dealers	Disc	000	
*All dimensions are nominal					

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74SSTUB32866AZKER	LFBGA	ZKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

16-Feb-2012



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74SSTUB32866AZKER	LFBGA	ZKE	96	1000	336.6	336.6	31.8

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Falls within JEDEC MO-205 variation CC.

D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).



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