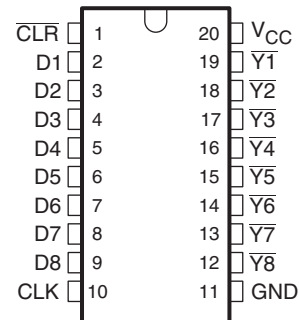


8-BIT OPEN-COLLECTOR SINK DRIVER WITH LATCH

FEATURES

- LBC3S (Lin BiCMOS) Process
- High Voltage Output ($V_{OUT} = 24\text{ V}$)
- Output Current ($I_{OL\text{ Max}} = 40\text{ mA}$)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
 - 2000-V Human Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged Device Model (C101)

**N OR PW PACKAGE
(TOP VIEW)**



DESCRIPTION

The TLC59212 is an 8-bit open-collector driver with latch designed for 5-V V_{CC} operation.

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{\text{CLR}}$) input. Information at the data (D) input meeting the setup time requirements is transferred to the $\overline{\text{Y}}$ output on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D-input has no effect at the output.

The TLC59212 is characterized for operation from -40°C to 85°C .

ORDERING INFORMATION⁽¹⁾

| T_A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 85°C | PDIP – N | Reel of 1000 | TLC59212IN | Y59212 |
| | TSSOP – PW | Reel of 2000 | TLC59212IPWR | Y59212 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE (EACH LATCH)⁽¹⁾

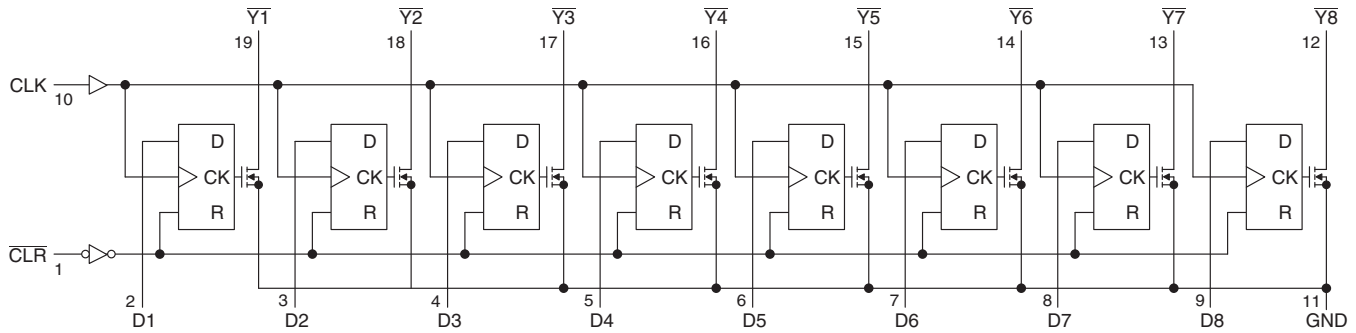
| INPUTS | | | OUTPUT Y |
|-------------------------|-----|---|-------------|
| $\overline{\text{CLR}}$ | CLK | D | |
| L | X | X | H* |
| H | ↑ | L | H* |
| H | ↑ | H | L |
| H | L | X | Y_0 |
| H | ↓ | X | Y_0 |

- (1) L: Low-level
 H: High-level
 H*: with pullup resistor
 X: Irrelevant
 ↑: Rising edge
 ↓: Falling edge
 Z: High-impedance (OFF)



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LOGIC SYMBOL⁽¹⁾



(1) This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|--|---------------------------------|-----|---------|
| V _{CC} | Supply voltage range | -0.5 | 7 | V |
| D | Input voltage range | D, CLK, $\overline{\text{CLR}}$ | | V |
| V _O | Output voltage range | H output | | V |
| I _O | Output current range | 1 bit for output low | | 40 mA |
| I _{IK} | Input clamp current | V _I < 0 V | | -20 mA |
| θ _{JA} | Package thermal impedance ⁽²⁾ | N package | | 69 °C/W |
| | | PW package | | 83 °C/W |
| T _A | Operating free-air temperature range | -40 | 85 | °C |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

V_{CC} = 4.5 V to 5.5 V

| | CONDITIONS | MIN | MAX | UNIT |
|-----------------|--------------------------------|-----------------------|-----------------------|-------|
| V _{CC} | Supply voltage | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} × 0.7 | V _{CC} | V |
| V _{IL} | Low-level input voltage | 0 | V _{CC} × 0.3 | V |
| V _O | Output voltage | 0 | 24 | V |
| I _O | Output current | Duty cycle < 100% | | 40 mA |
| T _A | Operating free-air temperature | -40 | 85 | °C |

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---------------------|--------------------------------|---|------------------|------|------|---------------|---------------|
| V_{t+} | Positive-going input threshold | D, $\overline{\text{CLR}}$, CLK | | | 3.5 | V | |
| V_{t-} | Negative-going input threshold | D, $\overline{\text{CLR}}$, CLK | 1.5 | | | V | |
| V_t | Hysteresis | D, $\overline{\text{CLR}}$, CLK | 0.5 | | 2 | V | |
| $V_{O(\text{off})}$ | Output tr sustain voltage | $I_{ce} = 1 \text{ mA}$ | 24 | | | V | |
| I_{OZ} | Output tr leakage current | $V_O = 24 \text{ V}$ | | 0 | 5 | μA | |
| I_{IH} | High-level input current | $V_{CC} = 5.5 \text{ V}$, $V_I = 5.5 \text{ V}$ | | 0 | 1 | μA | |
| I_{IL} | Low-level input current | $V_{CC} = 5.5 \text{ V}$, $V_I = 0 \text{ V}$ | | 0 | -1 | μA | |
| I_{off} | Leakage current | $V_I = 0 \text{ to } 5 \text{ V}$, $V_O = 0 \text{ to } 30 \text{ V}$, $V_{CC} = 0$ | | 0 | 5 | μA | |
| I_{CC} | Supply current | $V_I = 0 \text{ to } 5 \text{ V}$, $V_O = 0 \text{ to } 30 \text{ V}$, $V_{CC} = 0$ | Output = all OFF | | 0 | 5 | μA |
| | | | Output = all ON | | 8 | 20 | |
| V_{OL} | Low-level output voltage | $V_{CC} = 4.5 \text{ V}$, $I_O = 40 \text{ mA}$ | | 0.32 | 0.55 | V | |
| r_{ON} | ON-state resistance | $V_{CC} = 4.5 \text{ V}$, $I_O = 10 \text{ mA}$ | | 8 | 13 | Ω | |
| C_i | Input capacitance | $V_I = V_{CC} \text{ or GND}$ | | 5 | | pF | |

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted), see [Figure 1](#)

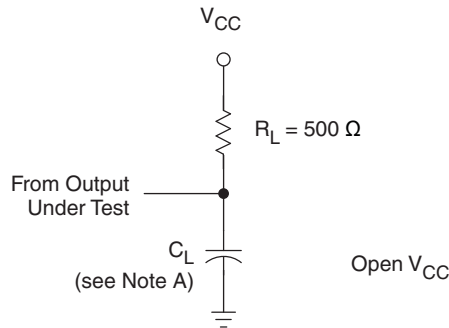
| PARAMETER | TEST CONDITIONS | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ | | UNIT |
|------------|---|--|--------------------------|-----|-----|--|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| t_{TLH} | Output = low to high | $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$ | | 60 | 185 | | 185 | ns |
| t_{THL} | Output = high to low | $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$ | | 10 | 185 | | 185 | ns |
| t_{PLH} | Output = low to high | $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$ | | 70 | 210 | | 250 | ns |
| t_{PHL} | Output = high to low | $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$ | | 45 | 210 | | 250 | ns |
| t_{PHLR} | $\overline{\text{CLR}}-\overline{\text{Y}}$ | $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$ | | 70 | 210 | | 250 | ns |

TIMING REQUIREMENTS

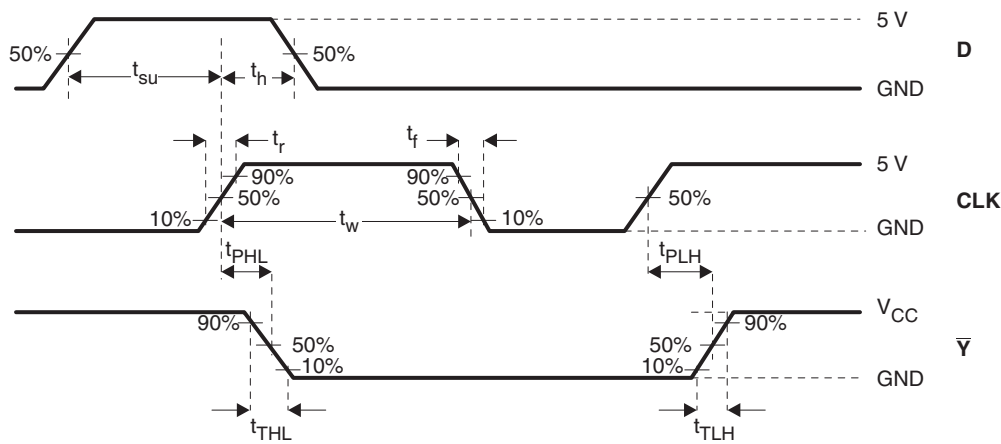
over recommended operating free-air temperature range, $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, O/C to Y (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ | | UNIT |
|-----------|-------------|------------------------------|--|-----|------|
| | | | MIN | MAX | |
| t_{su} | Setup time | CLK | $V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$ | | ns |
| t_h | Hold time | CLK | $V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$ | | ns |
| t_w | Pulse width | CLK, $\overline{\text{CLR}}$ | $V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$ | | ns |

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUT



VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, and $t_f \leq 3 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TLC59212IN | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC59212IPWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC59212IPWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

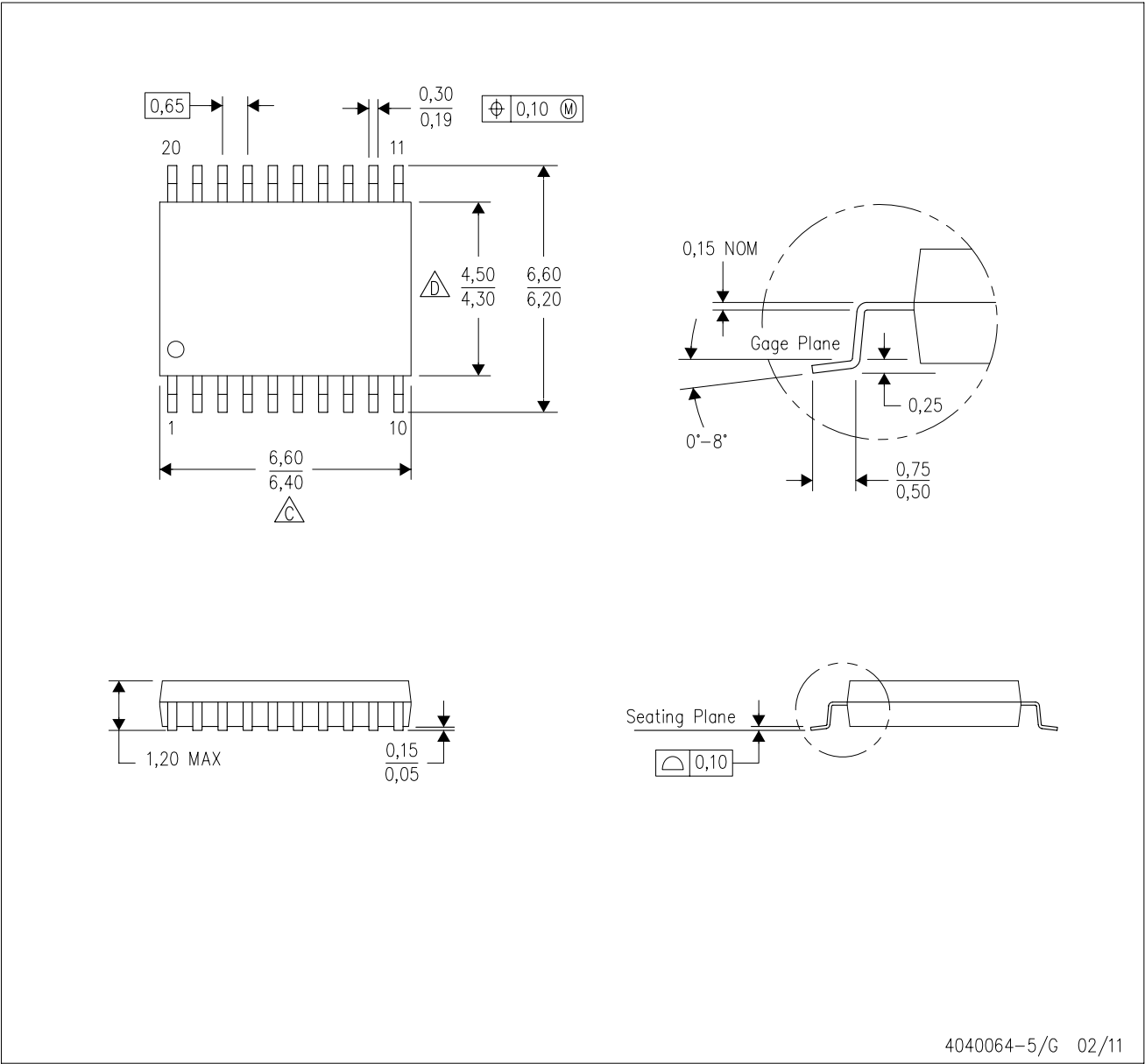


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLC59212IPWR | TSSOP | PW | 20 | 2000 | 346.0 | 346.0 | 33.0 |

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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