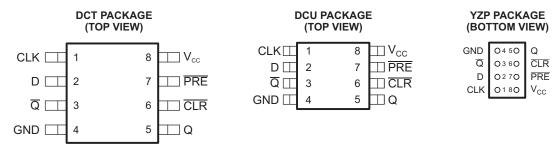
SCES203M-APRIL 1999-REVISED FEBRUARY 2007

FEATURES

- Available in the Texas Instruments
 NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{nd} of 5.9 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C

- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V V_{CC} operation.

NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC2G74YZPR	CP_
-40°C to 85°C	SSOP - DCT	Reel of 3000	SN74LVC2G74DCTR	C74
	Vecop pell	Reel of 3000	SN74LVC2G74DCUR	C74
	VSSOP – DCU	Reel of 250	SN74LVC2G74DCUT	C74_

- Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site. DCU: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

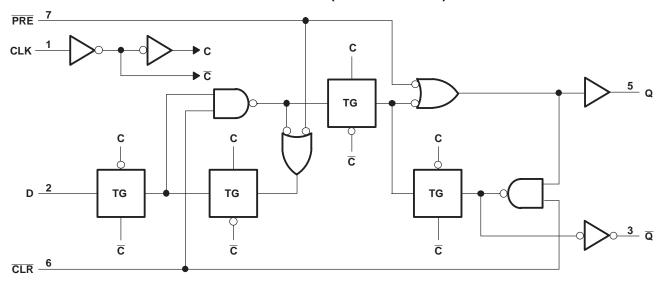


FUNCTION TABLE

	INP	OUTI	PUTS		
PRE	CLR	CLK	D	Q	Q
L	Н	X	X	Н	L
Н	L	X	X	L	Н
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
Н	Н	\uparrow	Н	Н	L
Н	Н	\uparrow	L	L	Н
Н	Н	L	X	Q_0	\overline{Q}_{0}

(1) This configuration is nonstable; that is, it does not persist when $\overline{\mathsf{PRE}}$ or $\overline{\mathsf{CLR}}$ returns to its inactive (high) level.

LOGIC DIAGRAM (POSITIVE LOGIC)





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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range ⁽²⁾		-0.5	6.5	V
Vo	Voltage range applied to any output in the	-0.5	6.5	V	
Vo	Voltage range applied to any output in the	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current V _O < 0			-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND)		±100	mA
		DCT package		220	
θ_{JA}	Package thermal impedance (4)	DCU package		227	°C/W
		YZP package		102	
T _{stg}	Storage temperature range	·	-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.





Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT		
.,	Complements	Operating	1.65	5.5	V		
V_{CC}	Supply voltage	Data retention only	1.5		V		
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	$0.65 \times V_{CC}$			
\/	High lovel input veltage	V_{CC} = 2.3 V to 2.7 V	1.7		V		
V_{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V					
		V _{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$				
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$			
\/	Low level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V		
V_{IL}	Low-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$		0.8	V		
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$			
VI	Input voltage		0	5.5	V		
Vo	Output voltage		0	V _{CC}	V		
		V _{CC} = 1.65 V		-4			
		V _{CC} = 2.3 V		-8			
I_{OH}	High-level output current	V _{CC} = 3 V		-16	mA		
		V _{CC} = 3 V		-24			
		V _{CC} = 4.5 V		-32			
		V _{CC} = 1.65 V		4			
		V _{CC} = 2.3 V		8			
I_{OL}	Low-level output current	V _{CC} = 3 V		16	mA		
		V _{CC} = 3 V		24			
		V _{CC} = 4.5 V		32			
		V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20			
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		ns/V			
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$					
T _A	Operating free-air temperature		-40	85	°C		

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

Р	ARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP(1)	MAX	UNIT
		$I_{OH} = -100 \mu\text{A}$	1.65 V to 5.5 V	V _{CC} - 0.1		
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		
\/		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		V
V _{OH}		$I_{OH} = -16 \text{ mA}$	3 V	2.4		V
		$I_{OH} = -24 \text{ mA}$	3 V	2.3		
		$I_{OH} = -32 \text{ mA}$	4.5 V	3.8		
		$I_{OL} = 100 \mu A$	1.65 V to 5.5 V		0.1	
		I _{OL} = 4 mA	1.65 V		0.45	
V _{OL}	V	I _{OL} = 8 mA	2.3 V		0.3	V
V OL		I _{OL} = 16 mA	3 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
		I _{OL} = 32 mA	4.5 V		0.55	
I	Data or control inputs	V _I = 5.5 V or GND	0 to 5.5 V		±5	μΑ
$I_{\rm off}$		V_I or $V_O = 5.5 \text{ V}$	0		±10	μΑ
I_{CC}	·	$V_1 = 5.5 \text{ V or GND}, \qquad I_0 = 0$	1.65 V to 5.5 V		10	μΑ
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V		500	μΑ
C_{i}		$V_I = V_{CC}$ or GND	3.3 V	5		pF

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V _{CC} = ± 0.1		V _{CC} = ± 0.2		V _{CC} = ± 0.3		V _{CC} = ± 0.5	5 V 5 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}				80		175	·	175		200	MHz
Dula duratia	CLK	6.2		2.7		2.7		2		20	
t _w	Pulse duration	PRE or CLR low	6.2		2.7		2.7		2		ns
	0-1	Data	2.9		1.7		1.3		1.1		
t _{su} Setup time, before CLK↑	PRE or CLR inactive	1.9		1.4		1.2		1		ns	
t _h	Hold time, data after CLK↑		0		0.3		1.2		0.5		ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			,			, ,	•	,			
PARAMETER FROM		TO (OUTBUT)	V _{CC} = ± 0.1	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			80		175		175		200		MHz
	CLK	Q	4.8	13.4	2.2	7.1	2.2	5.9	1.4	4.1	
t _{pd}	CLK	Q	6	14.4	3	7.7	2.6	6.2	1.6	4.4	ns
	PRE or CLR	Q or Q	4.4	12.9	2.3	7	1.7	5.9	1.6	4.1	



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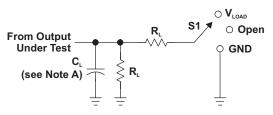
Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
	FANAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNII
C_{pd}	Power dissipation capacitance	f = 10 MHz	35	35	37	40	pF

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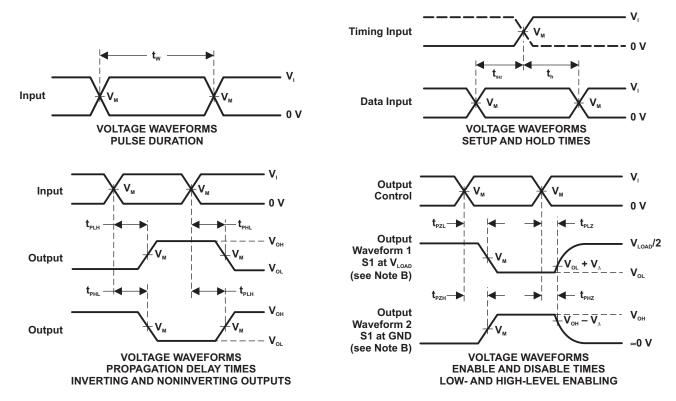
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t_{PLZ}/t_{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

	INF	PUTS	V	V		Б	V
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _L	R _L	V _Δ
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V
2.5 V ± 0.2 V	V_{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_o = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and \dot{t}_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





5-Mar-2012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LVC2G74DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC2G74DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC2G74DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC2G74DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
SN74LVC2G74DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC2G74DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC2G74DCUT	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC2G74DCUTE4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC2G74DCUTG4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC2G74YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

5-Mar-2012

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL. Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC2G74:

Automotive: SN74LVC2G74-Q1

■ Enhanced Product: SN74LVC2G74-EP

NOTE: Qualified Version Definitions:

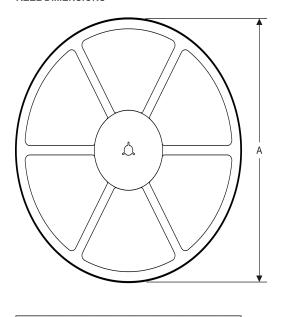
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

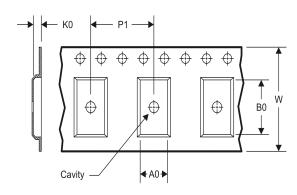
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G74DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74DCUR	US8	DCU	8	3000	180.0	9.0	2.05	3.3	1.0	4.0	8.0	Q3
SN74LVC2G74YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
SN74LVC2G74YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G74DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G74DCUR	US8	DCU	8	3000	182.0	182.0	20.0
SN74LVC2G74YZPR	DSBGA	YZP	8	3000	220.0	220.0	34.0
SN74LVC2G74YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES:

- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.



DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



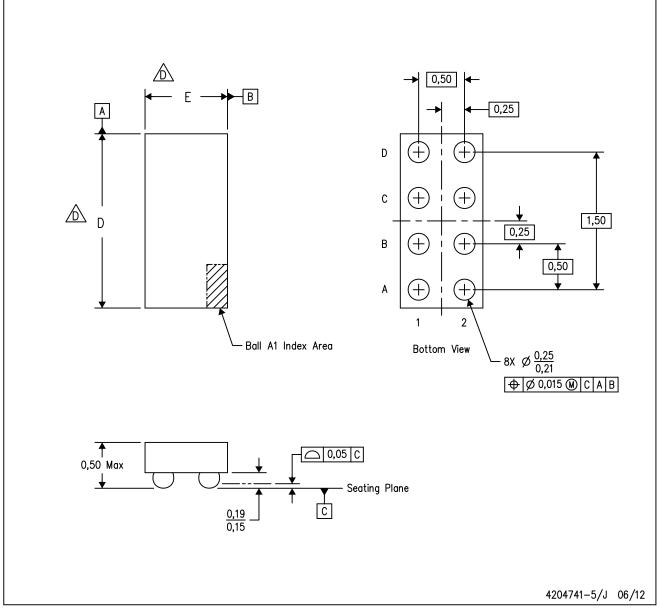
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- This drawing is subject to change without notice.
- Ç. NanoFree™ package configuration.
- ⚠ The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative. E. This package is a Pb-free solder ball design. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.



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