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13 DQB1

GND [] 12

DW OR NT PACKAGE 3-State Buffer-Type Outputs Drive Bus (TOP VIEW) **Lines Directly** Each Register File Has Individual 24 🛮 V_{CC} S₀ **Write-Enable Controls and Address Lines** 1A0 **[**]2 23 S1 **Designed Specifically for Multibus** 1A1 🛮 3 22**∏** 2A3 **Architecture and Overlapping File** 1A2 **∏**4 21 T 2A2 **Operations** 20 2A1 1A3 🛮 5 Prioritized B-Input Port Prevents Write 1₩ **[**]6 19**∏** 2A0 **Conflicts During Dual-Input Mode** 18 2W S2 Π_7 DQA1 []8 17 S3 Package Options Include Plastic DQA2 Π_9 16 **∏** DQB4 Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs DQA3 110 15 DQB3 DQA4 [] 11 14 DQB2

This device features two 16-word by 4-bit register files. Each register file has individual write-enable

description

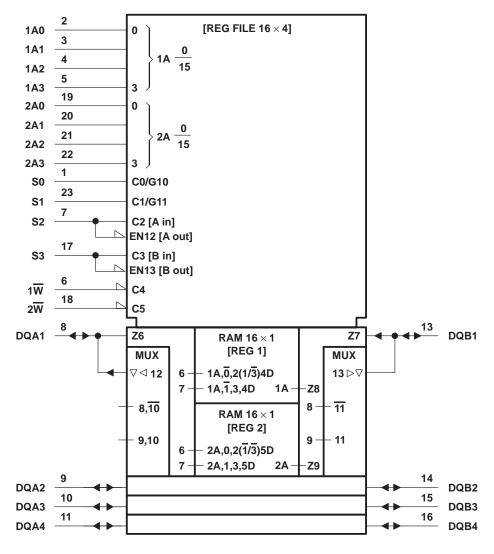
 $(1\overline{W},2\overline{W})$ controls and address lines. This device has two 4-bit data I/O ports (DQA1–DQA4 and DQB1–DQB4). The data I/O ports can output to bus A and bus B, receive input from bus A and bus B, receive input from bus A and output to bus B, or output to bus A and receive input from bus B. To prevent writing conflicts in the dual-input mode, the B-input port takes priority. Two select (S0 and S1) lines control which port has access to which register. S2 determines whether the A ports are in the input or the output modes and S3 does likewise for the B ports. The address lines (1A0–1A3 or 2A0–2A3) are decoded by an internal 1-of-16 decoder to select which register word is to be accessed. All outputs are 3-state buffer-type outputs designed specifically to drive bus lines directly.

The SN74ALS870 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

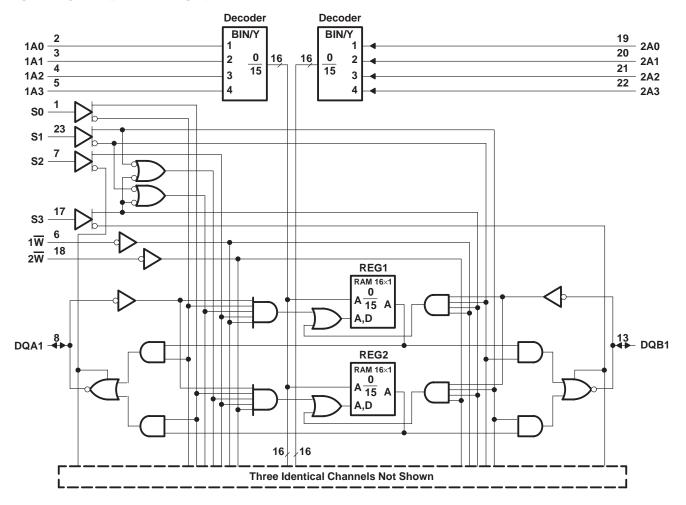
	FILI	ESELECT	INPUT/OUTPUT				
S0	S1	FILE SEL	S2 S3		I/O SEL		
L	L	1R to A, 1R to B					
Н	L	2R to A, 1R to B	Ι,	L	A out, B out		
L	Н	1R to A, 2R to B	-		A out, B out		
Н	Н	2R to A, 2R to B					
L	L	A to 1R, 1R to B					
Н	L	A to 2R, 1R to B	Н		A in, B out		
L	Н	A to 1R, 2R to B	''	L	A III, D Out		
Н	Н	A to 2R, 2R to B					
L	L	1R to A, B to 1R					
Н	L	2R to A, B to 1R	١,	Н	A out, B in		
L	Н	1R to A, B to 2R	-	''	A out, B III		
Н	Н	2R to A, B to 2R					
L	L	B to 1R					
Н	L	A to 2R, B to 1R	Н	н	A in, B in		
L	Н	A to 1R, B to 2R	''	''	A III, D III		
Н	Н	B to 2R					

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}	7 V
Input voltage, V _I : All inputs	$\dots \dots \dots \ 7 \ V$
I/O ports	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T _A	0°C to 70°C
Storage temperature range	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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recommended operating conditions

			MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		4.5	5	5.5	V	
VIH	High-level input voltage		2			V	
VIL	Low-level input voltage				0.8	V	
IOH	High-level output current				-2.6	mA	
loL	L Low-level output current				24	mA	
t _W	Pulse duration, write					ns	
		Address before write↓					
t _{su}	Setup time	Data before write↑	15			ns	
		12					
		Address before write↓					
t _h	Hold time	Data before write↑	0			ns	
	Select before write↓		12				
T _A	Operating free-air temperature		0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDIT	MIN	TYP [†]	MAX	UNIT	
VIK		$V_{CC} = 4.5 V,$	$I_{I} = -18 \text{ mA}$			-1.2	V
VOH		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	V _{CC} -2		V
		$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$	2.4	3.2		V
VoL		$V_{CC} = 4.5 V,$	I _{OL} = 24 mA		0.35	0.5	V
1.	Control inputs	Vac EEV	V _I = 7 V			0.1	mA
Ħ	DQA and DQB ports	VCC = 5.5 V	V _I = 5.5 V			0.2	ma
	1W and 2W					20	
lіН	Other control inputs	$V_{CC} = 5.5 V$,	$V_1 = 2.7 \ V$			40	μΑ
DQA and DQB ports‡						50	1
1	Control inputs	Vac EEV	\/ ₁ 0.4\/			-0.2	A
IIL	DQA and DQB ports‡	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.2	mA
IO§		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	mA
Icc		V _{CC} = 5.5 V	·		80	110	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

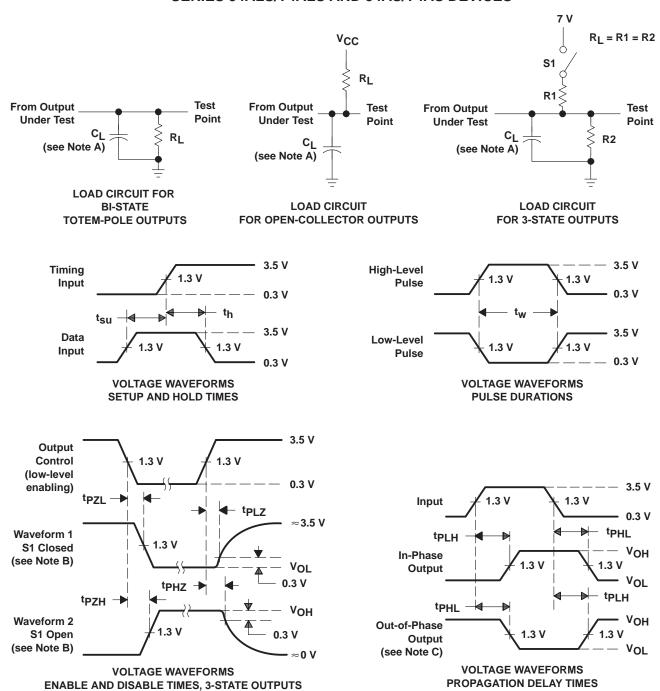
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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	V _{CC} = 4.5 C _L = 50 pF R1 = 500 Ω R2 = 500 Ω T _A = MIN to	UNIT	
			MIN	MAX	
^t a(A)	Any A	Any DQ	3	19	ns
.	S0	Any DQA	3	15	
^t a(S)	S1	Any DQB	3	15	ns
•	S2	Any DQA	3	14	
^t dis	S3	Any DQB	3	14	ns
	S2	Any DQA	3	17	
^t en	S3	Any DQB	3	17	ns
	W	Any DQ	5	23	
^t pd	DQA	DQB	5	26	ns
	DQB	DQA	5	26]

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, t_{Γ} = t_{f} = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGE OPTION ADDENDUM

www.ti.com 29-Apr-2010

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ALS870NT	NRND	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS870NTE4	NRND	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

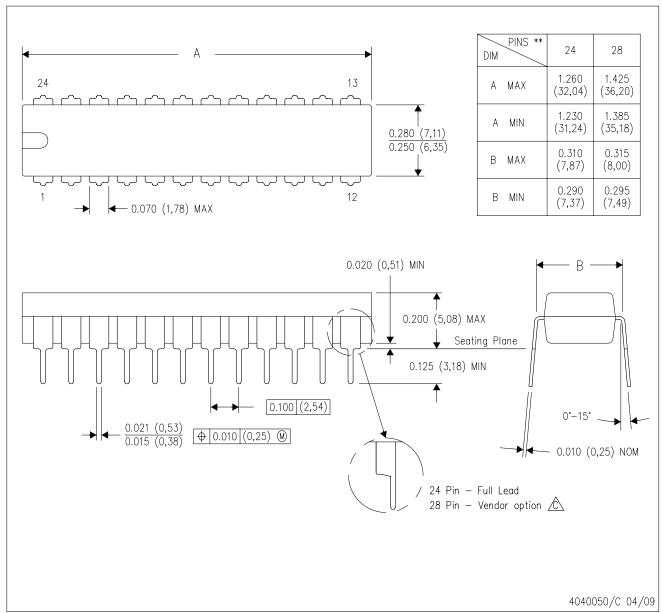
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NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

The 28 pin end lead shoulder width is a vendor option, either half or full width.



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