

# System LED Drivers for Mobile phones

# 6LEDs Illumination



**BD2802GU** No.11041EAT12

### Description

The BD2802GU is a RGB LED driver specifically engineered for decoration purposes. This RGB driver incorporates lighting patterns and illuminates without imposing any load on CPU. This RGB driver is best-suited for illumination using RGB LEDs and decoration using monochrome LEDs. In addition, this RGB driver has been successfully miniaturized through the use of a VCSP85H2 (2.8 mm 0.5 mm pitch) chip size package.

### Features

- 1) RGB LED driver (dual drivers)
  - A slope control function is incorporated (allowing dual drivers to be controlled independently).
  - Slope control can be implemented using the DC current.
  - Two modes "continuous illumination mode" and "illumination single cycle mode" are supported.
  - Independent external ON/OFF synchronizing terminals (of dual drivers) are provided.
  - Multiple drivers can be used concurrently by using the I<sup>2</sup>C address change function and supporting reference clock I/O.
- 2) Thermal shutdown
- 3) I<sup>2</sup>C BUS fast mode support (maximum rate: 400 kHz)
  - A device address can be changed via an external pin.
- \* This driver has not been designed for anti-radiation.
- \* This document may be altered without prior notice.
- \* This document does not provide for delivery.

# ●Absolute Maximum Ratings(Ta=25°C)

Parameter	Symbol	Limits	Unit
Maximum Applied voltage	VMAX	7	V
Power Dissipation	Pd	1250 <sup>(Note1)</sup>	mW
Operating Temperature Range	Topr	-40 <b>~</b> +85	°C
Storage Temperature Range	Tstg	-55 <b>~</b> +150	°C

(Note1)Power dissipation deleting is 10.0mW/ °C, when it's used in over 25 °C. (It's deleting is on the board that is ROHM's standard)

### ■Recommended Operating Conditions(VBAT ≥ VIO, Ta=-40~85°C)

Parameter	Symbol	Limits	Unit
VBAT input voltage	VBAT	٧	
VIO pin voltage	VIO	1.65 ~ 3.3	V

● Electrical Characteristics(Unless otherwise specified, Ta=25°C, VBAT=3.6V, VIO=1.8V)

Circuit Current]   VBAT Circuit current 1	Parameter	Symbol		Limits		Unit	Condition
VBAT Circuit current 1	Parameter	Symbol	Min.	Тур.	Max.	Unit	Cortalion
VBAT Circuit current 2	【Circuit Current】						
VBAT Circuit current 3	VBAT Circuit current 1	IBAT1	-	0.1	3.0	μΑ	RESETB=0V, VIO =0V
VBAT Circuit current 3	VBAT Circuit current 2	IBAT2	-	0.5	3.0	μΑ	RESETB=0V, VIO=1.8V
LED current Step   ILEDSTP   128	VBAT Circuit current 3	IBAT3	-	0.8	1.2	mA	Exclusive of LED current,
LED Maximum setup   IMAX   -   -   30.48   mA   RGB1 group, RGB2 group RGBISET=100kΩ   RGB1 group, RGB2 group,	【LED Driver】						
LED current accurate   ILED   18   20   22   mA   RGBISET=10kΩ   RGB1 group, RGB2 group, Terminal voltage =1V   ILED=20mA setting, RGB1SET =120kΩ   RGB1 group, RGB2 group, Terminal voltage =1V   ILED=20mA setting, RGB1SET =120kΩ   RGB1 group, RGB1SET =120kΩ   RGB1 group, RGB1SET =120kΩ   RGB1 group, RG	LED current Step	ILEDSTP		128		step	RGB1 group, RGB2 group
LED current accurate   ILED   18   20   22   mA   Terminal voltage = 1V   ED = 20mA setting, RGBISET = 120kΩ   RGB1 group, between RGB2 group, Terminal voltage = 1V   ILED=20mA setting   RGB1 group, between RGB2 group, Terminal voltage = 1V   ILED=20mA setting   RGB1 group, between RGB2 group, Terminal voltage = 1V   ILED=20mA setting	LED Maximum setup curren	IMAX	-	-	30.48	mA	RGBISET=100kΩ
LED current Matching   ILEDMT   -   5   10   %   Terminal voltage =1V   ILED OFF Leak current   ILKL   -   -   1.0   μA	LED current accurate	ILED	18	20	22	mA	Terminal voltage =1V ILED=20mA setting, RGBISET
[OSC] OSC oscillation frequency	LED current Matching	ILEDMT	-	5	10	%	Terminal voltage =1V
OSC oscillation frequency   fosc   0.8   1.0   1.2   MHz	LED OFF Leak current	ILKL	-	-	1.0	μΑ	
Lievel input voltage   VILI   -0.3   -   0.25×VIO   V	[OSC] OSC oscillation frequency	fosc	0.8	1.0	1.2	MHz	
Hevel input voltage	【SDA, SCL】(I2C interfac	e)	1	T			
Hysteresis of Schmitt trigger input   Vhysl   0.05×VIO   -   -   V   V   V	L level input voltage	VILI	-0.3	-	0.25×VIO	<del>-</del>	
trigger input L level output voltage VOLI 0 - 0.3 V SDA pin, IOL=3 mA Input current linI -10 - 10 μA Input voltage = 0.1×VIO~0.9×VIO [RESETB] (CMOS input pin) L level input voltage VILR -0.3 - 0.25×VIO V H level input voltage VIHR 0.75×VIO - VBAT+0.3 V Input voltage = 0.1×VIO~0.9×VIO  [ADDSEL] (CMOS input pin) L level input voltage VILADD -0.3 - 0.25×VBAT V H level input voltage VILADD -0.3 - 0.25×VBAT V H level input voltage VIHADD 0.7 ×VBAT - VBAT+0.3 V Input current linADD -10 - 10 μA Input voltage = 0.1×VBAT~0.9×VBA [RGB1CNT, RGB2CNT] (CMOS input pin with Pull-down resistance) L level input voltage VILCNT -0.3 - 0.25×VIO V H level input voltage VILCNT -0.3 - 0.25×VIO V Input current linCNT - 3.6 10 μA Input voltage = 1.8V [CLKIO(Output)] (CMOS output pin) L level output voltage VOLCLK 0.2 V IOL=1mA H level output voltage VOHCLK VIO-0.2 V IOH=1mA  Output frequency fclk 200 250 300 kHz  [CLKIO (Input)] (CMOS input pin) L level input voltage VILCK - 0.3 - 0.25×VIO V H level input voltage VOHCLK VIO-0.2 V IOH=1mA  Output frequency fclk 200 250 300 kHz  [CLKIO (Input)] (CMOS input pin) L level input voltage VILCK - 0.3 - 0.25×VIO V H level input voltage VILCK - 0.3 - 0.25×VIO V H level input voltage VILCK V IOH=1mA  Output frequency fclk 200 250 300 kHz  [CLKIO (Input)] (CMOS input pin) L level input voltage VILCK - 0.3 - 0.25×VIO V	H level input voltage	VIHI	0.75×VIO	-	VBAT+0.3	V	
Input current   Inin   -10   -10   μA   Input voltage = 0.1×VIO~0.9×VIO	Hysteresis of Schmitt trigger input	Vhysl	0.05×VIO	-	-	V	
[RESETB] (CMOS input pin)  L level input voltage	L level output voltage	VOLI	0	-	0.3	V	SDA pin, IOL=3 mA
Level input voltage	Input current	linl	-10	-	10	μΑ	Input voltage = 0.1×VIO~0.9×VIO
Hevel input voltage	[RESETB] (CMOS input	pin)					-
Input current	L level input voltage	VILR	-0.3	-	0.25×VIO	V	
[ADDSEL] (CMOS input pin)  L level input voltage	H level input voltage	VIHR	0.75×VIO	-	VBAT+0.3	V	
Lievel input voltage   VILADD   -0.3   -   0.25×VBAT   V	Input current		-10	-	10	μΑ	Input voltage = 0.1×VIO~0.9×VIO
H level input voltage	[ADDSEL] (CMOS input	pin)					-
Input current   InADD   -10   -   10   μA   Input voltage = 0.1×VBAT~0.9×VBAT	L level input voltage	VILADD	-0.3	-	0.25×VBAT	V	
[RGB1CNT, RGB2CNT] (CMOS input pin with Pull-down resistance)  L level input voltage VILCNT -0.3 - 0.25×VIO V  H level input voltage VIHCNT 0.75×VIO - VBAT+0.3 V  Input current linCNT - 3.6 10 μA Input voltage = 1.8V  [CLKIO(Output)] (CMOS output pin)  L level output voltage VOLCLK 0.2 V IOL=1mA  H level output voltage VOHCLK VIO-0.2 - V IOH=1mA  Output frequency fclk 200 250 300 kHz  [CLKIO (Input)] (CMOS input pin)  L level input voltage VILCLK -0.3 - 0.25×VIO V H level input voltage VIHCLK 0.75×VIO - VIO+0.3 V	H level input voltage	VIHADD	0.7 ×VBAT	-	VBAT+0.3	V	
L level input voltage	Input current	linADD	-10	-	10	μΑ	Input voltage = 0.1×VBAT~0.9×VBAT
H level input voltage VIHCNT 0.75×VIO - VBAT+0.3 V  Input current linCNT - 3.6 10 μA Input voltage = 1.8V  [CLKIO(Output)] (CMOS output pin)  L level output voltage VOLCLK 0.2 V IOL=1mA  H level output voltage VOHCLK VIO-0.2 V IOH=1mA  Output frequency fclk 200 250 300 kHz  [CLKIO (Input)] (CMOS input pin)  L level input voltage VILCLK -0.3 - 0.25×VIO V  H level input voltage VIHCLK 0.75×VIO - VIO+0.3 V	【RGB1CNT, RGB2CNT】	(CMOS inp	out pin with	Pull-down r	esistance)		
Input current   IinCNT   -	L level input voltage	VILCNT	-0.3	-	0.25×VIO	V	
[CLKIO(Output)] (CMOS output pin)         L level output voltage       VOLCLK       -       -       0.2       V       IOL=1mA         H level output voltage       VOHCLK       VIO-0.2       -       -       V       IOH=1mA         Output frequency       fclk       200       250       300       kHz         [CLKIO (Input)] (CMOS input pin)         L level input voltage       VILCLK       -0.3       -       0.25×VIO       V         H level input voltage       VIHCLK       0.75×VIO       -       VIO+0.3       V	H level input voltage	VIHCNT	0.75×VIO	-	VBAT+0.3	V	
L level output voltage         VOLCLK         -         -         0.2         V         IOL=1mA           H level output voltage         VOHCLK         VIO-0.2         -         -         V         IOH=1mA           Output frequency         fclk         200         250         300         kHz           [CLKIO (Input)]         (CMOS input pin)         Level input voltage         VILCLK         -0.3         -         0.25×VIO         V           H level input voltage         VIHCLK         0.75×VIO         -         VIO+0.3         V	Input current	linCNT	-	3.6	10	μA	Input voltage = 1.8V
H level output voltage	[CLKIO(Output)] (CMOS	output pin	)				,
H level output voltage	L level output voltage		-	-	0.2	V	IOL=1mA
[CLKIO (Input)]       (CMOS input pin)         L level input voltage       VILCLK       -0.3       -       0.25×VIO       V         H level input voltage       VIHCLK       0.75×VIO       -       VIO+0.3       V	H level output voltage		VIO-0.2	-	-	V	IOH=1mA
[CLKIO (Input)]       (CMOS input pin)         L level input voltage       VILCLK       -0.3       -       0.25×VIO       V         H level input voltage       VIHCLK       0.75×VIO       -       VIO+0.3       V	Output frequency			250	300	kHz	
L level input voltage VILCLK -0.3 - 0.25×VIO V H level input voltage VIHCLK 0.75×VIO - VIO+0.3 V			1	I			I
H level input voltage VIHCLK 0.75×VIO - VIO+0.3 V	L level input voltage		-0.3	-	0.25×VIO	V	
	H level input voltage			-		V	
	Input current			3.6			Input voltage = 1.8V

# ●Block Diagram / Application Circuit example

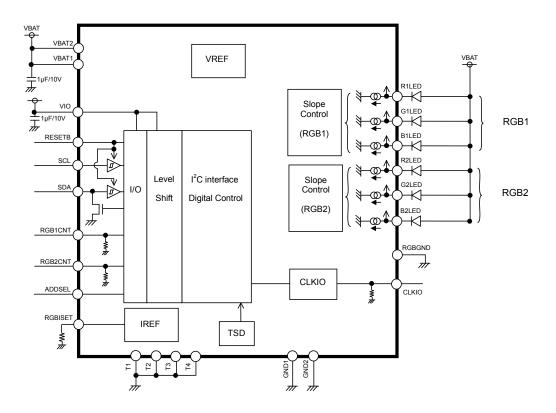
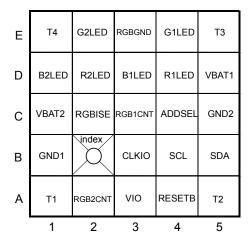


Fig.3 Block Diagram / Application Circuit example

# ●Pin Arrangement [Bottom View]

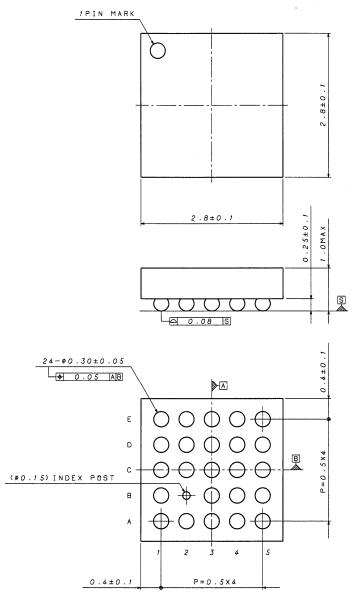


# Outside size figure

VCSP85H2 CSP small Package

Size : 2.8mm×2.8mm (Tolerance :  $\pm$  0.1mm each side) height 1.0mm max

Ball pitch: 0.5 mm



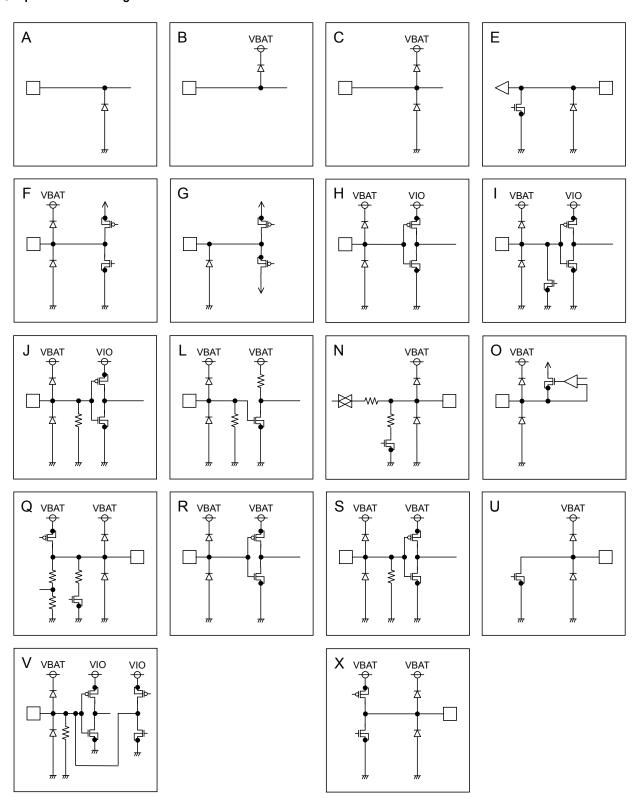
(UNIT:mm)

# ●Pin Functions

III I UIIC				Input	Level		
No	Pin No.	Pin Name	I/O	For Power	For GND	ESD Diode	Functions
1	D5	VBAT1	-	-	GND	Battery is connected	Α
2	C1	VBAT2	-	-	GND	Battery is connected	Α
3	A1	T1	-	VBAT	GND	Test Pin (short to GND)	S
4	A5	T2	-	VBAT	GND	Test Pin (short to GND)	S
5	E5	Т3	-	VBAT	GND	Test Pin (short to GND)	S
6	E1	T4	-	VBAT	-	Test Pin (short to GND)	В
7	А3	VIO	-	VBAT	GND	I/O voltage source is connected	С
8	A4	RESETB	1	VBAT	GND	Reset input (L: RESET, H: RESET cancel)	Н
9	B5	SDA	I/O	VBAT	GND	1 <sup>2</sup> C data input	I
10	B4	SCL	1	VBAT	GND	1 <sup>2</sup> C clock input	Н
11	B1	GND1	-	VBAT	-	Ground	В
12	C5	GND2	-	VBAT	-	Ground	В
13	E3	RGBGND	-	VBAT	-	Ground	В
14	C2	RGBISET	1	VBAT	GND	RGB LED reference current	0
15	D4	R1LED	1	-	GND	Red LED1 connected	Е
16	E4	G1LED	1	-	GND	Green LED1 connected	Е
17	D3	B1LED	1	-	GND	Blue LED1 connected	Е
18	D2	R2LED	1	-	GND	Red LED2 connected	Е
19	E2	G2LED	1	-	GND	Green LED2 connected	Е
20	D1	B2LED	I	-	GND	Blue LED2 connected	Е
21	С3	RGB1CNT	1	VBAT	GND	RGB1 LED external ON/OFF Synchronism (L : OFF, H : ON)*	J
22	A2	RGB2CNT	ı	VBAT	GND	RGB2 LED external ON/OFF Synchronism (L : OFF, H : ON)*	J
23	C4	ADDSEL	I	VBAT	GND	1 <sup>2</sup> C device address change terminal	R
24	В3	CLKIO	I/O	VBAT	GND	Standard clock input-and-output terminal	V
_							

<sup>\*</sup> A setup of a register is separately necessary to validate it.

# ●Equivalent circuit diagram



### ●I<sup>2</sup>C BUS format

The writing operation is based on the I<sup>2</sup>C slave standard.

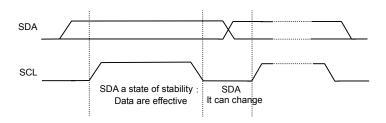
### · Slave address

	A7	A6	A5	A4	A3	A2	A1	R/W
ADDSEL=L	0	0	1	1	0	1	0	0
ADDSEL=H	0	0	1	1	0	1	1	0

Slave address can be changed with the external terminal ADDSEL.

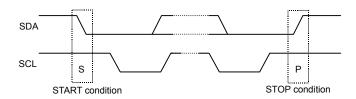
### Bit Transfer

SCL transfers 1-bit data during H. SCL cannot change signal of SDA during H at the time of bit transfer. If SDA changes while SCL is H, START conditions or STOP conditions will occur and it will be interpreted as a control signal.



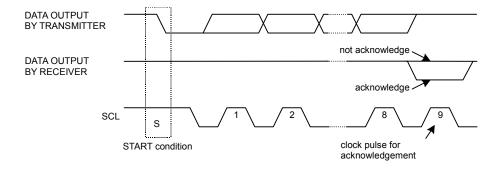
### START and STOP condition

When SDA and SCL are H, data is not transferred on the I<sup>2</sup>C- bus. This condition indicates, if SDA changes from H to L while SCL has been H, it will become START (S) conditions, and an access start, if SDA changes from L to H while SCL has been H, it will become STOP (P) conditions and an access end.



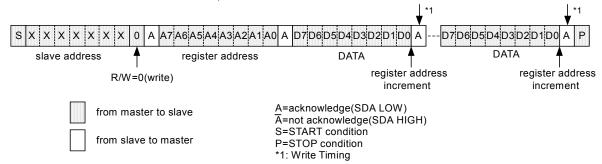
# Acknowledge

It transfers data 8 bits each after the occurrence of START condition. A transmitter opens SDA after transfer 8bits data, and a receiver returns the acknowledge signal by setting SDA to L.

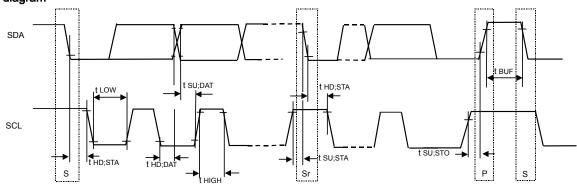


### · Writing protocol

A register address is transferred by the next 1 byte that transferred the slave address and the write-in command. The 3rd byte writes data in the internal register written in by the 2nd byte, and after 4th byte or, the increment of register address is carried out automatically. However, when a register address turns into the last address, it is set to 00h by the next transmission. After the transmission end, the increment of the address is carried out.



### Timing diagram



● Electrical Characteristics(Unless otherwise specified, Ta=25 °C, VBAT=3.6V, VIO=1.8V)

Dozometer	Cumph of	Sta	andard-m	ode	Fast-mode			- Unit
Parameter	Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit
[I <sup>2</sup> C BUS format]								
SCL clock frequency	fscl	0	-	100	0	-	400	kHz
LOW period of the SCL clock	tLOW	4.7	-	-	1.3	-	-	μs
HIGH period of the SCL clock	thigh	4.0	-	-	0.6	-	-	μs
Hold time (repeated) START condition	tup.cta	4.0			0.6			
After this period, the first clock is generated	thd;sta	4.0	-	-	0.0	-	-	μs
Set-up time for a repeated START	tsu;sta	4.7			0.6			110
condition	150,51A	4.7	-	-	0.0		_	μs
Data hold time	thd;dat	0	-	3.45	0	-	0.9	μs
Data set-up time	tsu;dat	250	-	-	100	-	-	ns
Set-up time for STOP condition	tsu;sto	4.0	-	-	0.6	-	-	μs
Bus free time between a STOP	tour.	4.7			1.2			110
and START condition	IBOF	tBUF 4.7		_	1.3	_	-	μs

●Register map

Address					Resiste	er data				Function
Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Function
00h	W	-	-	CLKMD	CLKEN	-	-	-	SFTRST	Soft Reset clock setup
01h	W	-	RGB2MEL	RGB2OS	RGB2EN	-	RGB1MEL	RGB10S	RGB1EN	RBG-LED control
02h	W	SFRGB1(1)	SFRGB1(0)	SRRGB1(1)	SRRGB1(0)	-	TRGB1(2)	TRGB1(1)	TRGB1(0)	RGB1-hour setup
03h	W	-	IR11(6)	IR11(5)	IR11(4)	IR11(3)	IR11(2)	IR11(1)	IR11(0)	R1 current 1 setup
04h	W	-	IR12(6)	IR12(5)	IR12(4)	IR12(3)	IR12(2)	IR12(1)	IR12(0)	R1 current 2 setup
05h	W	-	-	-	-	PR1(3)	PR1(2)	PR1(1)	PR1(0)	R1 Wave patturn setup
06h	W	=	IG11(6)	IG11(5)	IG11(4)	IG11(3)	IG11(2)	IG11(1)	IG11(0)	G1 current 1 setup
07h	W	=	IG12(6)	IG12(5)	IG12(4)	IG12(3)	IG12(2)	IG12(1)	IG12(0)	G1 current 2 setup
08h	W	-	-	-	-	PG1(3)	PG1(2)	PG1(1)	PG1(0)	G1 Wave patturn setup
09h	W	-	IB11(6)	IB11(5)	IB11(4)	IB11(3)	IB11(2)	IB11(1)	IB11(0)	B1 current 1 setup
0Ah	W	=	IB12(6)	IB12(5)	IB12(4)	IB12(3)	IB12(2)	IB12(1)	IB12(0)	B1 current 2 setup
0Bh	W	=	ı	-	-	PB1(3)	PB1(2)	PB1(1)	PB1(0)	B1 Wave patturn setup
0Ch	W	SFRGB2(1)	SFRGB2(0)	SRRGB2(1)	SRRGB2(0)	-	TRGB2(2)	TRGB2(1)	TRGB2(0)	RGB2-hour setup
0Dh	W	-	IR21(6)	IR21(5)	IR21(4)	IR21(3)	IR21(2)	IR21(1)	IR21(0)	R2 current 1 setup
0Eh	W	-	IR22(6)	IR22(5)	IR22(4)	IR22(3)	IR22(2)	IR22(1)	IR22(0)	R2 current 2 setup
0Fh	W	-	-	-	-	PR2(3)	PR2(2)	PR2(1)	PR2(0)	R2 Wave patturn
10h	W	-	IG21(6)	IG21(5)	IG21(4)	IG21(3)	IG21(2)	IG21(1)	IG21(0)	G2 current 1 setup
11h	W	-	IG22(6)	IG22(5)	IG22(4)	IG22(3)	IG22(2)	IG22(1)	IG22(0)	G2 current 2 setup
12h	W	-	-	-	-	PG2(3)	PG2(2)	PG2(1)	PG2(0)	G2 Wave patturn setup
13h	W	-	IB21(6)	IB21(5)	IB21(4)	IB21(3)	IB21(2)	IB21(1)	IB21(0)	B2 current 1 setup
14h	W	-	IB22(6)	IB22(5)	IB22(4)	IB22(3)	IB22(2)	IB22(1)	IB22(0)	B2 current 2 setup
15h	W	-	-	-	-	PB2(3)	PB2(2)	PB2(1)	PB2(0)	B2 Wave patturn setup

Input "0" for "-".

Vacancy address may be use for test.

Prohibit to accessing the address that isn't mentioned and the register for test.

# ● Register Description

Adress 00h <Soft Reset>

BIT	Name	Initial	Function					
DII	ivairie	IIIIIIai	0	1				
D7	-	-	-	-				
D6	-	-	-	-				
D5	CLKMD	0	Clock Input mode	Clock Output mode				
D4	CLKEN	0	Clock input and output invalid	Clock input and output Effective				
D3	-	-	-	-				
D2	-	-	-	-				
D1	-	-	-	-				
D0	SFTRST	0	Reset Release	Reset				

# Adress 01h <RGB LED control >

BIT	Name	Init	Fund	ction		
DII	Name	IIIIL	0	1		
D7	-	-	-	-		
D6	RGB2MEL	0	RGB2 external control invalid	RGB2 external control valid		
D5	RGB2OS	0	RGB2 Stop	RGB2 1 periodic operation		
D4	RGB2EN	0	RGB2 Stop	RGB2 continuous operation		
D3	ı	ı	-	-		
D2	RGB1MEL	0	RGB1 external control invalid	RGB1 external control valid		
D1	RGB10S	0	RGB1 Stop	RGB1 1 periodic operation		
D0	RGB1EN	0	RGB1 Stop	RGB1 continuous operation		

<sup>\*</sup> RGB\*OS returns to 0 automatically after 1 cycle operation.

### Adress 02h <RGB1 time>

Agress	02h <rgb11< th=""><th>ime&gt;</th><th></th><th></th><th></th><th></th></rgb11<>	ime>							
BIT	Name	Init			Function				
DII	Name	IIIIL		0		1			
			SFRGB1(	1)	SFRGB1(0)	Slope Down transition			
D7	SFRGB1(1)	0	0	1)	0	Slope Down transition			
	Of ROBI(1)		0		1	Wave form cycle / 16			
			1		0	Wave form cycle / 8			
			1		1	Wave form cycle / 4			
D6	SFRGB1(0)	0	It is a theoretical	value on logic	c control, and the reac	tion time of the analog section is			
					e time from a slope sta				
			SRRGB1(	1)	SRRGB1(0)	Slope Up transition			
D5	SRRGB1(1) 0		SRRGB1(1) 0		0	,	0	0	
			0		1	Wave form cycle / 16			
			1		0	Wave form cycle / 8			
			1		1	Wave form cycle / 4			
D4	SRRGB1(0)	0	It is a theoretical	value on logic	ion time of the analog section is not				
			included."Slope time" is the time from a slope start to a slope end.						
D3	_	_		_					
D2	TRGB1(2)	0	TRGB1(2)	TRGB1(1)	) TRGB1(0)	Wave form cycle			
D2	TRGBT(2)	0	0	0	0	0.131 s			
			0	0	1	0.52 s			
			0	1	0	1.05 s			
D1	TRGB1(1)	0	0	1	1	2.10 s			
			1	0	0	4.19 s			
			1	0	1	8.39 s			
D0	TRGB1(0)	0	1	1	0	12.6 s			
	IRGDI(U)		1	1	1	16.8 s			
		l							

Setting time is counted based on the frequency of OSC. The above-mentioned value is a value at the time of Typ (1MHz). When operating by the external clock, input frequency is a value at the time of Typ (250kHz).

<sup>\*</sup> RGB\*EN precedes to RGB\*OS. In use in 1 cycle operation, there is the necessity for RGB\*EN=0.

<sup>\*</sup>Refer to "•Use of a RGB wave setup" for the detailed function of each register of this page.

Adress 03h <R1 current 1setup >

7101000	on artification											
BIT	Name	Init				Fun	nction					
DII	Ivaille	11111		C	)				1			
D7	-	-		-					-			
D6	IR11(6)	0	IR11(6)	IR11(5)	IR11(4)	IR11(3)	IR11(2)	IR11(1)	IR11(0)	Current		
D5	IR11(5)	0	0	0	0	0	0	0	0	0		
D4	IR11(4)	0	0	0	0	0	0	0	1	0.2mA		
D3	IR11(3)	0	:	:	:	:	:	:	•	0.2mA step		
D2	IR11(2)	0	1	1	1	1	1	1	0	25.2mA		
D1	IR11(1)	0	1	1	1	1	1	1	1	25.4mA		
D0	IR11(0)	0	At RGBISE	Tpin 120k	Ω connect	ion						

Adress 04h <R1 current2 setup >

	o m - 447 canonic cottap											
BIT	Name	Init				Fun	nction					
DII	ivallie	Ш		C	)				1			
D7	-	-		_					-			
D6	IR12(6)	0	IR12(6)	IR12(5)	IR12(4)	IR12(3)	IR12(2)	IR12(1)	IR12(0)	Current		
D5	IR12(5)	0	0	0	0	0	0	0	0	0		
D4	IR12(4)	0	0	0	0	0	0	0	1	0.2mA		
D3	IR12(3)	0	•	•	•	•	•	•	•	0.2mA		
	. ,		•	•	•	•	•	•	•	step		
D2	IR12(2)	0	1	1	1	1	1	1	0	25.2mA		
D1	IR12(1)	0	1	1	1	1	1	1	1	25.4mA		
D0	IR12(0)	0	At RGBISE	Tpin 120k	Ω connecti	on						

Adress 05h <R1 Wave Pattern >

					Fu	nction		
BIT	Name	Init		0		1		
D7	-	-		-		-		
D6	-	-		-			-	
D5	-	-		-			-	
D4	-	-		-			-	
D3	PR1(3)	0	PR1(3)	PR1(2)	PR1(1)	PR1(0)	Wave	
	FKI(3)		0	0	0	0	Pattern1	
			0	0	0	1	Pattern2	
D2	PR1(2)	1	0	0	1	0	Pattern3	
				•		•		
				•		•		
D1	PR1(1)	1		•	•	•	•	
			1	1	0	1	Pattern14	
<b>D</b> 0	554(0)		1	1	1	0	Pattern15	
D0	PR1(0)	R1(0)   1	1	1	1	1	Pattern16	
				l	ı	L	1	

Adress 06h <G1 current1 setup >

7 10 000	areas our sort current ractures										
BIT	Name	Init				Fun	ction				
DII	INAITIE	IIIIC		0				1			
D7	-	-			-			-			
D6	IG11(6)	0	IG11(6)	IG11(5)	IG11(4)	IG11(3)	IG11(2)	IG11(1)	IG11(0)	Current	
D5	IG11(5)	0	0	0	0	0	0	0	0	0	
D4	IG11(4)	0	0	0	0	0	0	0	1	0.2mA	
D3	IG11(3)	0	<u> </u>	•	:	•	:		•	0.2mA step	
D2	IG11(2)	0	1	1	1	1	1	1	0	25.2mA	
D1	IG11(1)	0	1	1	1	1	1	1	1	25.4mA	
D0	IG11(0)	0	At RGBISETpin 120k $\Omega$ connection								

<sup>\*</sup>Refer to "•Use of a RGB wave setup " for the detailed function of each register of this page.

Adress 07h <G1 current2 setup >

Adiess of the Greaterize scup -											
BIT	Name	Init				Fun	ction	otion			
DII	ivairie	IIIIL		(	)		1				
D7	-	-			-				-		
D6	IG12(6)	0	IG12(6)	IG12(5)	IG12(4)	IG12(3)	IG12(2)	IG12(1)	IG12(0)	Current	
D5	IG12(5)	0	0	0	0	0	0	0	0	0	
D4	IG12(4)	0	0	0	0	0	0	0	1	0.2mA	
D3	IG12(3)	0	:	:	•	•	:	•	:	0.2mA step	
D2	IG12(2)	0	1	1	1	1	1	1	0	25.2mA	
D1	IG12(1)	0	1	1	1	1	1	1	1	25.4mA	
D0	IG12(0)	0	At RGBISETpin 120k $\Omega$ connection								

### Adress 08h <G1 G1 Wave Pattern >

Auless voli STGT Wave Falletti >									
BIT	Name	Init			Fun	ction			
DII	ivairie	Ш		0		1			
D7	-	-		-			-		
D6	-	-		-			-		
D5	-	-		-			-		
D4	-	-		-			-		
Do	504(0)		PG1(3)	PG1(2)	PG1(1)	PG1(0)	Wave		
D3	PG1(3)	0	0	0	0	0	Pattern 1		
			0	0	0	1	Pattern 2		
D2	PG1(2)	1	0	0	1	0	Pattern 3		
	( )			•	•		•		
				•	•	•	•		
D1	PG1(1)	1	•	•	•	•	•		
			1	1	0	1	Pattern 14		
DO	PG1(0)	1	1	1	1	0	Pattern 15		
50	D0 PG1(0)	1	1	1	1	1	Pattern 16		

### Adress 09h <B1 current1setup >

Adress on Broadentostap											
BIT	Name	Init				Fur	nction				
DII	Name	IIIIL		0				1			
D7	-	-			-				-		
D6	IB11(6)	0	IB11(6)	IB11(5)	IB11(4)	IB11(3)	IB11(2)	IB11(1)	IB11(0)	Current	
D5	IB11(5)	0	0	0	0	0	0	0	0	0	
D4	IB11(4)	0	0	0	0	0	0	0	1	0.2mA	
D3	IB11(3)	0	-	•	•	•	•	•	•	0.2mA	
	1011(3)	U		•	•	•	•	•	•	step	
D2	IB11(2)	0	1	1	1	1	1	1	0	25.2mA	
D1	IB11(1)	0	1	1	1	1	1	1	1	25.4mA	
D0	IB11(0)	0	At RGBISETpin 120kΩ connection								

# Adress 0Ah <B1 current2setup >

BIT	Name	Init				Fun	ction	ction				
БП	Name	IIIIL		0			1					
D7	-	-			-		-					
D6	IB12(6)	0	IB12(6)	IB12(5)	IB12(4)	IB12(3)	IB12(2)	IB12(1)	IB12(0)	Current		
D5	IB12(5)	0	0	0	0	0	0	0	0	0		
D4	IB12(4)	0	0	0	0	0	0	0	1	0.2mA		
D3	IB12(3)	0		•	•	•	•	•	•	0.2mA		
D3	1012(3)	U	-	•	•	•	•	•		step		
D2	IB12(2)	0	1	1	1	1	1	1	0	25.2mA		
D1	IB12(1)	0	1	1	1	1	1	1	1	25.4mA		
D0	IB12(0)	0	At RGBISETpin 120kΩ connection									

<sup>\*</sup> Refer to "●Use of a RGB wave setup " for the detailed function of each register of this page.

		D 4 144 D 44	
Adress	OBh	<b1 pattern:<="" td="" wave=""><td>&gt;</td></b1>	>

BIT	Name	Init			Fur	nction			
DII	INAITIE	11111		0			1		
D7	-	-		-		-			
D6	ı	-		-			-		
D5	-	-		-			-		
D4	ı	-		-			-		
D3	PB1(3)	0	PB1(3)	PB1(2)	PB1(1)	PB1(0)	Wave		
	1 1 1 (3)	U	U	0	0	0	0	0	Pattern1
			0	0	0	1	Pattern2		
D2	PB1(2)	1	0	0	1	0	Pattern3		
			•	•		•	•		
			•	•	•	•	•		
D1	PB1(1)	1	•	•	•	•	•		
			1	1	0	1	Pattern14		
D0	DD4(0)	_	1	1	1	0	Pattern15		
D0	D0 PB1(0)	0)   1	1	1	1	1	Pattern16		

Adress 0Ch <RGB2 time >

Nomo	lnit			Function	
ivame	IIIIL		0		1
		SFRGB2(1	)	SFRGB2(0)	Slope Down transition
SFRGB2(1)	0	0		0	0
		0		1	Wave form cycle / 16
		1		0	Wave form cycle / 8
		1		1	Wave form cycle / 4
SFRGB2(0)	0	not included.	•		•
		SRRGB2(1	)	SRRGB2(0)	Slope up transition
CDDCD2/4\	0	·	,	` '	0
D5 SRRGB2(1)	(1) 0	<u> </u>		1	Wave form cycle / 16
		1		0	Wave form cycle / 8
		1		1	Wave form cycle / 4
SRRGB2(0)	0	included.	•		time of the analog section is not
-	-		-		-
TD 0 D0 (0)	•	TRGB2(2)	TRGB2(1)	TRGB2(0)	Wave form cycle
TRGB2(2)	0	0	0	0	0.131 s
		0	0	1	0.52 s
		0	1	0	1.05 s
TRGB2(1)	0	0	1	1	2.10 s
		1	0	0	4.19 s
		1	0	1	8.39 s
TRGB2(0)	0	1	1	0	12.6 s
D0 TRGB2(0)	U	1	1	1	16.8 s
	SRRGB2(1)  SRRGB2(0)  - TRGB2(2)	SFRGB2(1)       0         SFRGB2(0)       0         SRRGB2(1)       0         SRRGB2(0)       0         -       -         TRGB2(2)       0         TRGB2(1)       0	SFRGB2(1)         0         SFRGB2(1)           SFRGB2(0)         0         1           SFRGB2(0)         0         1           It is a theoretical not included. "Slope time" is the state of	SFRGB2(1)   0     SFRGB2(1)	SFRGB2(1)   O   SFRGB2(1)   SFRGB2(0)     SFRGB2(1)   O   O   O     O   O   O     O   O   O

Setting time is counted based on the frequency of OSC. The above-mentioned value is a value at the time of Typ (1MHz). When operating by the external clock, input frequency is a value at the time of Typ (250kHz)

<sup>\*</sup> Refer to " Use of a RGB wave setup " for the detailed function of each register of this page.

Adress 0Dh <R2 current 1setup>

7101000	Auress obli sitz current isetup										
l DIT	Name	Init				Fun	ction				
BIT	ivallie	IIIIL	0					1			
D7	-	-			-		-				
D6	IR21(6)	0	IR21(6)	IR21(5)	IR21(4)	IR21(3)	IR21(2)	IR21(1)	IR21(0)	Current	
D5	IR21(5)	0	0	0	0	0	0	0	0	0	
D4	IR21(4)	0	0	0	0	0	0	0	1	0.2mA	
D3	IR21(3)	0	•	•	•	•	•	•	•	0.2mA step	
D2	IR21(2)	0	1	1	1	1	1	1	0	25.2mA	
D1	IR21(1)	0	1	1	1	1	1	1	1	25.4mA	
D0	IR21(0)	0	At RGBISETpin 120kΩ connection								

Adress 0Eh <R2 current 2setup>

Adress Ven 442 suitsit 25stap										
BIT	Name	Init				Fun	ction			
DII	Name	ITIIL		0			1			
D7	-	-			-				-	
D6	IR22(6)	0	IR22(6)	IR22(5)	IR22(4)	IR22(3)	IR22(2)	IR22(1)	IR22(0)	Current
D5	IR22(5)	0	0	0	0	0	0	0	0	0
D4	IR22(4)	0	0	0	0	0	0	0	1	0.2mA
D3	IR22(3)	0	:	•	•	•			•	0.2mA step
D2	IR22(2)	0	1	1	1	1	1	1	0	25.2mA
D1	IR22(1)	0	1	1	1	1	1	1	1	25.4mA
D0	IR22(0)	0	At RGBISETpin 120kΩ connection							

Adress 0Fh <R2 Wave Pattern setup>

DIT			iii ootap		Fun	ction			
BIT	Name	Init		0		1			
D7	-	-		-			-		
D6	ı	-		-			-		
D5	ı	-		-			-		
D4	-	-		-			-		
D3	DD0/0)		PR2(3)	PR2(2)	PR2(1)	PR2(0)	Wave		
DS	PR2(3)	0	0	0	0	0	Pattern 1		
			0	0	0	1	Pattern 2		
D2	PR2(2)	1	0	0	1	0	Pattern 3		
	. ,		•		•		•		
			-		•		·		
D1	PR2(1)	1	-		•		·		
			1	1	0	1	Pattern 14		
D0	DDO(A)		1	1	1	0	Pattern 15		
D0	0 PR2(0)	PR2(0) 1	1	1	1	1	Pattern 16		

Adress 10h <G2 current 1setup>

7101000	1011 132 current 13ctup										
BIT	Name	Init	Function								
DII	Name	HIIL	0				1				
D7	-	-		-	-			-			
D6	IG21(6)	0	IG21(6)	IG21(5)	IG21(4)	IG21(3)	IG21(2)	IG21(1)	IG21(0)	Current	
D5	IG21(5)	0	0	0	0	0	0	0	0	0	
D4	IG21(4)	0	0	0	0	0	0	0	1	0.2mA	
D3	IG21(3)	0	<u> </u>		:	:	:	:	•	0.2mA step	
D2	IG21(2)	0	1	1	1	1	1	1	0	25.2mA	
D1	IG21(1)	0	1	1	1	1	1	1	1	25.4mA	
D0	IG21(0)	0	At RGBISETpin 120k $\Omega$ connection								

<sup>\*</sup> Refer to "●Use of a RGB wave setup " for the detailed function of each register of this page.

Adress 11h <G2 current 2setup>

		0111 200		Function							
BIT	Name	Init		(	)	1 un	Clion		1		
D7	-	-			-			-			
D6	IG22(6)	0	IG22(6)	IG22(5)	IG22(4)	IG22(3)	IG22(2)	IG22(1)	IG22(0)	Current	
D5	IG22(5)	0	0	0	0	0	0	0	0	0	
D4	IG22(4)	0	0	0	0	0	0	0	1	0.2mA	
D3	IG22(3)	0	:		•		•	•		0.2mA step	
D2	IG22(2)	0	1	1	1	1	1	1	0	25.2mA	
D1	IG22(1)	0	1	1	1	1	1	1	1	25.4mA	
D0	IG22(0)	0	At RGBISETpin 120k $\Omega$ connection								

Adress 12h <G2 Wave Pattern setup >

Adress	12n <g2 pattern="" setup="" wave=""></g2>										
DIT	IT Nome		Function								
BIT	Name	Init		0		1					
D7	-	-		-		-					
D6	-	-		-			-				
D5	-	-		-			-				
D4	-	-		-		-					
Do	D.C.(0)	0	PG2(3)	PG2(2)	PG2(1)	PG2(0)	Wave				
D3	PG2(3)		Ü	U	0	0	0	0	0	0	Pattern 1
		1	1	0	0	0	1	Pattern 2			
D2	PG2(2)			1	1	1	0	0	1	0	Pattern 3
	, ,			•	•	•	•				
			•	•	-	•	-				
D1	PG2(1)	PG2(1) 1	•	•	•	•	•				
	D0 PG2(0)						1	1	0	1	Pattern 14
DO		1	1	1	1	0	Pattern 15				
50		(0)   1	1	1	1	1	Pattern 16				

Adress 13h <B2 current 1setup>

DIT	None	lm:4				Fun	ction				
BIT	Name	Init		0				1			
D7	-	-			-			-			
D6	IB21(6)	0	IB21(6)	IB21(5)	IB21(4)	IB21(3)	IB21(2)	IB21(1)	IB21(0)	Current	
D5	IB21(5)	0	0	0	0	0	0	0	0	0	
D4	IB21(4)	0	0	0	0	0	0	0	1	0.2mA	
D3	IB21(3)	0	•	•	•	•	•	•	•	0.2mA	
D2	IB21(2)	0	1	1	1	1	1	1	0	step 25.2mA	
D1	IB21(1)	0	1	1	1	1	1	1	1	25.4mA	
D0	IB21(0)	0	At RGBISE	At RGBISETpin 120kΩ connection							

Adress 14h <B2 current 2setup>

. 10	Adiess 1411 452 current 25ctup										
BIT Name	Name	Init	Function								
DII	Ivaille	11111		(	)		1				
D7	-	-			-			-			
D6	IB22(6)	0	IB22(6)	IB22(5)	IB22(4)	IB22(3)	IB22(2)	IB22(1)	IB22(0)	Current	
D5	IB22(5)	0	0	0	0	0	0	0	0	0	
D4	IB22(4)	0	0	0	0	0	0	0	1	0.2mA	
D3	IB22(3)	0	•	•	•	•	•	•	•	0.2mA	
	`		•	•	•	•	•	•	•	step	
D2	IB22(2)	0	1	1	1	1	1	1	0	25.2mA	
D1	IB22(1)	0	1	1	1	1	1	1	1	25.4mA	
D0	IB22(0)	0	At RGBISETpin 120kΩ connection								

<sup>\*</sup>Refer to "•Use of a RGB wave setup " for the detailed function of each register of this page.

Adress 15h <B2 Wave Pattern setup >

DIT	BIT Name		·		Fun	ction					
ВП				0		1					
D7	-	-		-		-					
D6	-	-		-			-				
D5	-	-		-			-				
D4	-	-		-		-					
Do	DD0(0)	DD0(0)	_	PB2(3)	PB2(2)	PB2(1)	PB2(0)	Wave			
D3	PB2(3)	0	0	0	0	0	0	0	0	Pattern 1	
		1	1	1	1	1	0	0	0	1	Pattern 2
D2	PB2(2)						0	0	1	0	Pattern 3
	( )			•			•	•			
			•				•				
D1	PB2(1)	1	-		-	-					
			1	1	0	1	Pattern 14				
DO	D0 PB2(0)	PB2(0) 1	1	1	1	0	Pattern 15				
D0			1	1	1	1	Pattern 16				

<sup>\*</sup> Refer to "ullet Use of a RGB wave setup " for the detailed function of each register of this page.

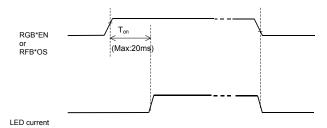
### RGB LED Driver Operation Description

- Two drivers "RGB1 (R1LED, G1LED, B1LED)" and "RGB2 (R2LED, G2LED, B2LED)" are mounted.
- A slope function is incorporated to control drivers independently.
- Refer to RGB Waveform Setting for more information about output waveform setting.
- The LED current can be set via a resistance value (RISET) to be connected to the RGBISET terminal. The maximum current value can be derived from the following expression:

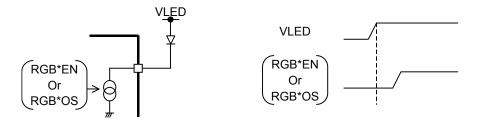
ILEDmax [A] =  $3.048 / RISET [k\Omega] (Typ)$ 

However, this setting must be made so that the maximum current value can be less than or equal to 30.48mA. In addition, the RGBISET terminal has an overcurrent protection circuit to prevent the excessive LED current from flowing for low impedance to the ground.

- Note that the setting voltage shall be higher than or equal to a saturation voltage (0.2V) in the constant current circuit. When LED Vf is large, the LED destination shall be connected to another step-up circuit.



The LED destination is fixed before on (RGB\*EN=Hi or RGB\*OS=Hi).



# ●The synchronism of RGB1/RGB2

The period of RGB1 and RGB2 and start, stop timing can be set up independently.

When synchronizes RGB1 and RGB2, You must start an internal counter at the same time under the state of resetting. (Internal Counter are prepared for each of RGB1 and RGB2, so You must reset both.)

<How to reset internal Counter>

Inside Counter can be reset by carrying out one of following actions.

- Reset by hard reset (RSTB\_IL). (RGB1, RGB2 is reset together.)
- Reset by soft reset. (RGB1, RGB2 is reset together.)
- It is written register of the current setup (I1 · I2), the slope setup, the period setup and the pattern setup. Internal Counter of RGB1 is reset when it is written between Address=0Bh from 02h. Internal Counter of RGB2 is reset when it is written between Address=15h from 0Ch. Counter is reset as to overwriting the same value.

### Note)

Internal Counter isn't reset if write RGB1EN =L and RGB2EN =L. (Address=01h).

When it write RGB1EN=L (RGB2EN=L), inside Counter is held, and IC will operate from the held state at next restart.

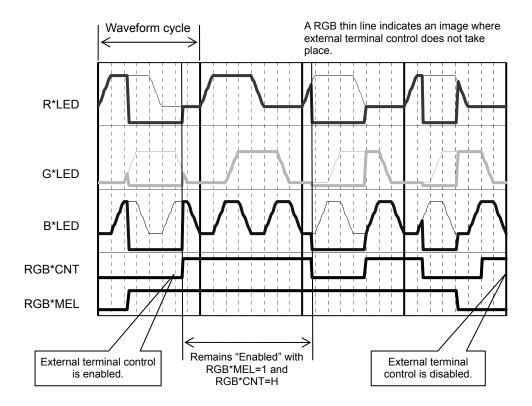
### ●RGB Waveform Setting

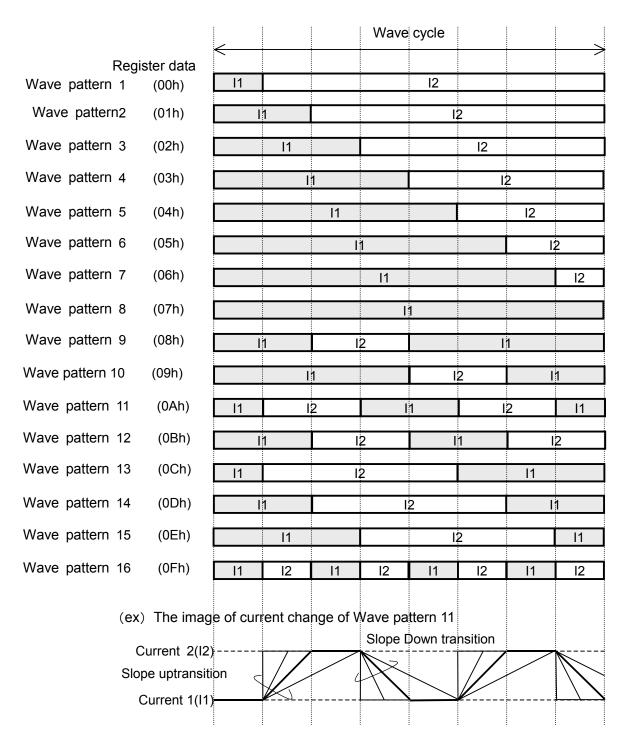
Various kinds of RGB control can be implemented by designating waveform cycles, waveform patterns, current settings 1, 2 and rising/falling slope times.

To activate a RGB waveform, a continuous operation via RGB\*EN or a single-shot operation via RGB\*OS can be selected. In addition, when control via the external terminal RGB\*CNT is enabled via RGB\*MEL, the corresponding LED can be lit in synchronization with the external signal.

- 1. Waveform cycle
  - A single cycle time is set for a waveform pattern.
  - This setting can be made independently for RGB1 and RGB2.
- 2. Waveform pattern
  - A pattern in a waveform cycle is set.
  - Sixteen types of waveform patterns can be set in units of waveform patterns.
  - For concrete waveform patterns, refer to the timing diagram shown on the next page.
- 3. Current settings 1 and 2 (I1, I2)
  - Two currents in a waveform pattern are set.
  - When the maximum current value is 25.4mA, it is possible to set the current ranging from 0 to 25.4mA with an increment of 0.2mA (128 steps).
  - The polarity of a waveform is determined by the greater-than/ less-than relationship in the current setting.
  - This setting can be made in units of terminals.
- 4. Rising/falling slope time
  - A current change time during switching between current settings 1 and 2 is set.
  - A time per step (0.2mA) is calculated based on a difference between the currents selected in current settings 1, 2 and a setting slope time.
  - For this reason, a time per step (0.2mA) is short when a difference between setting currents I1 and I2 is large. In contrast, it is long when a difference between setting currents I1 and I2 is small.
  - Regardless of current settings 1 and 2, a rising slope time applies at current increase and a falling slope time applies at current decrease. For concrete waveform images, refer to the timing diagram shown on the next page.
- 5. External terminal synchronization control

When control via the external terminal RGB\*CNT is enabled via RGB\*MEL, lighting is enabled if the input external signal goes "H." In contrast, it is disabled if the external input signal goes "L." In this way, synchronization with the external signal is enabled so that LED can be blinked in conjunction with a ringing tone (a melody signaling a ringtone).





RGB wave setting timing diagram

### 6. Clock I/O

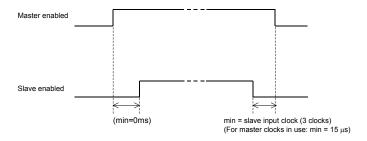
A reference clock I/O function is mounted in this IC chip. When two IC chips are used to extend an illumination capability, clock supply to the other RGB LED driver can be accomplished for synchronization with this LSI chip. This setting can be made via the register.

Clock output can be made with CLKEN=1 and CLKMD=1.

Reg	ister	CLKIO terminal state	Clask recention		
CLKEN	CLKMD	CLKIO terminai state	Clock reception		
0	0/1	Input	Does not receive external clocks.		
1	0	Input	Operates on external clocks.		
ı	1	Output	-		

●When two BD2802GU drivers are used and the clock is shared by CLKIO:

Because a sequence is already programmed within an IC chip for RGB falling, "Enable" shall be set to "OFF" and clock supply shall be continued for at least three clocks so that operations can be performed using external clocks.



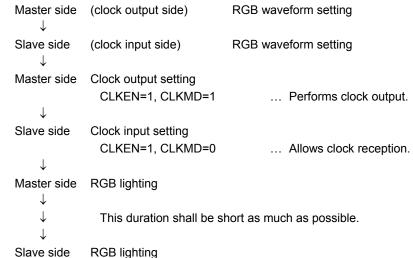
Master: Chip using CLKIO as output Slave: Chip using CLKIO as input

\*Even in independent slave mode, its setting "Enable" shall be reset to "OFF" and then clock supply must be continued for 3 clocks or more.

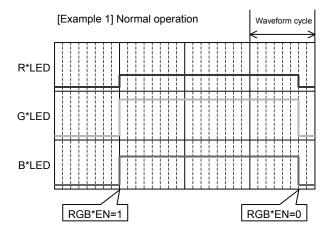
Clock I/O switching shall be avoided during RGB operation.

Enable: CLKEN, RGB1EN, RGB2EN, RGB1OS, RGB2OS

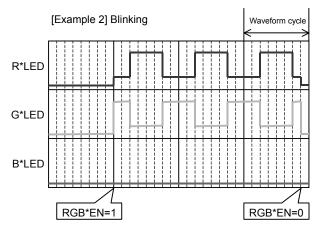
# - Setting example



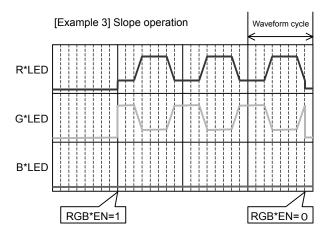
### 7. RGB waveform setting examples



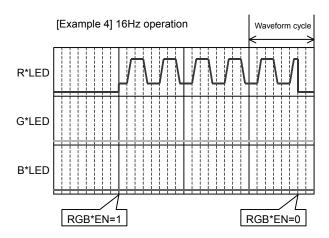
Selecting a waveform pattern 8 causes a continuous normal operation to take place through the setting current 1.



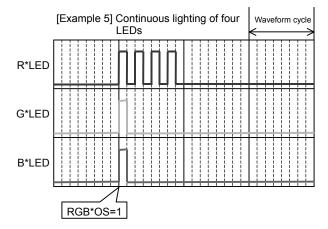
Setting a rising/falling slope time to "0" causes blinking to take place. Phase switching takes place via the setting currents of R and G.



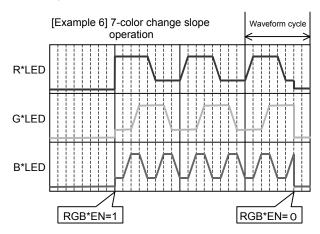
When a rising/falling slope time is longer than the setting made in example 2, a continuous color change is made by slope operation.



Combining the settings of a waveform pattern 11 and a waveform cycle 131ms causes blinking at a rate of 15.3Hz (approx. 16Hz).



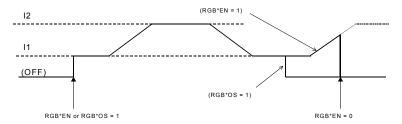
This example shows that lighting occurs continuously in the order of white, red, red and red. To achieve this, waveform patterns 16, 1 and RGB\*OS single cycle operation need to be combined.



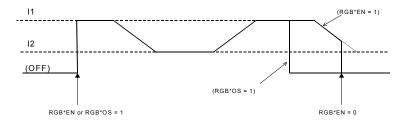
R, G and B waveform patterns are set in a way that any of R, G and B changes constantly.

- 8. RGB slope waveforms
  - Example of waveform at activation

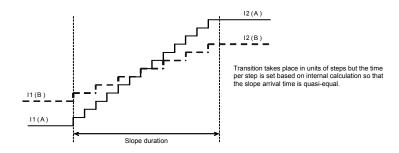
Current setting: I1 < I2



Current setting: I1 > I2



- Current difference in each channel (example)



# 9. Setting change in slope duration

A slope operation is performed by an internal sequencer.

When an attempt is made to change the setting in a slope duration, the active slope operation is reset and a newly set slope operation is restarted.

In this case, however, LED lighting stops for a maximum of 16.4ms (OSC frequency=typ) for synchronization with the internal clock until the operation is restarted.

### Description of other operations

### 1. Reset

There are two types of reset: software reset and hardware reset.

- (1) Software reset
  - Setting the register (SFTRST) to "1" causes all the registers to be initialized.
  - The registers subject to software reset automatically return to zero (Auto Return 0).

### (2) Hardware reset

- Changing the RESETB terminal setting from "H" to "L" causes a state subject to hardware reset.
- Attempting hardware reset causes the states of all registers and output terminals to be initialized to their initial values, so that address reception is entirely stopped.
- Attempting reset in the hardware reset state causes the RESETB terminal state to change from "L" to "H" and vice versa.
- The RESETB terminal is provided with a filter circuit and a duration of 5μs or less with the terminal set to "L" is not recognized as hardware reset.

### (3) Reset sequence

- When hardware reset is attempted during software reset, software reset is already cleared when hardware reset is cleared (because the software reset initial value is 0).

### 2. Thermal shutdown

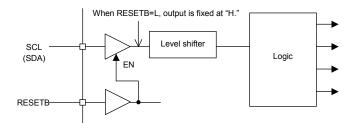
The thermal shutdown is effective for LED and OSC portions.

The thermal shutdown function is activated when the detected temperature is approx. 195°C.

The detected temperature has a hysteresis and the detection cancel temperature is approx. 175°C (reference value in design).

### 3. I/O portion

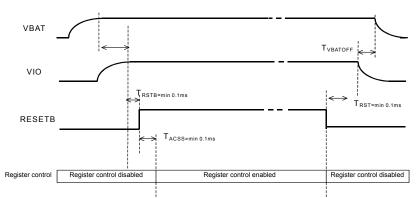
While the RESETB terminal is in "L" state, no input signal is propagated to the IC logic portion because SDA and SCL input buffer operations are all stopped.



Special care should be taken because a current path may be formed via a terminal protection diode, depending on an I/O power-on sequence or an input level.

### 4. Power on/off sequence

Voltage shall be applied as follows at driver activation. When a delay element is connected to a VIO voltage source and a reset cancel signal is input to the RESETB terminal, special care should be taken to the rising time of VIO voltage to delay the RESETB signal without fail.

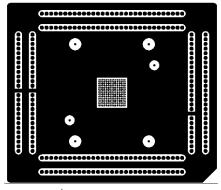


### 5. Terminating the unused terminals

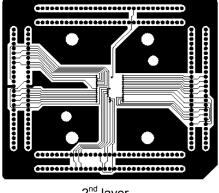
Be sure to set the test terminals and unused terminals as summarized in the following table. In addition, refer to the preceding equivalent circuit and terminate the above terminals in a way that no problem occurs during actual use.

procount	g oquitaionic on ouic and	terminate the above terminate in a may that he problem occare during actual						
	T1, T2, T3, T4	Test input terminals. Short-circuit these terminals to GND.						
LED terminals not to be used		Short-circuit these terminals to GND.						
LED (e)	minais not to be used	In this case, don't set the registers related to LEDs not to be used.						
RGB1C	RGB1CNT, RGB2CNT Short-circuit these terminals to GND.(Built-in pull-down resistance)							
CLKIO Short-circuit this terminal to GND.(Built-in pull-down resistance)								
ADDSEL Be sure to short-circuit this terminal to VBAT or GND.								

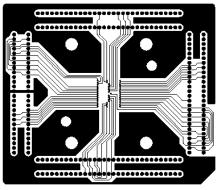
# ●PCB pattern of the Power dissipation measuring board



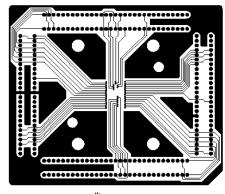
1<sup>st</sup> layer(component)



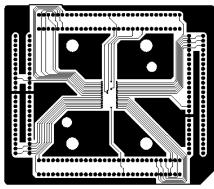
2<sup>nd</sup> layer



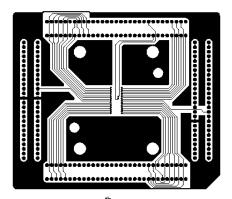
3<sup>rd</sup> layer



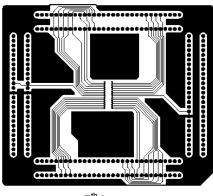
4<sup>th</sup> layer



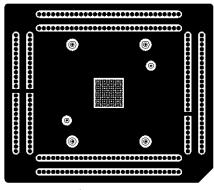
5<sup>th</sup> layer



6<sup>th</sup> layer



7<sup>th</sup> layer



8<sup>th</sup> layer (solder)

### Notes for Use

### (1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

### (2) Power supply and ground line

Design PCB pattern to provide low impedance for the wiring between the power supply and the ground lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and ground lines. Especially, when there are ground pattern for small signal and ground pattern for large current included the external circuits, please separate each ground pattern. Furthermore, for all power supply pins to ICs, mount a capacitor between the power supply and the ground pin. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

### (3) Ground voltage

Make setting of the potential of the ground pin so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no pins are at a potential lower than the ground voltage including an actual electric transient.

### (4) Short circuit between pins and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between pins or between the pin and the power supply or the ground pin, the ICs can break down.

### (5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

### (6) Input pins

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input pin. Therefore, pay thorough attention not to handle the input pins, such as to apply to the input pins a voltage lower than the ground respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input pins a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

### (7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

### (8) Thermal shutdown circuit (TSD)

This LSI builds in a thermal shutdown (TSD) circuit. When junction temperatures become detection temperature or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

### (9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

### (10) About the pin for the test, the un-use pin

Prevent a problem from being in the pin for the test and the un-use pin under the state of actual use. Please refer to a function manual and an application notebook. And, as for the pin that doesn't specially have an explanation, ask our company person in charge.

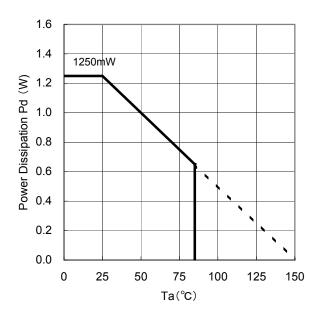
### (11) About the rush current

Because the rush current flows momentarily for internal logic instability caused by a power-on sequence or delay, special care should be taken to the power supply coupling capacity, power supply, ground pattern wiring width and wiring.

# (12) About descriptions given in this document

Though the function description and application node are design documents prepared for application design, we don't take liability for descriptions given in these documents. Be sure to decide applications after thoroughly investigating and evaluating the external devices as well as this BS2802GU LED driver.

# ●Power Dissipation (On the ROHM's standard board)



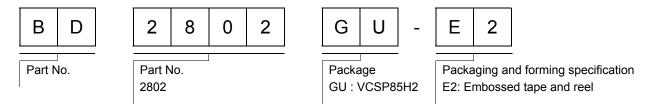
Information of the ROHM's standard board

Material: glass-epoxy

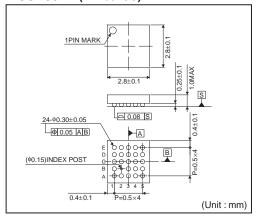
Size: 50mm×58mm×1.75mm (8Layer)

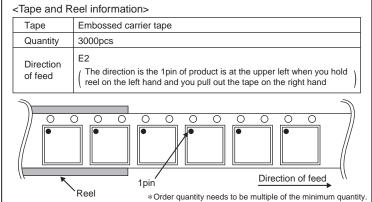
Pattern of the board: Refer to it that goes later.

# Ordering part number



# VCSP85H2 (BD2802GU)





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