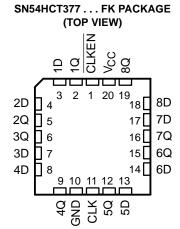
SCLS067D - NOVEMBER 1988 - REVISED MARCH 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 12 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Inputs Are TTL-Voltage Compatible

SN54HCT377 . . . J OR W PACKAGE SN74HCT377 . . . DW OR N PACKAGE (TOP VIEW)

CLKEN [1Q [1D [2D [2Q [3Q [3D [4D [1 2 3 4 5 6 7 8	20 19 18 17 16 15 14	V _{CC} 8Q 8D 7D 7Q 6Q 6D 5D
			Г

- Contain Eight Flip-Flops With Single-Rail Outputs
- Clock Enable Latched to Avoid False Clocking
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators



description/ordering information

These devices are positive-edge-triggered D-type flip-flops. The 'HCT377 devices are similar to the 'HCT273 devices, but feature a latched clock-enable (CLKEN) input instead of a common clear.

Information at the data (D) inputs meeting the <u>setup</u> time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse if <u>CLKEN</u> is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the <u>D</u> input has no effect at the output. These devices are designed to prevent false clocking by transitions at <u>CLKEN</u>.

ORDERING INFORMATION

TA	PACKAC	3E†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74HCT377N	SN74HCT377N
–40°C to 85°C	SOIC - DW	Tube	SN74HCT377DW	HCT377
	SOIC - DW	Tape and reel	SN74HCT377DWR	пстэтт
	CDIP – J	Tube	SNJ54HCT377J	SNJ54HCT377J
–55°C to 125°C	CFP – W	Tube	SNJ54HCT377W	SNJ54HCT377W
	LCCC – FK	Tube	SNJ54HCT377FK	SNJ54HCT377FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



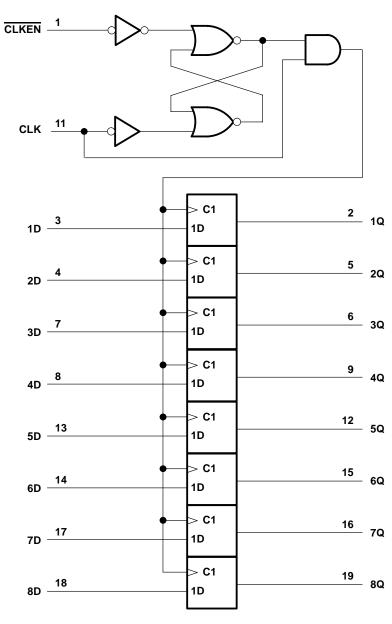
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FUNCTION TABLE (each flip-flop)

II	INPUTS							
CLKEN	CLK	D	Q					
Н	Х	Χ	Q_0					
L	\uparrow	Н	Н					
L	\uparrow	L	L					
Х	L	Χ	Q_0					

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ _{JA} (see Note 2): DW package	58°C/W
N package	69°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			SN54HCT377			SN74HCT377			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	\$ 5.5	4.5	5	5.5	V
VIH	High-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2	Į.	-/4	2			V
V _{IL}	Low-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		77.	0.8			0.8	V
٧ı	Input voltage		0	1	VCC	0		VCC	V
Vo	Output voltage		0	3	VCC	0		VCC	V
t _t	Input transition (rise and fall) times		O	7	500			500	ns
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		Vaa	Т	A = 25°C	;	SN54H	CT377	SN74HCT377		UNIT
PARAMETER	lesi co	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII	
Vo.,	\/ı = \/u \ or \/u	I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		V
Voн	VI = VIH or VIL	$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.30		3.7	3	3.84		٧
Voi	VI = VIH or VIL	I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
VOL	VI = VIH OI VIL	$I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	٧
lį	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100	′ ′ ′,	±1000		±1000	nA
ICC	$V_I = V_{CC}$ or 0,	IO = 0	5.5 V			8	$\mathcal{I}_{\eta_{\ell}}$	160		80	μΑ
Δl _{CC} ‡	One input at 0.5 V Other inputs at GN	,	5.5 V		1.4	2.4	704g	3		2.9	mA
C _i			4.5 V to 5.5 V		3	10		10*		10	pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

[‡]This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			Vaa	T _A = :	25°C	SN54H	CT377	SN74HCT377		UNIT
			VCC	MIN	MAX	MIN	MAX	MIN	MAX	UNII
f _{clock} Clock frequency			4.5 V		25		17		20	MHz
^f clock	Clock frequency		5.5 V		30		19		22	IVII IZ
t _W Pulse duration	CLK high or low	4.5 V	20		30	_	25		ns	
	CERTIIGH OF IOW	5.5 V	18		28		23		115	
	Output time to form OUT	Data	4.5 V	12		18	KE	15		ns
١.			5.5 V	10		17	Q	14		
t _{su}	Setup time before CLK↑	CLKEN high or low	4.5 V	12		18	`	15		
			5.5 V	10		17		14		
		Data	4.5 V	3		3		3		
 	Hold time data after CLK↑	Data	5.5 V	3		3		3		ns
t _h	HOW WITH WALA AILER CLK	OLIVEN in a division and division	4.5 V	5		5		5		
		CLKEN inactive or active	5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

				SN54HCT377						
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC	T _A = 25°C			MIN MAX	MAX	UNIT	
	(1141 01)	(0011 01)		MIN	TYP	MAX	NIIIA	IVIAA		
f			4.5 V	25	31	11.	4 17		MHz	
†max			5.5 V	30	37	9/5	19		IVIITZ	
	OLK	Δ	4.5 V		15	30		45		
¹рd	t _{pd} CLK Any		5.5 V		12	S 28		40	ns	
		Any	4.5 V		8	15		22	no	
t _t		Any	5.5 V		6	14		21	ns	

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

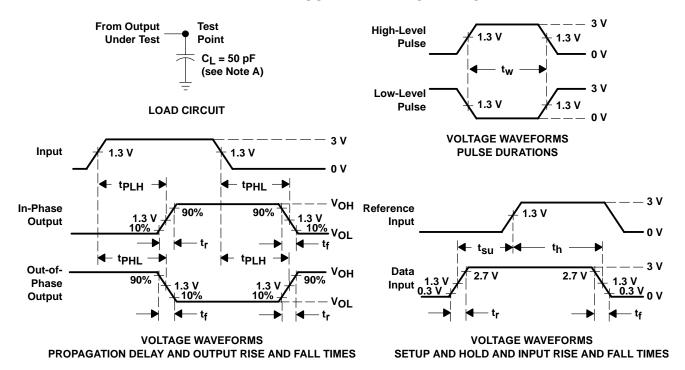
FROM TO		SN74HCT377							
PARAMETER	FROM (INPUT)	TO (OUTPUT)	Vcc	T _A = 25°C			MIN	MAX	UNIT
	(1141 01)			MIN	TYP	MAX	IVIIIV	IVIAA	
, 1	4.5 V	25	31		20		A 41 1-		
†max			5.5 V	30	37		22		MHz
	CLK	Any	4.5 V		15	30		38	no
^t pd	CLK	K Any	5.5 V		12	28		35	ns
+.		Λny	4.5 V		8	15		19	nc
t _t		Any	5.5 V		6	14		17	ns

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load	30	pF



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_f = 6 \ ns$, $t_f = 6 \ ns$.
- C. The outputs are measured one at a time with one input transition per measurement.
- D. For clock inputs, $f_{\mbox{max}}$ is measured when the input duty cycle is 50%.
- E. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms





MEN 15 .com 18-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74HCT377DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT377DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT377DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT377DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT377DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT377DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT377N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HCT377NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device			Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT377	DWR SC	OIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1





*All dimensions are nominal

ĺ	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
I	SN74HCT377DWR	SOIC	DW	20	2000	346.0	346.0	41.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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