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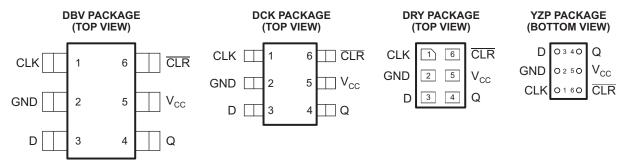
SCES560E-MARCH 2004-REVISED JUNE 2008

SINGLE D-TYPE FLIP-FLOP WITH ASYNCHRONOUS CLEAR

FEATURES

- Available in the Texas Instruments NanoFree[™] Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.3 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single D-type flip-flop is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G175 has an asynchronous clear (\overline{CLR}) input. When \overline{CLR} is high, data from the input pin (D) is transferred to the output pin (Q) on the clock's (CLK) rising edge. When \overline{CLR} is low, Q is forced into the low state, regardless of the clock edge or data on D.

NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.



ORDERING INFORMATION

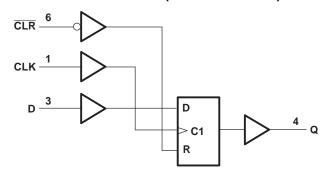
T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
	NanoFree™ - WCSP (DSBGA) 0.23-mm Large Bump - YZP (Pb-free)	Reel of 3000	SN74LVC1G175YZPR	D6_
	SON - DRY	Reel of 5000	SN74LVC1G175DRYR	D6_
-40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G175DBVR	C75
		Reel of 250	SN74LVC1G175DBVT	075_
	COT (CC 70) DCK	Reel of 3000	SN74LVC1G175DCKR	D6
	SOT (SC-70) – DCK	Reel of 250	SN74LVC1G175DCKT	D0_

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) DBV/DCK/DRY: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, = Pb-free).

FUNCTION TABLE

	INPUTS	OUTPUT	
CLR	CLK	D	Q
Н	1	L	L
Н	↑	Н	Н
Н	H or L	Χ	Q_{O}
L	X	X	L

LOGIC DIAGRAM (POSITIVE LOGIC)



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Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range		-0.5	6.5	V
Vo	Voltage range applied to any output in the hi	igh-impedance or power-off state ⁽²⁾	-0.5	6.5	V
Vo	Voltage range applied to any output in the hi	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-50	mA
lok	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current		±50	mA	
	Continuous current through V _{CC} or GND			±100	mA
		DBV package		165	
0	Dealers the arreal issue adapted (4)	DCK package		259	90/1/
θ_{JA}	Package thermal impedance ⁽⁴⁾	DRY package		234	°C/W
		YZP package		123	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed. The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
\/	Cumply yeltogo	Operating	1.65	5.5	V
V_{CC}	Supply voltage	Data retention only	1.5		V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
\ /	High lavel constructions	V_{CC} = 2.3 V to 2.7 V	1.7		V
V_{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
V	Low level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
VI	Input voltage	·	0	5.5	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-8	
I_{OH}	High-level output current	V 2.V		-16	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 4.5 V		-32	
		V _{CC} = 1.65 V		4	
		V _{CC} = 2.3 V		8	
I_{OL}	Low-level output current	V 0.V		16	mA
		V _{CC} = 3 V		24	
		V _{CC} = 4.5 V			
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		ns/V	
	·	V _{CC} = 5 V ± 0.5 V	10		
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION	NS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
	$I_{OH} = -100 \mu A$		1.65 V to 5.5 V	V _{CC} - 0.1			
	$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
V _{OH}	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V	
VOH	$I_{OH} = -16 \text{ mA}$	OH = -16 mA					V
	$I_{OH} = -24 \text{ mA}$	3 V	2.3				
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8				
	I _{OL} = 100 μA		1.65 V to 5.5 V			0.1	
	I _{OL} = 4 mA		1.65 V			0.45	
V	I _{OL} = 8 mA	I _{OL} = 8 mA				0.3	V
V _{OL}	I _{OL} = 16 mA		3 V			0.4	
	I _{OL} = 24 mA		3 V	0.55			
	I _{OL} = 32 mA		4.5 V			0.55	
I _I	V _I = 5.5 V or GND		0 to 5.5 V			±1	μΑ
I _{off}	V_I or $V_O = 5.5 \text{ V}$		0			±10	μΑ
I _{CC}	$V_I = 5.5 \text{ V or GND}, \qquad I_O =$	0	1.65 V to 5.5 V			10	μΑ
ΔI_{CC}	One input at V _{CC} - 0.6 V, Other	er inputs at V _{CC} or GND	3 V to 5.5 V			500	μΑ
C _i	V _I = V _{CC} or GND		3.3 V		3		pF

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

					V _{CC} = 1.8 V ±0.15 V		2.5 V ? V	V _{CC} = 3.3 V ±0.3 V		V _{CC} = 5 V ±0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency				100		125		150		175	MHz
	Dulas duration	CLR	Low	5.6		3		2.8		2.5		
t _w	Pulse duration	CLK	High or low	3.5		3		2.8		2.5		ns
	Catum times Instance OLIVA	Data	Data			2.5		2		1.5		
t _{su}	Setup time, before CLK↑ CLR inactive		0		0		0.5		0.5		ns	
t _h	Hold time, data after CLK	↑		0		0		0.5		0.5		ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ±0.1	1.8 V 5 V	V _{CC} = 2.5 V ±0.2 V		V _{CC} = 3.3 V ±0.3 V		V _{CC} = 5 V ±0.5 V		UNIT
	(INFOT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			100		125		150		175		MHz
4	CLK	Q	2.5	12.9	2	6.5	1.4	4.6	1	3	no
^L pd	CLR	· · ·	2.5	12.4	2	6	1.2	4.3	1	3.2	ns

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Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ±0.1	1.8 V 5 V		V _{CC} = 2.5 V ±0.2 V		3.3 V 3 V	V _{CC} = 5 V ±0.5 V		UNIT
	(INFOT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			100		125		150		175		MHz
+	CLK	0	2.7	13.4	2.2	7.1	1.6	5.7	1.5	4	20
t _{pd}	CLR	Q	2.7	12.9	2.2	7	1.5	5.8	1.3	4.1	ns

Operating Characteristics

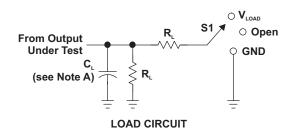
 $T_A = 25^{\circ}C$

	PARAMETER	TEST	V _{CC} = 1.8 V	$V_{CC} = 2.5 V$	$V_{CC} = 3.3 \text{ V}$	V _{CC} = 5 V	UNIT
	PARAMETER	CONDITIONS	TYP	TYP	TYP	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	18	19	19	21	pF

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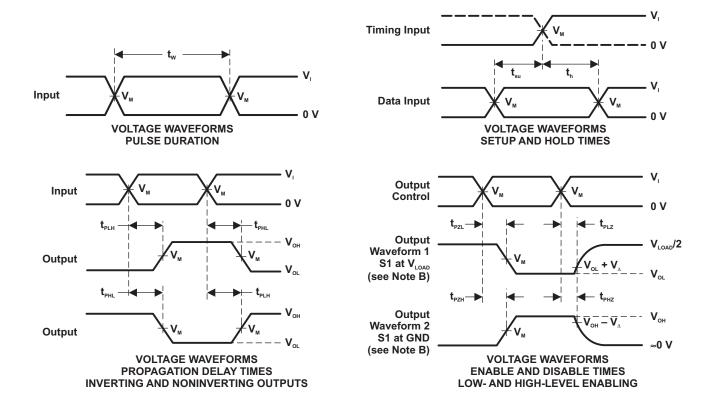


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t_{PLZ}/t_{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

.,	INPUTS			.,		-	.,
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C ^r	$R_{\scriptscriptstyle L}$	V _A
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.15 V
2.5 V ± 0.2 V	V_{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 M Ω	0.3 V
5 V ± 0.5 V	Vcc	≤2.5 ns	V _{cc} /2	2 × V	15 pF	1 Μ Ω	0.3 V



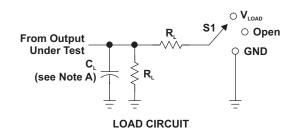
NOTES: A. C, includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{o} = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and \dot{t}_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. $t_{\mbox{\tiny PLH}}$ and $t_{\mbox{\tiny PHL}}$ are the same as $t_{\mbox{\tiny pd}}.$
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

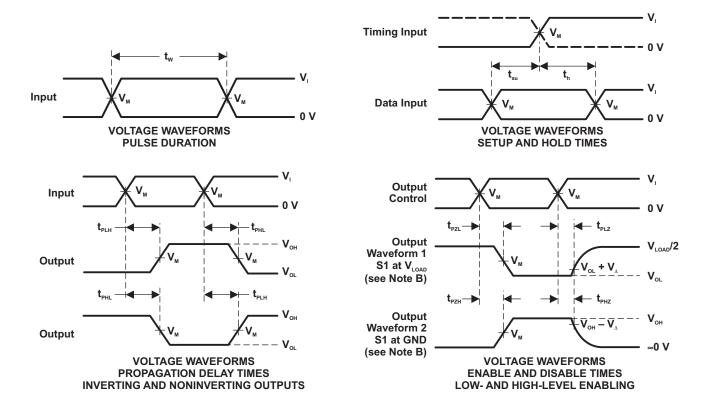


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t_{PLZ}/t_{PZL}	\mathbf{V}_{LOAD}
t _{PHZ} /t _{PZH}	GND

V	INPUTS		V	V		_	\ \ \	
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C ^r	R _⊾	V _A	
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V	
$2.5~V~\pm~0.2~V$	V_{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V	
$3.3 \text{ V} \pm 0.3 \text{ V}$	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	
5 V ± 0.5 V	V_{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V	



NOTES: A. C, includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{o} = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and \dot{t}_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. $t_{\mbox{\tiny PLH}}$ and $t_{\mbox{\tiny PHL}}$ are the same as $t_{\mbox{\tiny pd}}.$
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms







PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74LVC1G175DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G175DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G175DBVTE4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G175DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G175DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G175DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G175DCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G175DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G175DRYRG4	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G175DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G175DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G175DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G175DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G175DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G175YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



PACKAGE OPTION ADDENDUM

8-Dec-2008

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G175:

● Enhanced Product: SN74LVC1G175-EP

NOTE: Qualified Version Definitions:

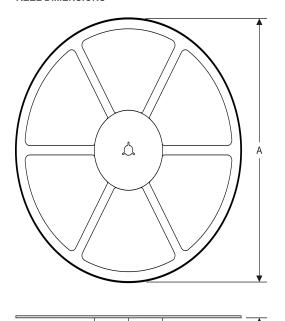
• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

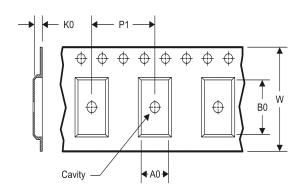
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G175DBVR	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G175DBVT	SOT-23	DBV	6	250	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G175DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G175DCKR	SC70	DCK	6	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
SN74LVC1G175DCKT	SC70	DCK	6	250	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
SN74LVC1G175DCKT	SC70	DCK	6	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G175DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G175YZPR	DSBGA	YZP	6	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G175DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G175DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
SN74LVC1G175DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G175DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1G175DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74LVC1G175DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC1G175DRYR	SON	DRY	6	5000	203.0	203.0	35.0
SN74LVC1G175YZPR	DSBGA	YZP	6	3000	220.0	220.0	34.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.



DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.



DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.





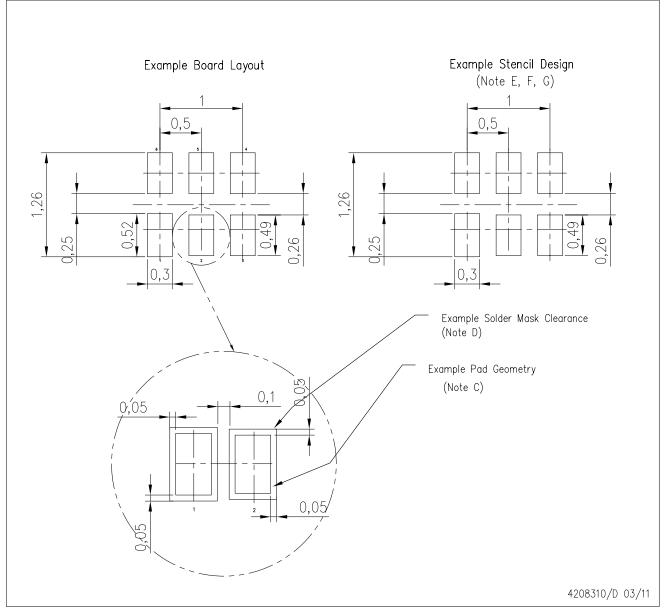
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.
- The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
- E. This package complies to JEDEC MO-287 variation UFAD.
- $frac{f}{K}$ See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.



DRY (S-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

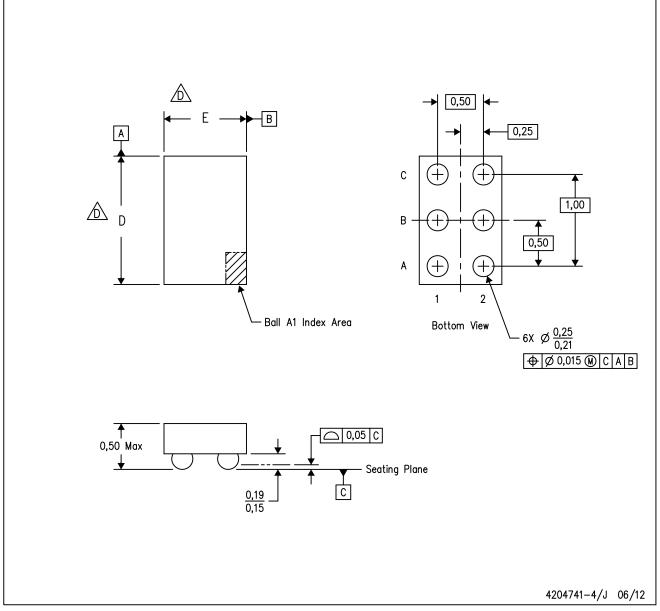


- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
- E. This package is a Pb-free solder ball design. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.



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