

## 1.2V to 3.6V, 12-Bit, Nanopower, 4-Wire Micro TOUCH SCREEN CONTROLLER with I<sup>2</sup>C™ Interface

Check for Samples: [TSC2007-Q1](#)

### FEATURES

- Qualified for Automotive Applications
- 4-Wire Touch Screen Interface
- Single 1.2 V to 3.6 V Supply/Reference
- Ratiometric Conversion
- Effective Throughput Rate:
  - Up to 20 kHz (8-Bit) or 10 kHz (12-Bit)
- Preprocessing to Reduce Bus Activity
- I<sup>2</sup>C Interface Supports:
  - Standard, Fast, and High-Speed Modes
- Simple, Command-Based User Interface:
  - [TSC2003-Q1](#) Compatible
  - 8- or 12-Bit Resolution
- On-Chip Temperature Measurement
- Touch Pressure Measurement
- Digital Buffered  $\overline{\text{PENIRQ}}$
- On-Chip, Programmable  $\overline{\text{PENIRQ}}$  Pull-Up
- Auto Power-Down Control
- Low Power:
  - 32.24  $\mu\text{A}$  at 1.2 V, Fast Mode, 8.2 kHz Eq Rate
  - 39.31  $\mu\text{A}$  at 1.8 V, Fast Mode, 8.2 kHz Eq Rate
  - 53.32  $\mu\text{A}$  at 2.7 V, Fast Mode, 8.2 kHz Eq Rate
- Enhanced ESD Protection:
  - $\pm 8$  kV HBM
  - $\pm 1$  kV CDM
  - $\pm 25$  kV Air Gap Discharge
  - $\pm 15$  kV Contact Discharge
- 5 x 6.4 TSSOP-16 Package

U.S. Patent NO. 6246394; other patents pending.

### APPLICATIONS

- Media Players
- Multiscreen Touch Control Systems

### DESCRIPTION

The TSC2007-Q1 is a very low-power touch screen controller designed to work with power-sensitive, handheld applications that are based on an advanced low-voltage processor. It works with a supply voltage as low as 1.2V, which can be supplied by a single-cell battery. It contains a complete, ultra-low power, 12-bit, analog-to-digital (A/D) resistive touch screen converter, including drivers and the control logic to measure touch pressure.

In addition to these standard features, the TSC2007-Q1 offers preprocessing of the touch screen measurements to reduce bus loading, thus reducing the consumption of host processor resources that can then be redirected to more critical functions.

The TSC2007-Q1 supports an I<sup>2</sup>C serial bus and data transmission protocol in all three defined modes: standard, fast, and high-speed. It offers programmable resolution of 8 or 12 bits to accommodate different screen sizes and performance needs.

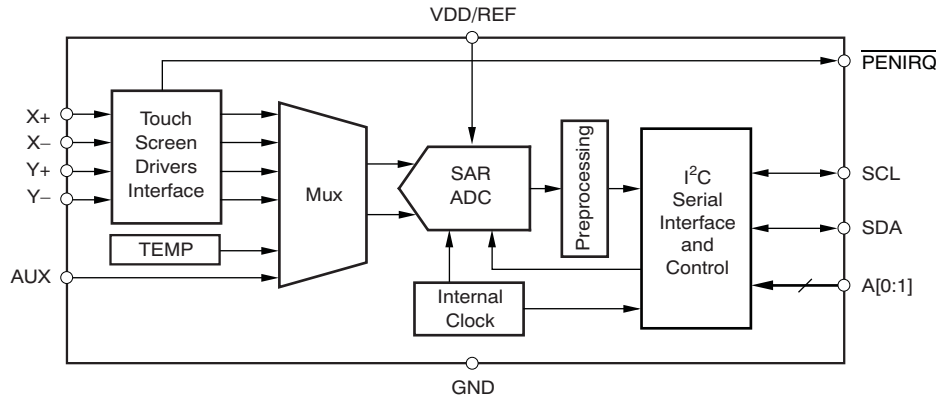
The TSC2007-Q1 is available in a 16-pin TSSOP package. The TSC2007-Q1 is characterized for the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  industrial temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

I<sup>2</sup>C is a trademark of NXP Semiconductors.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to +85°C	TSSOP – PW	Reel of 2000	TSC2007IPWRQ1	TS20071

- (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI website at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		VALUE	UNIT
Voltage	Analog input X+, Y+, AUX to GND	-0.4 to V <sub>DD</sub> + 0.1	V
	Analog input X-, Y- to GND	-0.4 to V <sub>DD</sub> + 0.1	V
Voltage range	VDD/REF pin to GND	-0.3 to +5	V
Digital input voltage to GND		-0.3 to V <sub>DD</sub> + 0.3	V
Digital output voltage to GND		-0.3 to V <sub>DD</sub> + 0.3	V
Power dissipation		(T <sub>J</sub> Max - T <sub>A</sub> )/θ <sub>JA</sub>	
Thermal impedance, θ <sub>JA</sub>	TSSOP package	86	°C/W
Operating free-air temperature range, T <sub>A</sub>		-40 to +85	°C
Storage temperature range, T <sub>STG</sub>		-65 to +150	°C
Junction temperature, T <sub>J</sub> Max		+150	°C
Lead temperature	Vapor phase (60 sec)	+215	°C
	Infrared (15 sec)	+220	°C
IEC contact discharge <sup>(2)</sup>	X+, X-, Y+, Y-	±15	kV
IEC air discharge <sup>(2)</sup>	X+, X-, Y+, Y-	±25	kV

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
- (2) Test method based on IEC standard 61000-4-2. Contact Texas Instruments for test details.

## ELECTRICAL CHARACTERISTICS

 At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = +1.2\text{V}$  to  $+3.6\text{V}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>AUXILIARY ANALOG INPUT</b>						
Input voltage range			0		$V_{DD}$	V
Input capacitance				12		pF
Input leakage current			-1		+1	$\mu\text{A}$
<b>A/D CONVERTER</b>						
Resolution		Programmable: 8 or 12 bits			12	Bits
No missing codes		12-bit resolution	11			Bits
Integral linearity				$\pm 1.5$		LSB <sup>(1)</sup>
Offset error		$V_{DD} = 1.8\text{V}$		-1.2		LSB
		$V_{DD} = 3.0\text{V}$		-3.1		LSB
Gain error		$V_{DD} = 1.8\text{V}$		0.7		LSB
		$V_{DD} = 3.0\text{V}$		0.1		LSB
<b>TOUCH SENSORS</b>						
$\overline{\text{PENIRQ}}$ pull-up resistor, $R_{\text{IRQ}}$		$T_A = +25^{\circ}\text{C}$ , $V_{DD} = 1.8\text{V}$ , command '1011' set '0000'		51		k $\Omega$
		$T_A = +25^{\circ}\text{C}$ , $V_{DD} = 1.8\text{V}$ , command '1011' set '0001'		90		k $\Omega$
Switch on-resistance	Y+, X+			6		$\Omega$
	Y-, X-			5		$\Omega$
Switch drivers drive current <sup>(2)</sup>		100ms duration			50	mA
<b>INTERNAL TEMPERATURE SENSOR</b>						
Temperature range			-40		+85	$^{\circ}\text{C}$
Resolution	Differential method <sup>(3)</sup>	$V_{DD} = 3\text{V}$		1.94		$^{\circ}\text{C}/\text{LSB}$
		$V_{DD} = 1.6\text{V}$		1.04		$^{\circ}\text{C}/\text{LSB}$
	TEMP1 <sup>(4)</sup>	$V_{DD} = 3\text{V}$		0.35		$^{\circ}\text{C}/\text{LSB}$
		$V_{DD} = 1.6\text{V}$		0.19		$^{\circ}\text{C}/\text{LSB}$
Accuracy	Differential method <sup>(3)</sup>	$V_{DD} = 3\text{V}$		$\pm 2$		$^{\circ}\text{C}/\text{LSB}$
		$V_{DD} = 1.6\text{V}$		$\pm 2$		$^{\circ}\text{C}/\text{LSB}$
	TEMP1 <sup>(4)</sup>	$V_{DD} = 3\text{V}$		$\pm 3$		$^{\circ}\text{C}/\text{LSB}$
		$V_{DD} = 1.6\text{V}$		$\pm 3$		$^{\circ}\text{C}/\text{LSB}$
<b>INTERNAL OSCILLATOR</b>						
Internal clock frequency, $f_{\text{CLK}}$	8-Bit	$V_{DD} = 1.2\text{V}$		3.19		MHz
		$V_{DD} = 1.8\text{V}$		3.66		MHz
		$V_{DD} = 2.7\text{V}$		3.78		MHz
		$V_{DD} = 3.6\text{V}$		3.82		MHz
	12-Bit	$V_{DD} = 1.2\text{V}$		1.6		MHz
		$V_{DD} = 1.8\text{V}$		1.83		MHz
		$V_{DD} = 2.7\text{V}$		1.88		MHz
		$V_{DD} = 3.6\text{V}$		1.91		MHz
Frequency drift	$V_{DD} = 1.6\text{V}$			0.0056		$\%/^{\circ}\text{C}$
	$V_{DD} = 3.0\text{V}$			0.012		$\%/^{\circ}\text{C}$

 (1) LSB means Least Significant Bit. With  $V_{DD}/\text{REF}$  pin =  $+1.6\text{V}$ , one LSB is  $391\ \mu\text{V}$ .

(2) Specified by design, but not tested. Exceeding 50 mA source current may result in device degradation.

(3) Difference between TEMP1 and TEMP2 measurement; no calibration necessary.

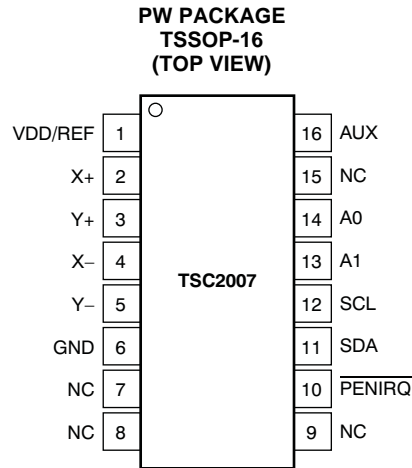
 (4) Temperature drift is  $-2.1\ \text{mV}/^{\circ}\text{C}$ .

**ELECTRICAL CHARACTERISTICS (continued)**At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = +1.2\text{V}$  to  $+3.6\text{V}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>DIGITAL INPUT/OUTPUT</b>							
Logic family				CMOS			
Logic level	$V_{IH}$	$1.2\text{V} \leq V_{DD} < 1.6\text{V}$		$0.7 \times V_{DD}$		$V_{DD} + 0.3$	V
		$1.6\text{V} \leq V_{DD} \leq 3.6\text{V}$		$0.7 \times V_{DD}$		$V_{DD} + 0.3$	V
	$V_{IL}$	$1.2\text{V} \leq V_{DD} < 1.6\text{V}$		-0.3		$0.2 \times V_{DD}$	V
		$1.6\text{V} \leq V_{DD} \leq 3.6\text{V}$		-0.3		$0.3 \times V_{DD}$	V
	$I_{IL}$	SCL and SDA pins		-1		1	$\mu\text{A}$
	$C_{IN}^{(5)}$	SCL and SDA pins				10	pF
	$V_{OH}$	$I_{OH} = 2$ TTL loads		$V_{DD} - 0.2$		$V_{DD}$	V
	$V_{OL}$	$I_{OL} = 2$ TTL loads		0		0.2	V
	$I_{LEAK}$	Floating output		-1		1	$\mu\text{A}$
$C_{OUT}^{(5)}$	Floating output				10	pF	
Data format				Straight binary			
<b>POWER-SUPPLY REQUIREMENTS</b>							
Power-supply voltage, $V_{DD}$		Specified performance		1.2		3.6	V
Quiescent supply current ( $V_{DD}$ with sensor off)	12-bit Fast mode (clock = 400kHz) PD[1:0] = 0,0	$V_{DD} = 1.2\text{V}$	32.56k eq rate		128	190	$\mu\text{A}$
			8.2k eq rate		32.24		$\mu\text{A}$
		$V_{DD} = 1.8\text{V}$	34.42k eq rate		165	240	$\mu\text{A}$
			8.2k eq rate		39.31		$\mu\text{A}$
		$V_{DD} = 2.7\text{V}$	34.79k eq rate		226.2	335	$\mu\text{A}$
			8.2k eq rate		53.32		$\mu\text{A}$
Power down supply current		Not addressed, SCL = SDA = 1			0	0.8	$\mu\text{A}$
<b>POWER ON/OFF SLOPE REQUIREMENTS<sup>(5)</sup></b>							
$V_{DD}$ off ramp		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		2			kV/s
$V_{DD}$ off time	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , $V_{DD} = 0\text{V}$			1.2			s
	$T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$ , $V_{DD} = 0\text{V}$			0.3			s
$V_{DD}$ on ramp		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		12			kV/s

(5) Not production tested. Specified by design.

## PIN CONFIGURATION



## PIN ASSIGNMENTS

PIN NO.	PIN NAME	I/O	A/D	DESCRIPTION
1	VDD/REF			Supply voltage and external reference input
2	X+	I	A	X+ channel input
3	Y+	I	A	Y+ channel input
4	X-	I	A	X- channel input
5	Y-	I	A	Y- channel input
6	GND			Ground
7	NC			No connection
8	NC			No connection
9	NC			No connection
10	$\overline{\text{PENIRQ}}$	O	D	Data available interrupt output. A delayed (process delay) pen touch detect. Pin polarity with active low.
11	SDA	I/O	D	Serial data I/O
12	SCL	I/O	D	Serial clock. This pin is normally an input, but acts as an output when the device stretches the clock to delay a bus transfer.
13	A1	I	D	Address input bit 1
14	A0	I	D	Address input bit 0
15	NC			No connection
16	AUX	I	A	Auxiliary channel input

## TIMING INFORMATION

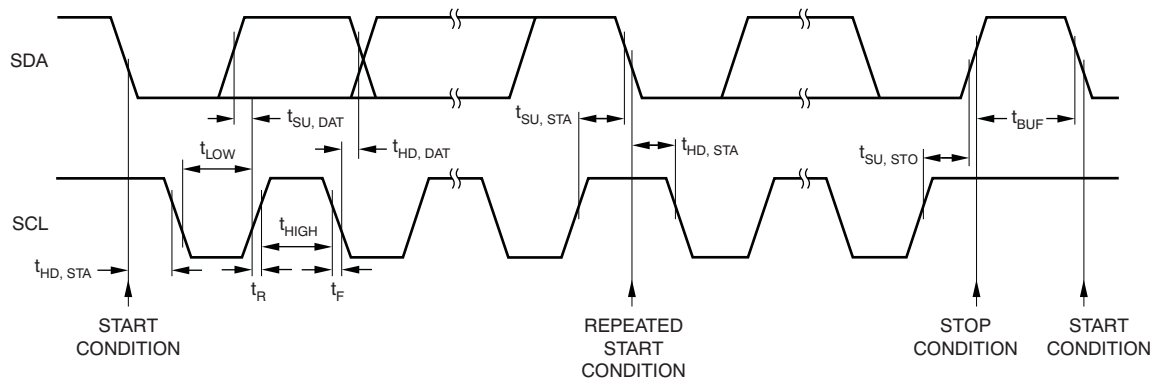


Figure 1. Detailed I/O Timing

### TIMING REQUIREMENTS: I<sup>2</sup>C Standard Mode (SCL = 100kHz)

All specifications typical at  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{DD}} = 1.6\text{V}$ , unless otherwise noted.

2-WIRE STANDARD MODE PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL clock frequency	$f_{\text{SCL}}$		0		100	kHz
Bus free time between a STOP and START condition	$t_{\text{BUF}}$		4.7			$\mu\text{s}$
Hold time (repeated) START condition	$t_{\text{HD, STA}}$		4.0			$\mu\text{s}$
Low period of SCL clock	$t_{\text{LOW}}$		4.7			$\mu\text{s}$
High period of the SCL clock	$t_{\text{HIGH}}$		4.0			$\mu\text{s}$
Setup time for a repeated START condition	$t_{\text{SU, STA}}$		4.7			$\mu\text{s}$
Data hold time	$t_{\text{HD, DAT}}$		0		3.45	$\mu\text{s}$
Data setup time	$t_{\text{SU, DAT}}$		250			ns
Rise time for both SDA and SCL signals (receiving)	$t_{\text{R}}$	$C_{\text{b}}$ = total bus capacitance			1000	ns
Fall time for both SDA and SCL signals (receiving)	$t_{\text{F}}$	$C_{\text{b}}$ = total bus capacitance			300	ns
Fall time for both SDA and SCL signals (transmitting)	$t_{\text{F}}$	$C_{\text{b}}$ = total bus capacitance			250	ns
Setup time for STOP condition	$t_{\text{SU, STO}}$		4.0			$\mu\text{s}$
Capacitive load for each bus line	$C_{\text{b}}$	$C_{\text{b}}$ = total capacitance of one bus line in pF			400	pF
Cycle time	8 bits	40 SCL + 127 CCLK, $V_{\text{DD}} = 1.8\text{V}$		434.7		$\mu\text{s}$
	12 bits	49 SCL + 148 CCLK, $V_{\text{DD}} = 1.8\text{V}$		570.9		$\mu\text{s}$
Effective throughput	8 bits	$V_{\text{DD}} = 1.8\text{V}$		2.3		kSPS
	12 bits	$V_{\text{DD}} = 1.8\text{V}$		1.75		kSPS
Equivalent rate = effective throughput $\times$ 7	8 bits	$V_{\text{DD}} = 1.8\text{V}$		16.1		kHz
	12 bits	$V_{\text{DD}} = 1.8\text{V}$		12.26		kHz

**TIMING REQUIREMENTS: I<sup>2</sup>C Fast Mode (SCL = 400kHz)**

 All specifications typical at –40°C to +85°C, V<sub>DD</sub> = 1.6V, unless otherwise noted.

2-WIRE FAST MODE PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL clock frequency	f <sub>SCL</sub>		0		400	kHz
Bus free time between a STOP and START condition	t <sub>BUF</sub>		1.3			μs
Hold time (repeated) START condition	t <sub>HD, STA</sub>		0.6			μs
Low period of SCL clock	t <sub>LOW</sub>		1.3			μs
High period of the SCL clock	t <sub>HIGH</sub>		0.6			μs
Setup time for a repeated START condition	t <sub>SU, STA</sub>		0.6			μs
Data hold time	t <sub>HD, DAT</sub>		0		0.9	μs
Data setup time	t <sub>SU, DAT</sub>		100			ns
Rise time for both SDA and SCL signals (receiving)	t <sub>R</sub>	C <sub>b</sub> = total bus capacitance	20+0.1×C <sub>b</sub>		300	ns
Fall time for both SDA and SCL signals (receiving)	t <sub>F</sub>	C <sub>b</sub> = total bus capacitance	20+0.1×C <sub>b</sub>		300	ns
Fall time for both SDA and SCL signals (transmitting)	t <sub>F</sub>	C <sub>b</sub> = total bus capacitance	20+0.1×C <sub>b</sub>		250	ns
Setup time for STOP condition	t <sub>SU, STO</sub>		0.6			μs
Capacitive load for each bus line	C <sub>b</sub>	C <sub>b</sub> = total capacitance of one bus line in pF			400	pF
Cycle time	8 bits	40 SCL + 127 CCLK, V <sub>DD</sub> = 1.8V		134.7		μs
	12 bits	49 SCL + 148 CCLK, V <sub>DD</sub> = 1.8V		203.4		μs
Effective throughput	8 bits	V <sub>DD</sub> = 1.8V		7.42		kSPS
	12 bits	V <sub>DD</sub> = 1.8V		4.92		kSPS
Equivalent rate = effective throughput × 7	8 bits	V <sub>DD</sub> = 1.8V		51.97		kHz
	12 bits	V <sub>DD</sub> = 1.8V		34.42		kHz

**TIMING REQUIREMENTS: I<sup>2</sup>C High-Speed Mode (SCL = 1.7MHz)**

 All specifications typical at –40°C to +85°C, V<sub>DD</sub> = 1.6V, unless otherwise noted.

2-WIRE HIGH-SPEED MODE PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL clock frequency	f <sub>SCL</sub>		0		1.7	MHz
Hold time (repeated) START condition	t <sub>HD, STA</sub>		160			ns
Low period of SCL clock	t <sub>LOW</sub>		320			ns
High period of the SCL clock	t <sub>HIGH</sub>		120			ns
Setup time for a repeated START condition	t <sub>SU, STA</sub>		160			ns
Data hold time	t <sub>HD, DAT</sub>		0		150	ns
Data setup time	t <sub>SU, DAT</sub>		10			ns
Rise time for SCL signal (receiving)	t <sub>R</sub>	C <sub>b</sub> = total bus capacitance	20		80	ns
Rise time for SDA signal (receiving)	t <sub>R</sub>	C <sub>b</sub> = total bus capacitance	20		160	ns
Fall time for SCL signal (receiving)	t <sub>F</sub>	C <sub>b</sub> = total bus capacitance	20		80	ns
Fall time for SDA signal (receiving)	t <sub>F</sub>	C <sub>b</sub> = total bus capacitance	20		160	ns
Fall time for both SDA and SCL signals (transmitting)	t <sub>F</sub>	C <sub>b</sub> = total bus capacitance	20		160	ns
Setup time for STOP condition	t <sub>SU, STO</sub>		160			ns
Capacitive load for each bus line	C <sub>b</sub>	C <sub>b</sub> = total capacitance of one bus line in pF			400	pF
Cycle time	8 bits	40 SCL + 127 CCLK, V <sub>DD</sub> = 1.8V		58.2		μs
	12 bits	49 SCL + 148 CCLK, V <sub>DD</sub> = 1.8V		109.7		μs
Effective throughput	8 bits	V <sub>DD</sub> = 1.8V		17.17		kSPS
	12 bits	V <sub>DD</sub> = 1.8V		9.12		kSPS
Equivalent rate = effective throughput × 7	8 bits	V <sub>DD</sub> = 1.8V		120.22		kHz
	12 bits	V <sub>DD</sub> = 1.8V		63.81		kHz

## TIMING REQUIREMENTS: I<sup>2</sup>C High-Speed Mode (SCL = 3.4MHz)

All specifications typical at –40°C to +85°C, V<sub>DD</sub> = 1.6V, unless otherwise noted.

2-WIRE HIGH-SPEED MODE PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL clock frequency	f <sub>SCL</sub>		0		3.4	MHz
Hold time (repeated) START condition	t <sub>HD, STA</sub>		160			ns
Low period of SCL clock	t <sub>LOW</sub>		160			ns
High period of the SCL clock	t <sub>HIGH</sub>		60			ns
Setup time for a repeated START condition	t <sub>SU, STA</sub>		160			ns
Data hold time	t <sub>HD, DAT</sub>		0		70	ns
Data setup time	t <sub>SU, DAT</sub>		10			ns
Rise time for SCL signal (receiving)	t <sub>R</sub>	C <sub>b</sub> = total bus capacitance	10		40	ns
Rise time for SDA signal (receiving)	t <sub>R</sub>	C <sub>b</sub> = total bus capacitance	10		80	ns
Fall time for SCL signal (receiving)	t <sub>F</sub>	C <sub>b</sub> = total bus capacitance	10		40	ns
Fall time for SDA signal (receiving)	t <sub>F</sub>	C <sub>b</sub> = total bus capacitance	10		80	ns
Fall time for both SDA and SCL signals (transmitting)	t <sub>F</sub>	C <sub>b</sub> = total bus capacitance	10		80	ns
Setup time for STOP condition	t <sub>SU, STO</sub>		160			ns
Capacitive load for each bus line	C <sub>b</sub>	C <sub>b</sub> = total capacitance of one bus line in pF			100	pF
Cycle time	8 bits	40 SCL + 127 CCLK, V <sub>DD</sub> = 1.8V		46.5		μs
	12 bits	49 SCL + 148 CCLK, V <sub>DD</sub> = 1.8V		95.3		μs
Effective throughput	8 bits	V <sub>DD</sub> = 1.8V		21.52		kSPS
	12 bits	V <sub>DD</sub> = 1.8V		10.49		kSPS
Equivalent rate = effective throughput × 7	8 bits	V <sub>DD</sub> = 1.8V		150.65		kHz
	12 bits	V <sub>DD</sub> = 1.8V		73.46		kHz



### TYPICAL CHARACTERISTICS

At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = +1.2\text{V}$  to  $+3.6\text{V}$ ,  $\text{PD1} = \text{PD0} = 0$ , Fast mode, 12-bit mode, non-continuous AUX measurement, and MAV filter enabled (see [MAV Filter](#) section), unless otherwise noted.

**POWER-DOWN SUPPLY CURRENT  
vs  
TEMPERATURE**

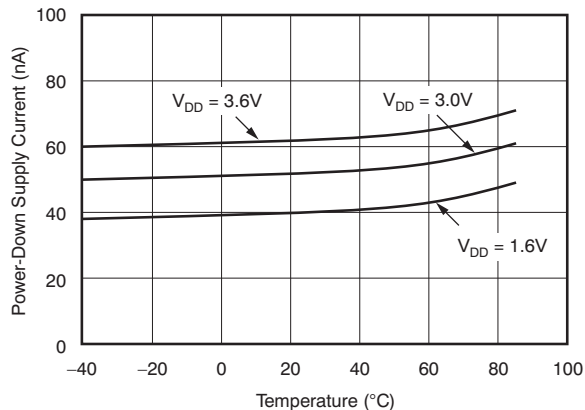


Figure 2.

**SUPPLY CURRENT  
vs  
TEMPERATURE**

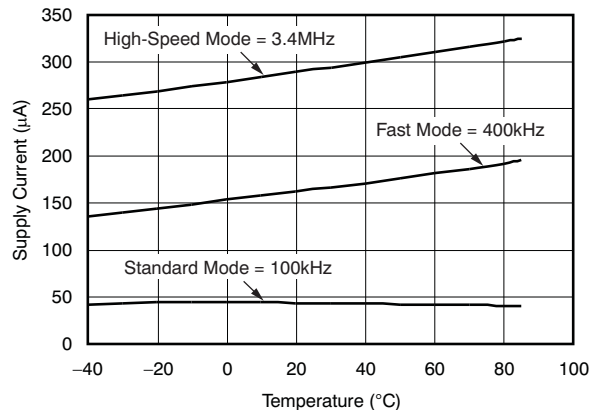


Figure 3.

**SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE  
(AUX Conversion)**

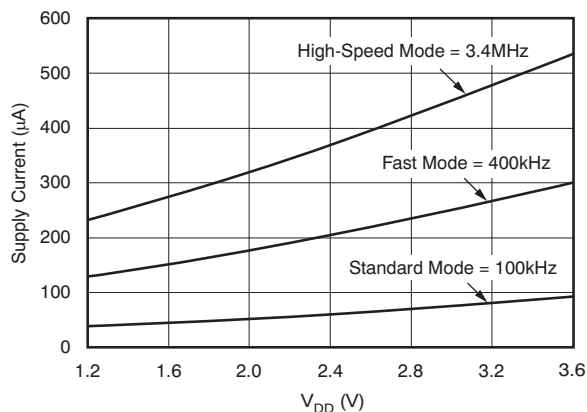


Figure 4.

**SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE**

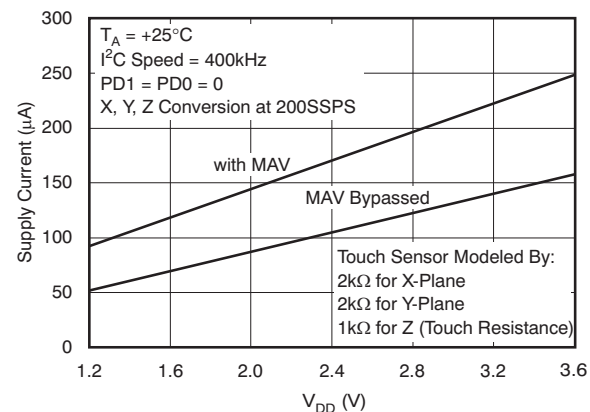


Figure 5.

### TYPICAL CHARACTERISTICS (continued)

At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = +1.2\text{V}$  to  $+3.6\text{V}$ ,  $\text{PD1} = \text{PD0} = 0$ , Fast mode, 12-bit mode, non-continuous AUX measurement, and MAV filter enabled (see [MAV Filter](#) section), unless otherwise noted.

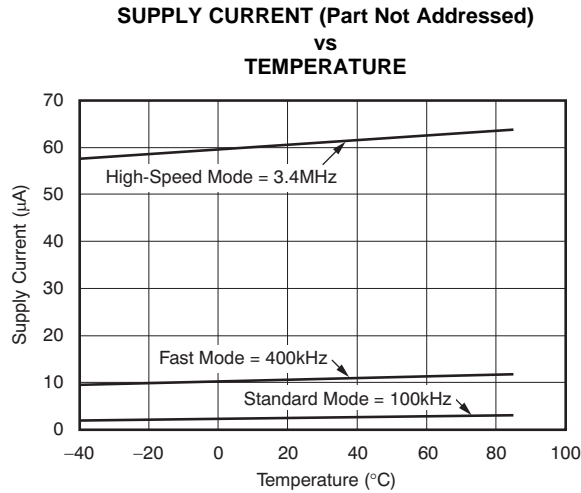


Figure 6.

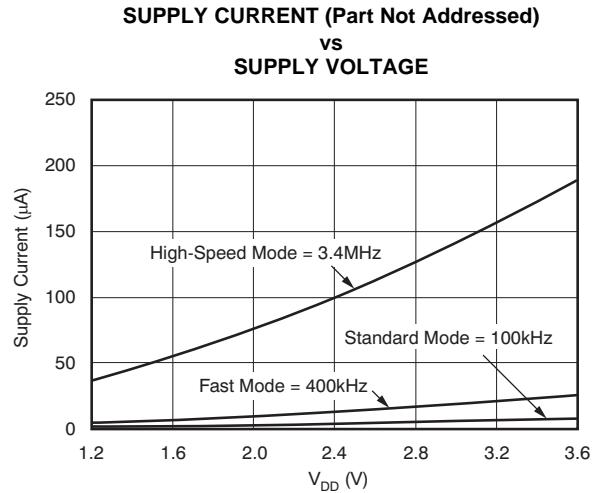


Figure 7.

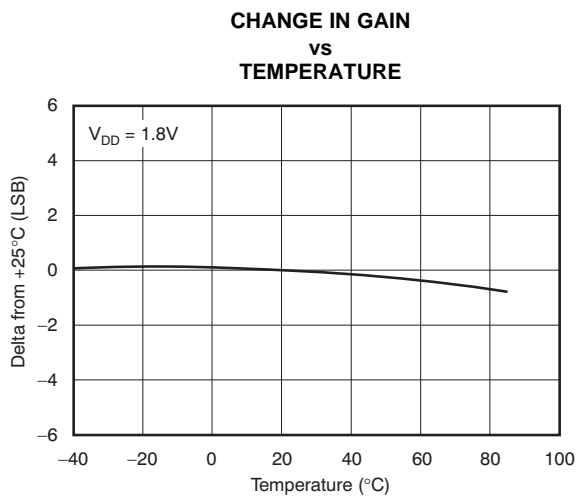


Figure 8.

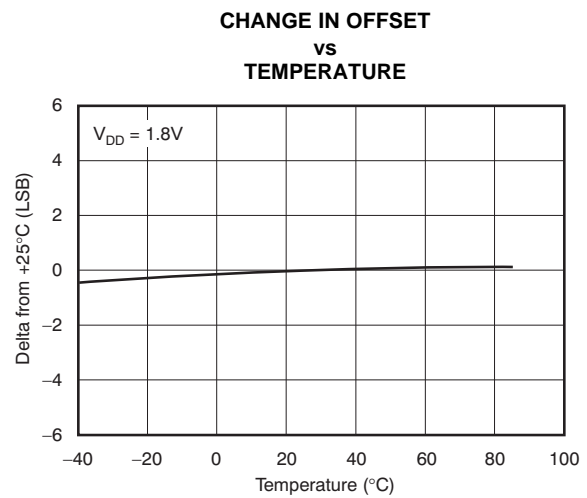
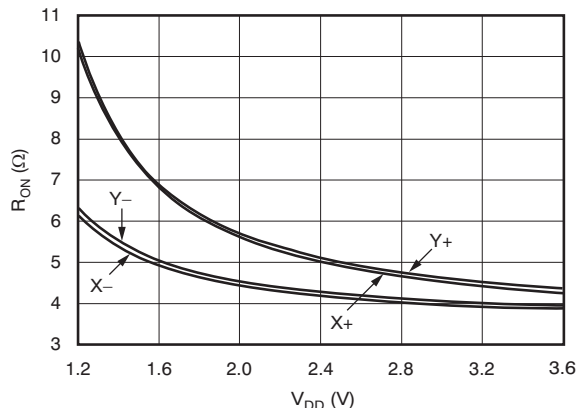


Figure 9.

**TYPICAL CHARACTERISTICS (continued)**

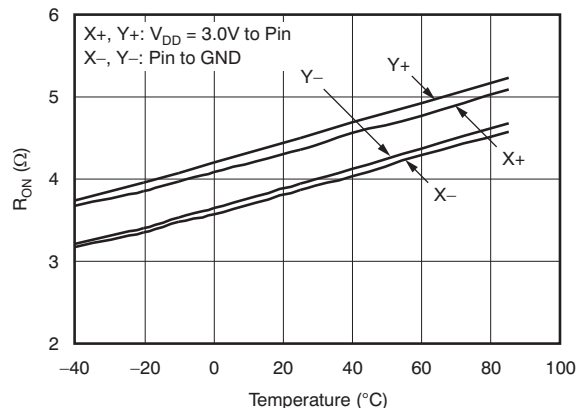
At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = +1.2\text{V}$  to  $+3.6\text{V}$ ,  $\text{PD1} = \text{PD0} = 0$ , Fast mode, 12-bit mode, non-continuous AUX measurement, and MAV filter enabled (see MAV Filter section), unless otherwise noted.

**SWITCH ON-RESISTANCE  
vs  
SUPPLY VOLTAGE**



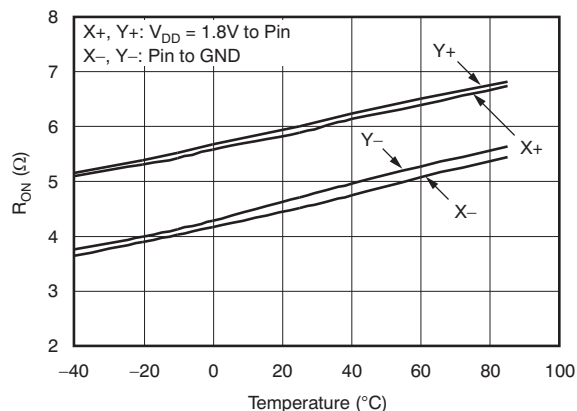
**Figure 10.**

**SWITCH ON-RESISTANCE  
vs  
TEMPERATURE**



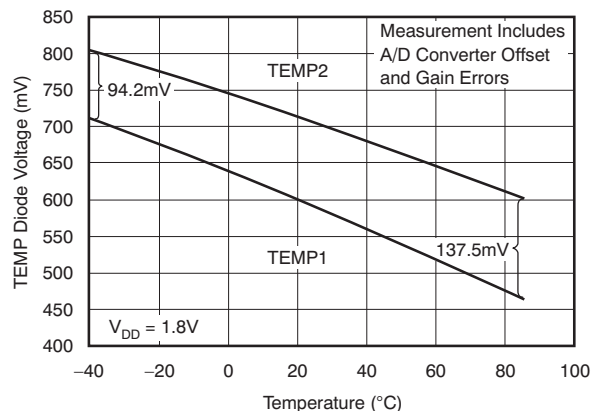
**Figure 11.**

**SWITCH ON-RESISTANCE  
vs  
TEMPERATURE**



**Figure 12.**

**TEMP DIODE VOLTAGE  
vs  
TEMPERATURE**



**Figure 13.**

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = +1.2\text{V}$  to  $+3.6\text{V}$ ,  $\text{PD1} = \text{PD0} = 0$ , Fast mode, 12-bit mode, non-continuous AUX measurement, and MAV filter enabled (see [MAV Filter](#) section), unless otherwise noted.

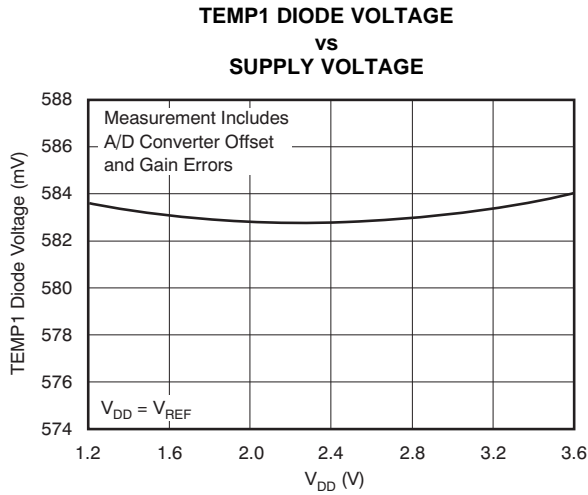


Figure 14.

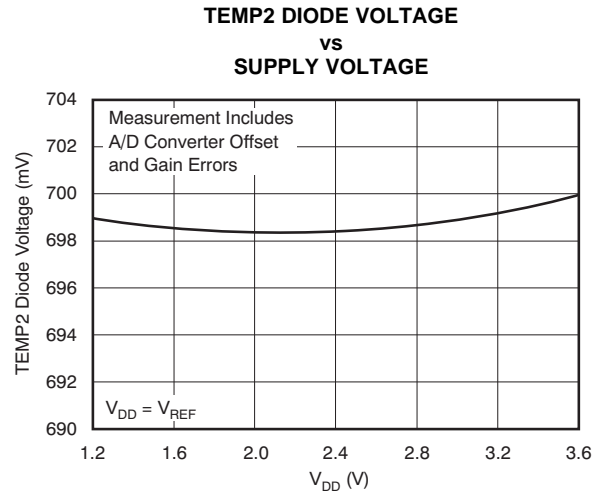


Figure 15.

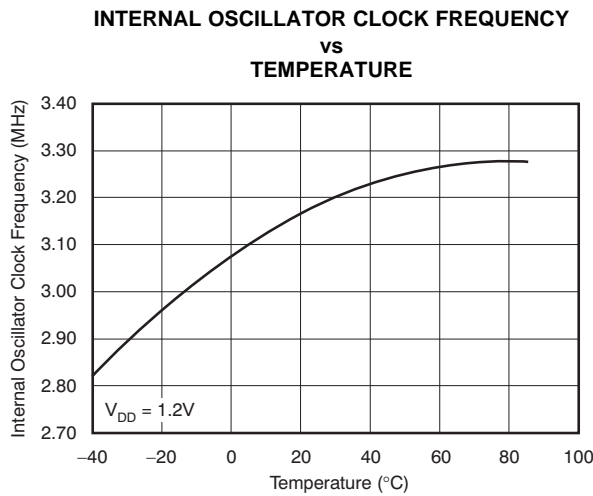


Figure 16.

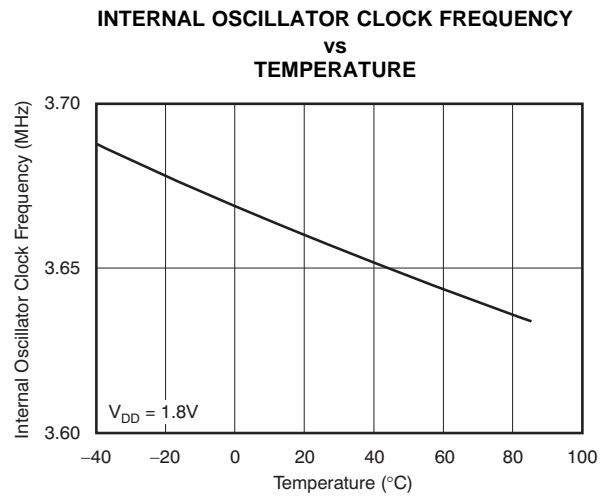


Figure 17.

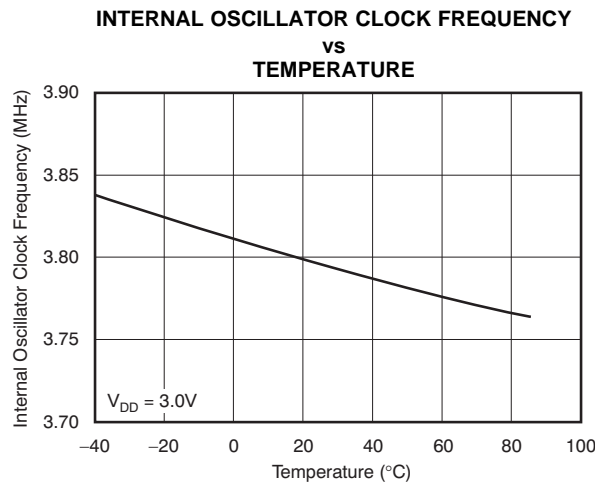


Figure 18.

## OVERVIEW

The TSC2007-Q1 is an analog interface circuit for a human interface touch screen device. All peripheral functions are controlled through the command byte and onboard state machines. The TSC2007-Q1 features include:

- Very low-power touch screen controller
- Very small onboard footprint
- Relieves host from tedious routine tasks by preprocessing, thus saving resources for more critical tasks
- Ability to work on very low supply voltage
- Minimal connection interface allows easiest isolation and reduces the number of dedicated I/O pins required
- Miniature, yet complete; requires no external supporting component
- Enhanced electrostatic discharge (ESD) protection

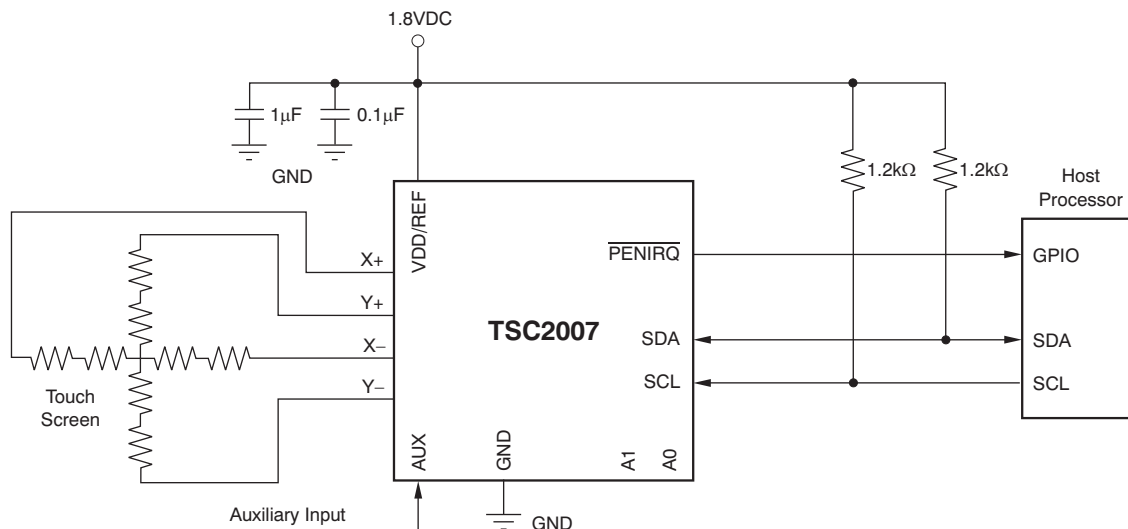
The TSC2007-Q1 consists of the following blocks (refer to the [block diagram](#) on the front page):

- Touch Screen Sensor Interface
- Auxiliary Input (AUX)
- Temperature Sensor
- Acquisition Activity Preprocessing
- Internal Conversion Clock
- I<sup>2</sup>C Interface

Communication with the TSC2007-Q1 is done via an I<sup>2</sup>C serial interface. The TSC2007-Q1 is an I<sup>2</sup>C slave device; therefore, data are shifted into or out of the TSC2007-Q1 under control of the host microprocessor, which also provides the serial data clock.

Control of the TSC2007-Q1 and its functions is accomplished by writing to the command register of an internal state machine. A simple command protocol compatible with I<sup>2</sup>C is used to address this register.

A typical application of the TSC2007-Q1 is shown in [Figure 19](#).



**Figure 19. Typical Circuit Configuration**

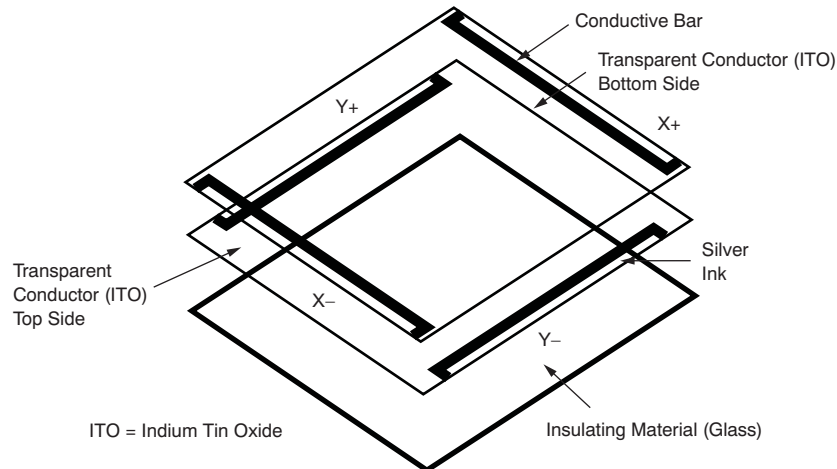
## TOUCH SCREEN OPERATION

A resistive touch screen operates by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix where the screen is touched by an input (stylus, pen, or finger). The change in the resistance ratio marks the location on the touch screen.

The TSC2007-Q1 supports resistive 4-wire configurations, as shown in [Figure 20](#). The circuit determines location in two coordinate pair dimensions, although a third dimension can be added for measuring pressure.

### 4-WIRE TOUCH SCREEN COORDINATE PAIR MEASUREMENT

A 4-wire touch screen is typically constructed as shown in [Figure 20](#). It consists of two transparent resistive layers separated by insulating spacers.



**Figure 20. 4-Wire Touch Screen Construction**

The 4-wire touch screen panel works by applying a voltage across the vertical or horizontal resistive network. The A/D converter converts the voltage measured at the point where the panel is touched. A measurement of the Y position of the pointing device is made by connecting the X+ input to a data converter chip, turning on the Y+ and Y– drivers, and digitizing the voltage seen at the X+ input. The voltage measured is determined by the voltage divider developed at the point of touch. For this measurement, the horizontal panel resistance in the X+ lead does not affect the conversion because of the high input impedance of the A/D converter.

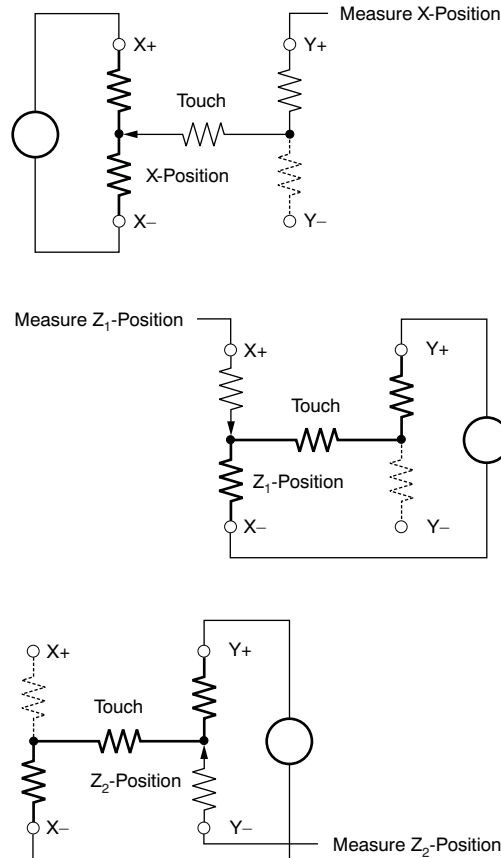
Voltage is then applied to the other axis, and the A/D converter converts the voltage representing the X position on the screen. This process provides the X and Y coordinates to the associated processor.

Measuring touch pressure (Z) can also be done with the TSC2007-Q1. To determine pen or finger touch, the pressure of the *touch* must be determined. Generally, it is not necessary to have very high performance for this test; therefore, 8-bit resolution mode may be sufficient (however, data sheet calculations are shown using the 12-bit resolution mode). There are several different ways of performing this measurement. The TSC2007-Q1 supports two methods. The first method requires knowing the X-plate resistance, the measurement of the X-position, and two additional cross panel measurements ( $Z_2$  and  $Z_1$ ) of the touch screen (see [Figure 21](#)). [Equation 1](#) calculates the touch resistance:

$$R_{\text{TOUCH}} = R_{X\text{-plate}} \cdot \frac{X_{\text{Position}}}{4096} \left( \frac{Z_2}{Z_1} - 1 \right) \quad (1)$$

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-position and Y-position, and  $Z_1$ . Equation 2 also calculates the touch resistance:

$$R_{\text{TOUCH}} = \frac{R_{X\text{-plate}} \cdot X_{\text{Position}}}{4096} \left( \frac{4096}{Z_1} - 1 \right) - R_{Y\text{-plate}} \cdot \left( 1 - \frac{Y_{\text{Position}}}{4096} \right) \quad (2)$$



**Figure 21. Pressure Measurement**

When the touch panel is pressed or touched and the drivers to the panel are turned on, the voltage across the touch panel often overshoots and then slowly settles down (decays) to a stable dc value. This effect is a result of mechanical bouncing caused by vibration of the top layer sheet of the touch panel when the panel is pressed. This settling time must be accounted for, or else the converted value is incorrect. Therefore, a delay must be introduced between the time the driver for a particular measurement is turned on, and the time a measurement is made.

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (for example, noise generated by the LCD panel or back-light circuitry). The value of these capacitors provides a low-pass filter to reduce the noise, but creates an additional settling time requirement when the panel is touched. The settling time typically shows up as gain error.

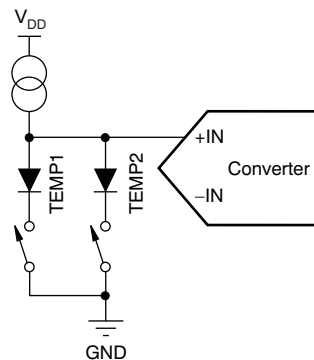
To solve this problem, the TSC2007-Q1 can be commanded to turn on the drivers only, without performing a conversion. Time can then be allowed to perform a conversion before the command is issued.

The TSC2007-Q1 touch screen interface can measure position (X,Y) and pressure (Z).

## INTERNAL TEMPERATURE SENSOR

In some applications, such as battery recharging, an ambient temperature measurement is required. The temperature measurement technique used in the TSC2007-Q1 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage ( $V_{BE}$ ) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the +25°C value of the  $V_{BE}$  voltage and then monitoring the delta of that voltage as the temperature changes.

The TSC2007-Q1 offers two modes of temperature measurement. The first mode requires calibration at a known temperature, but only requires a single reading to predict the ambient temperature. The TEMP1 diode, shown in Figure 22, is used during this measurement cycle. This voltage is typically 580mV at +25°C with a 10µA current. The absolute value of this diode voltage can vary by a few millivolts; the temperature coefficient ( $T_C$ ) of this voltage is very consistent at  $-2.1\text{mV}/^\circ\text{C}$ . During the final test of the end product, the diode voltage would be stored at a known room temperature, in system memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of  $0.35^\circ\text{C}/\text{LSB}$  (1LSB =  $732\mu\text{V}$  with  $V_{REF} = 3.0\text{V}$ ).



**Figure 22. Functional Block Diagram of Temperature Measurement Mode**

The second mode does not require a test temperature calibration, but uses a two-measurement (differential) method to eliminate the need for absolute temperature calibration and for achieving  $2^\circ\text{C}/\text{LSB}$  accuracy. This mode requires a second conversion of the voltage across the TEMP2 diode with a resistance 91 times larger than the TEMP1 diode. The voltage difference between the first (TEMP1) and second (TEMP2) conversion is represented by:

$$\Delta V = \frac{kT}{q} \cdot \ln(N) \quad (3)$$

Where:

$N$  = the resistance ratio = 91.

$k$  = Boltzmann's constant =  $1.3807 \times 10^{-23}$  J/K (joules/kelvins).

$q$  = the electron charge =  $1.6022 \times 10^{-19}$  C (coulombs).

$T$  = the temperature in kelvins (K).

This method can provide a much improved absolute temperature measurement, but a lower resolution of  $1.6^\circ\text{C}/\text{LSB}$ . The resulting equation to solve for  $T$  is:

$$T = \frac{q \cdot \Delta V}{k \cdot \ln(N)} \quad (4)$$

Where:

$\Delta V = V_{BE}(\text{TEMP2}) - V_{BE}(\text{TEMP1})$  (in mV)

$\therefore T = 2.573 \cdot \Delta V$  (in K)

or  $T = 2.573 \cdot \Delta V - 273$  (in  $^\circ\text{C}$ )

Temperature 1 and temperature 2 measurements have the same timing as the other data acquisition cycles shown in Figure 33 and Figure 34.



### ANALOG-TO-DIGITAL CONVERTER

Figure 23 shows the analog inputs of the TSC2007-Q1. The analog inputs (X, Y, and Z touch panel coordinates, chip temperature and auxiliary inputs) are provided via a multiplexer to the Successive Approximation Register (SAR) A/D converter. The A/D architecture is based on capacitive redistribution architecture, which inherently includes a sample-and-hold function.

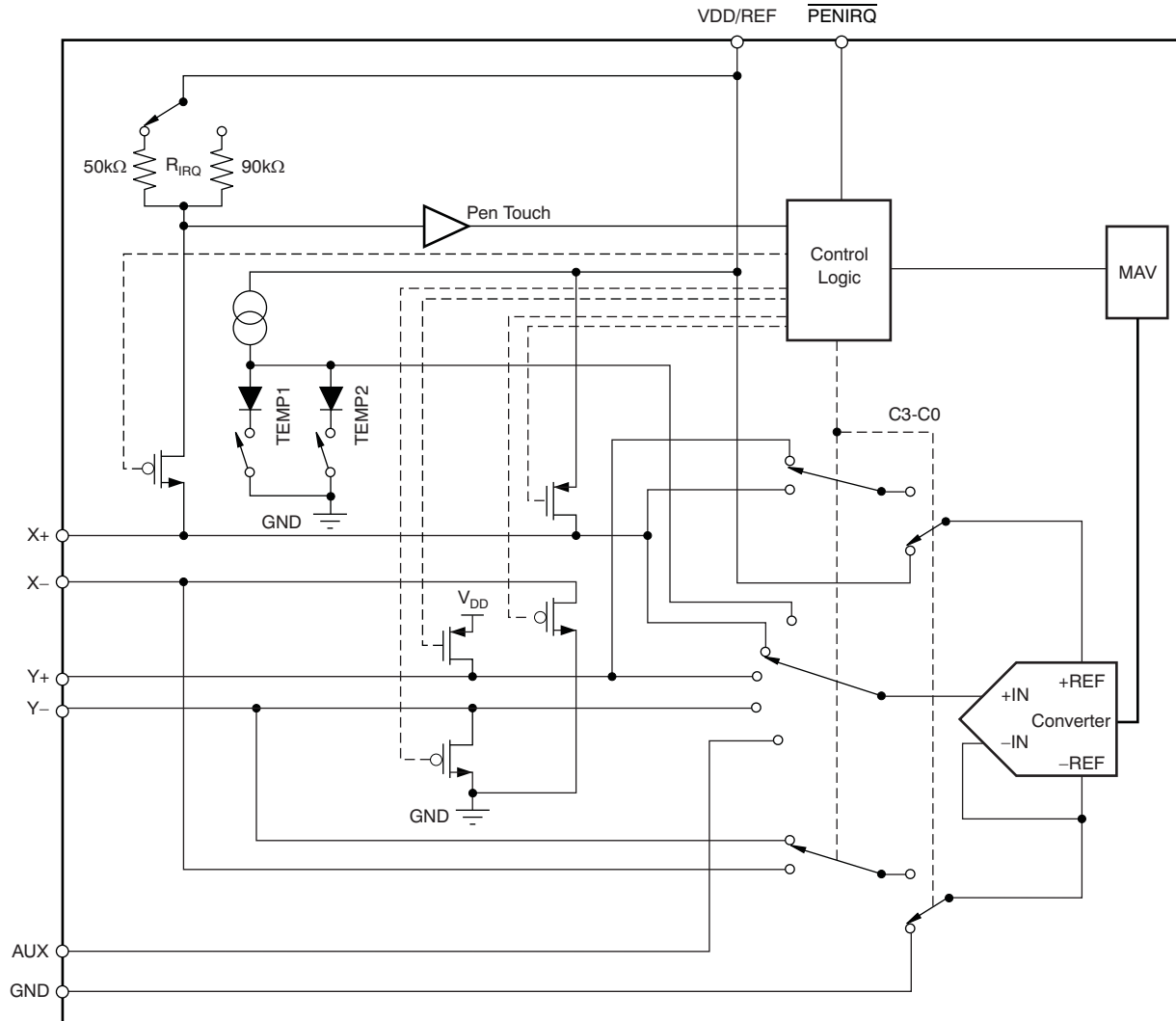


Figure 23. Analog Input Section (Simplified Diagram)

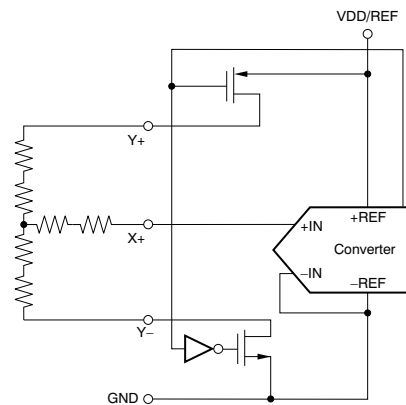
A unique configuration of low on-resistance switches allows an unselected A/D converter input channel to provide power and an accompanying pin to provide ground for driving the touch panel. By maintaining a differential input to the converter and a differential reference input architecture, it is possible to negate errors caused by the driver switch on-resistance.

## Reference

The TSC2007-Q1 uses an external voltage reference that is applied to the VDD/REF pin. The upper reference voltage range is the same as the supply voltage range, which allows for simple, 1.2V to 3.6V, single-supply operation of the chip.

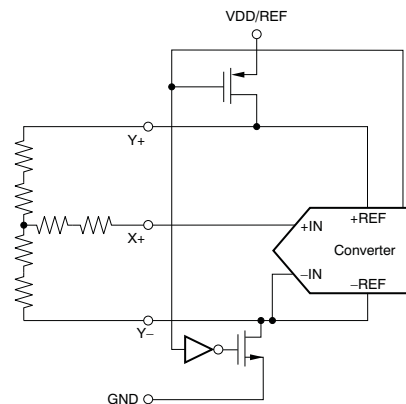
## Reference Mode

There is a critical item regarding the reference when making measurements while the switch drivers are on. For this discussion, it is useful to consider the basic operation of the TSC2007-Q1 (see [Figure 19](#)). The application used in the following example shows the device being used to digitize a resistive touch screen. If the touch screen controller uses a single-ended reference mode, as shown in [Figure 24](#), a measurement of the current Y position of the pointing device is made by connecting the X+ input to the A/D converter, turning on the Y+ and Y– drivers, and digitizing the voltage on X+. For this measurement, the resistance in the X+ lead does not affect the conversion; it does affect the settling time, but the resistance is usually small enough that this timing is not a concern. However, because the resistance between Y+ and Y– is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it would not be possible to achieve a 0V input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error. Therefore, the TSC2007-Q1 does not support single-ended reference mode.



**Figure 24. Simplified Diagram of Single-Ended Reference**

This situation is resolved, as shown in [Figure 25](#), by using the differential mode; the +REF and –REF inputs are connected directly to Y+ and Y–, respectively. This mode makes the A/D converter ratiometric. The result of the conversion is always a percentage of the external reference, regardless of how it changes in relation to the on-resistance of the internal switches.



**Figure 25. Simplified Diagram of Differential Reference  
(Both Y Switches Enabled, X+ is Analog Input)**



## Touch Detect

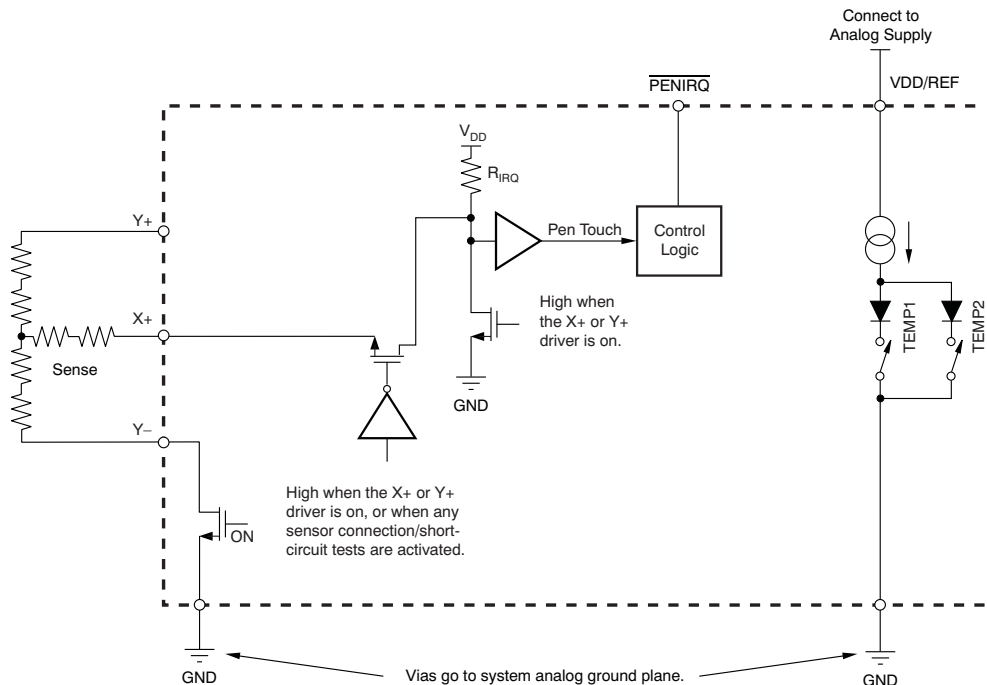
The  $\overline{\text{PENIRQ}}$  can be used as an interrupt to the host.  $R_{\text{IRQ}}$  is an internal pull-up resistor with a programmable value of either 50k $\Omega$  (default) or 90k $\Omega$ . Write command '1011' (setup command) followed by data '0001' sets the pull-up to 90k $\Omega$ . **NOTE:** The first three bits must be '0's and the select bit is the last bit. To change the pull-up back to 50k $\Omega$ , issue write command '1011' followed by data '0000'.

An example for the Y-position measurement is detailed in Figure 27. The  $\overline{\text{PENIRQ}}$  output is pulled high by an internal pull-up. While in power-down mode with  $\text{PD0} = 0$ , the Y- driver is on and connected to GND, and the  $\overline{\text{PENIRQ}}$  output is connected to the X+ input. When the panel is touched, the X+ input is pulled to ground through the touch screen, and the  $\overline{\text{PENIRQ}}$  output goes low because of the current path through the panel to GND, initiating an interrupt to the processor. During the measurement cycle for X-, Y-, and Z-position, the X+ input is disconnected from the  $\overline{\text{PENIRQ}}$  pull-down transistor to eliminate any pull-up resistor leakage current from flowing through the touch screen, thus causing no errors.

In addition to the measurement cycles for X-, Y-, and Z-position, commands that activate the X-drivers, Y-drivers, and Y+ and X-drivers without performing a measurement also disconnect the X+ input from the  $\overline{\text{PENIRQ}}$  pull-down transistor, and disable the pen-interrupt output function, regardless of the value of the  $\text{PD0}$  bit. Under these conditions, the  $\overline{\text{PENIRQ}}$  output is forced low. Furthermore, if the last command byte written to the TSC2007-Q1 contains  $\text{PD0} = 1$ , the pen-interrupt output function is disabled and cannot detect when the panel is touched. In order to re-enable the pen-interrupt output function under these circumstances, a command byte must be written to the TSC2007-Q1 with  $\text{PD0} = 0$ .

When the bus master sends the address byte with the  $\overline{\text{R/W}}$  bit = 0, and the TSC2007-Q1 sends an acknowledge, the pen-interrupt function is disabled. If the command that follows the address byte contains  $\text{PD0} = 0$ , then the pen-interrupt function is enabled at the end of a conversion. This action is approximately 100 $\mu\text{s}$  (12-bit mode) or 50 $\mu\text{s}$  (8-bit mode) after the TSC2007-Q1 receives a STOP/START condition, following the receipt of a command byte (see Figure 31 and Figure 30 for further details about when the conversion cycle begins).

In both cases previously listed, it is recommended that whenever the host writes to the TSC2007-Q1, the master processor masks the interrupt associated to  $\overline{\text{PENIRQ}}$ . This masking prevents false triggering of interrupts when the  $\overline{\text{PENIRQ}}$  line is disabled in the cases previously listed.



**Figure 27. Example of a Pen-Touch Induced Interrupt via the  $\overline{\text{PENIRQ}}$  Pin**

## Preprocessing

The TSC2007-Q1 has a combined MAV filter (median value filter and averaging filter).

### MAV Filter

If the acquired signal source is noisy because of the digital switching circuit, it may necessary to evaluate the data without noise. In this case, the median value filter operation helps remove the *noise*. The array of seven converted results is sorted first. The middle three values are then averaged to produce the output value of the MAV filter.

The MAV filter is applied to all measurements for all analog inputs including the touch screen inputs, temperature measurements TEMP1 and TEMP2, and auxiliary input AUX. To shorten the conversion time, the MAV filter may be bypassed through the setup command; see [Table 3](#) and [Table 4](#).



**Figure 28. MAV Filter Operation (Patent Pending)**

## I<sup>2</sup>C INTERFACE

The TSC2007-Q1 supports the I<sup>2</sup>C serial bus and data transmission protocol in all three defined modes: standard, fast, and high-speed. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a *master*. The devices that are controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The TSC2007-Q1 operates as a slave on the I<sup>2</sup>C bus. Connections to the bus are made via the open-drain I/O lines, SDA and SCL.

The following bus protocol has been defined (see [Figure 29](#)):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

**Bus Not Busy** Both data and clock lines remain HIGH.

**Start Data Transfer** A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

**Stop Data Transfer** A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

**Data Valid** The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit.

Within the I<sup>2</sup>C bus specifications, a standard mode (100kHz clock rate), a fast mode (400kHz clock rate), and a high-speed mode (1.7MHz or 3.4MHz clock rate) are each defined. The TSC2007-Q1 works in all three modes.

**Acknowledge** Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 29 details how data transfer is accomplished on the I<sup>2</sup>C bus. Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer ends with a STOP condition or a repeated START condition. Because a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

The TSC2007-Q1 may operate in the following two modes:

1. **Slave Receiver Mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2. **Slave Transmitter Mode:** The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data are transmitted on SDA by the TSC2007-Q1 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

### I<sup>2</sup>C Fast or Standard Mode (F/S Mode)

In I<sup>2</sup>C Fast or Standard (F/S) mode, serial data transfer must meet the timing shown in the [Timing Information](#) section.

In the serial transfer format of F/S mode, the master signals the beginning of a transmission to a slave with a START condition (S), which is a high-to-low transition on the SDA input while SCL is high. When the master has finished communicating with the slave, the master issues a STOP condition (P), which is a low-to-high transition on SDA while SCL is high, as shown in Figure 29. The bus is free for another transmission after a STOP condition has occurred. Figure 29 shows the complete F/S mode transfer on the I<sup>2</sup>C, 2-wire serial interface. The address byte, control byte, and data byte are transmitted between the START and STOP conditions. The SDA state is only allowed to change while SCL is low, except for the START and STOP conditions. Data are transmitted in 8-bit words. Nine clock cycles are required to transfer the data into or out of the device (8-bit word plus acknowledge bit).

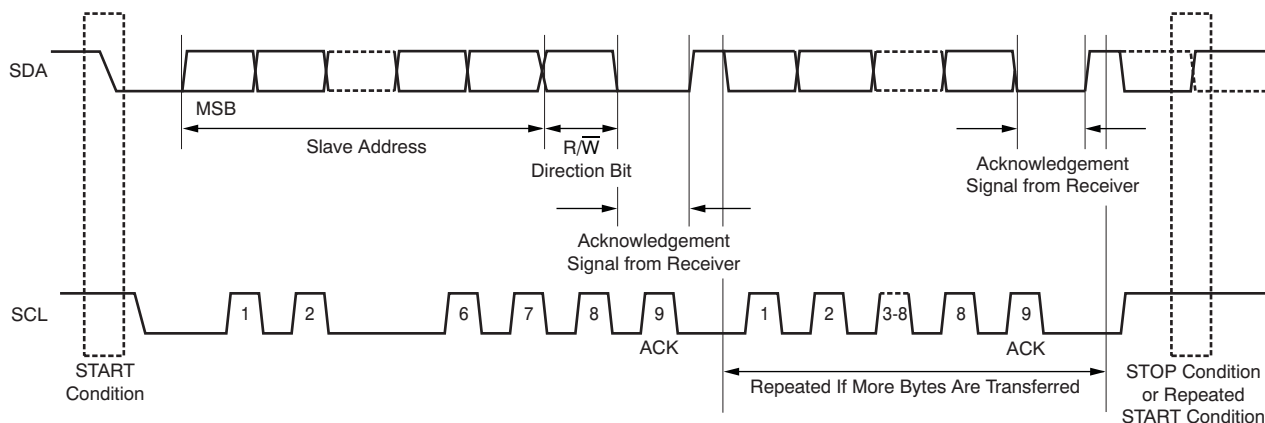


Figure 29. Complete Fast- or Standard-Mode Transfer

## I<sup>2</sup>C High-Speed Mode (Hs Mode)

The TSC2007-Q1 can operate with high-speed I<sup>2</sup>C masters. To do so, the pull-up resistor on SCL must be changed to an active pull-up, as recommended in the I<sup>2</sup>C specification.

Serial data transfer format in High-Speed (Hs) mode meets the Fast or Standard (F/S) mode I<sup>2</sup>C bus specification. Hs mode can only commence after the following conditions (all of which are in F/S mode) exist:

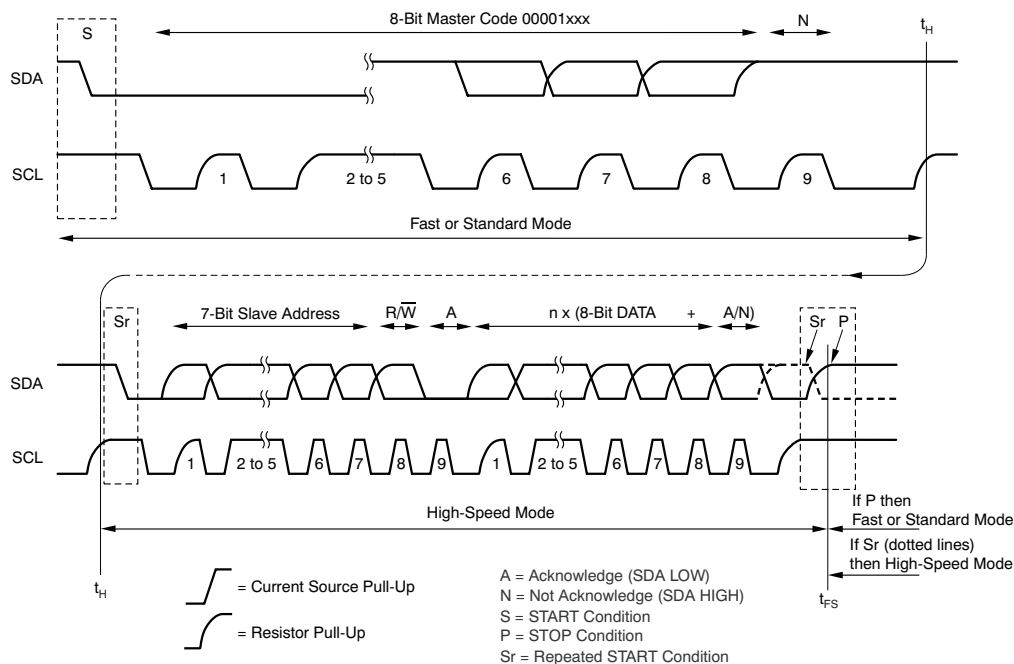
1. START condition (S)
2. 8-bit master code (00001xxx)
3. Not-acknowledge bit (N)

Figure 30 shows this sequence in more detail. Hs-mode master codes are reserved 8-bit codes used only for triggering Hs mode, and are not to be used for slave addressing or any other purpose. The master code indicates to other devices that an Hs-mode transfer is about to begin and the connected devices must meet the Hs mode specification. Because no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge bit (N).

After the not-acknowledge bit (N) and SCL have been pulled-up to a HIGH level, the master switches to Hs-mode and enables the current-source pull-up circuit for SCL (at time  $t_{H1}$  shown in Figure 30). Because other devices can delay the serial transfer before  $t_{H1}$  by stretching the LOW period of SCL, the master enables the current-source pull-up circuit when all devices have released SCL, and SCL has reached a HIGH level, thus speeding up the last part of the rise time of the SCL.

The master then sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/W bit address, and receives an acknowledge bit (A) from the selected slave. After a repeated START (Sr) condition and after each acknowledge bit (A) or not-acknowledge bit (N), the master disables its current-source pull-up circuit. This disabling enables other devices, such as the TSC2007-Q1, to delay the serial transfer (until the converted data are stored in the TSC internal shift register) by stretching the LOW period of SCL. The master re-enables its current-source pull-up circuit again when all devices have released SCL, and SCL reaches a HIGH level, which speeds up the last part of the SCL signal rise time.

Data transfer continues in Hs mode after the next repeated START (Sr), and only switches back to F/S mode after a STOP condition (P). To reduce the overhead of the master code, it is possible for the master to link a number of Hs mode transfers, separated by repeated START conditions (Sr).



**Figure 30. Complete High-Speed Mode Transfer**



## DIGITAL INTERFACE

### ADDRESS BYTE

The TSC2007-Q1 has a 7-bit slave address word. The first five bits (MSBs) of the slave address are factory-preset to comply with the I<sup>2</sup>C standard for A/D converters and are always set at '10010'. The logic state of the address input pins (A1-A0) determines the two LSBs of the device address to activate communication. Therefore, a maximum of four devices with the same preset code can be connected on the same bus at one time.

The A1-A0 address inputs are read whenever an address byte is received, and should be connected to the supply pin (VDD/REF) or the ground pin (GND). The slave address is latched into the TSC2007-Q1 on the falling edge of SCL after the read/write bit has been received by the slave.

The last bit of the address byte (R/ $\overline{W}$ ) defines the operation to be performed. When set to a '1', a read operation is selected; when set to a '0', a write operation is selected. Following the START condition, the TSC2007-Q1 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving the '10010' code, the appropriate device select bits, and the R/ $\overline{W}$  bit, the slave device outputs an acknowledge signal on the SDA line.

**Table 1. I<sup>2</sup>C Slave Address Byte**

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	0	0	1	0	A1	A0	R/ $\overline{W}$

#### Bit D0: R/ $\overline{W}$

- 1: I<sup>2</sup>C master read from TSC (I<sup>2</sup>C read addressing).
- 0: I<sup>2</sup>C master write to TSC (I<sup>2</sup>C write addressing).

### COMMAND BYTE

**Table 2. Command Byte Definition (Excluding the Setup Command)<sup>(1)</sup>**

BIT	NAME	DESCRIPTION
D7-D4	C3-C0	All Converter Function Select bits as detailed in <a href="#">Table 3</a> , except for the setup command ('1011').
D3-D2	PD1-PD0	00: Power down between cycles. $\overline{PENIRQ}$ enabled. 01: A/D converter on. $\overline{PENIRQ}$ disabled. 10: A/D converter off. $\overline{PENIRQ}$ enabled. 11: A/D converter on. $\overline{PENIRQ}$ disabled.
D1	M	0: 12-bit (Lower speed referred to as the 2MHz clock). 1: 8-bit (Higher speed referred to as the 4MHz clock).
D0	X	Don't care.

(1) The command byte definition for the setup command is shown in [Table 4](#).

**Bits D7-D4: C3-C0**—Converter function select bits. These bits select the input to be converted and the converter function to be executed, activate the drivers, and configure the  $\overline{PENIRQ}$  pull-up resistor ( $R_{IRQ}$ ). [Table 3](#) lists the possible converter functions.

**Bits D3-D2: PD1-PD0**—Power-down bits. These two bits select the power-down mode that the TSC2007-Q1 will be in after the current command completes, as shown in [Table 2](#).

It is recommended to set PD0 = 0 in each command byte to get the lowest power consumption possible. If multiple X-, Y-, and Z-position measurements will be done one right after another (such as when averaging), PD0 = 1 will leave the touch screen drivers on at the end of each conversion cycle.

**Bit D1: M**—Mode bit. If M = 0, the TSC2007-Q1 is in 12-bit mode. If M = 1, 8-bit mode is selected.

**Bit D0: X**—Don't care.

When the TSC2007-Q1 powers up, the power-down bits must be written to ensure that the device is placed into the mode that achieves the lowest power. Therefore, immediately after power-up, send a command byte that sets PD1 = PD0 = 0, so that the device will be in the lowest power mode, powering down between conversions.

**Table 3. Converter Function Select**

C3	C2	C1	C0	FUNCTION	INPUT TO A/D CONVERTER	X-DRIVERS	Y-DRIVERS	ACK	REFERENCE MODE
0	0	0	0	Measure TEMP0	TEMP0	OFF	OFF	Y	Single-Ended
0	0	0	1	Reserved	N/A	OFF	OFF	N	Single-Ended
0	0	1	0	Measure AUX	AUX	OFF	OFF	Y	Single-Ended
0	0	1	1	Reserved	N/A	OFF	OFF	N	Single-Ended
0	1	0	0	Measure TEMP1	TEMP1	OFF	OFF	Y	Single-Ended
0	1	0	1	Reserved	N/A	OFF	OFF	N	Single-Ended
0	1	1	0	Reserved	N/A	OFF	OFF	N	Single-Ended
0	1	1	1	Reserved	N/A	OFF	OFF	N	Single-Ended
1	0	0	0	Activate X-drivers	N/A	ON	OFF	Y	Differential
1	0	0	1	Activate Y-drivers	N/A	OFF	ON	Y	Differential
1	0	1	0	Activate Y+, X-drivers	N/A	X– ON	Y+ ON	Y	Differential
1	0	1	1	Setup command <sup>(1)</sup>	N/A	OFF	OFF	N	N/A
1	1	0	0	Measure X position	Y+	ON	OFF	Y	Differential
1	1	0	1	Measure Y position	X+	OFF	ON	Y	Differential
1	1	1	0	Measure Z1 position	X+	X– ON	Y+ ON	Y	Differential
1	1	1	1	Measure Z2 position	Y–	X– ON	Y+ ON	Y	Differential

- (1) The setup command has an additional four bits of data. These data are static; that is, they are not changed by other commands, except for the power-on reset. The default value for these bits after power-on reset is 0000. [Table 4](#) shows the definition of these data bits.

**Table 4. Command Byte Definition for the Setup Command**

BIT	NAME	DESCRIPTION
D7-D4	C3-C0 = '1011'	Setup command; must write '1011'.
D3-D2	PD1-PD0 = '00'	Reserved; must write '00'.
D1	Filter control	0: Use the onboard MAV filter (default). 1: Bypass the onboard MAV filter.
D0	$\overline{\text{PENIRQ}}$ pull-up resistor ( $R_{\text{IRQ}}$ ) select	0: $R_{\text{IRQ}} = 50\text{k}\Omega$ (default). 1: $R_{\text{IRQ}} = 90\text{k}\Omega$ .

## START A CONVERTER FUNCTION/WRITE CYCLE

A conversion/write cycle begins when the master issues the address byte containing the slave address of the TSC2007-Q1, with the eighth bit equal to a 0 ( $R/\overline{W} = 0$ ), as shown in Table 1. Once the eighth bit has been received, and the address matches the A1-A0 address input pin setting, the TSC2007-Q1 issues an acknowledge.

When the master receives the acknowledge bit from the TSC2007-Q1, the master writes the command byte to the slave (see Table 2). After the command byte is received by the slave, the slave issues another acknowledge bit. The master then ends the write cycle by issuing a repeated START or a STOP condition, as shown in Figure 31.

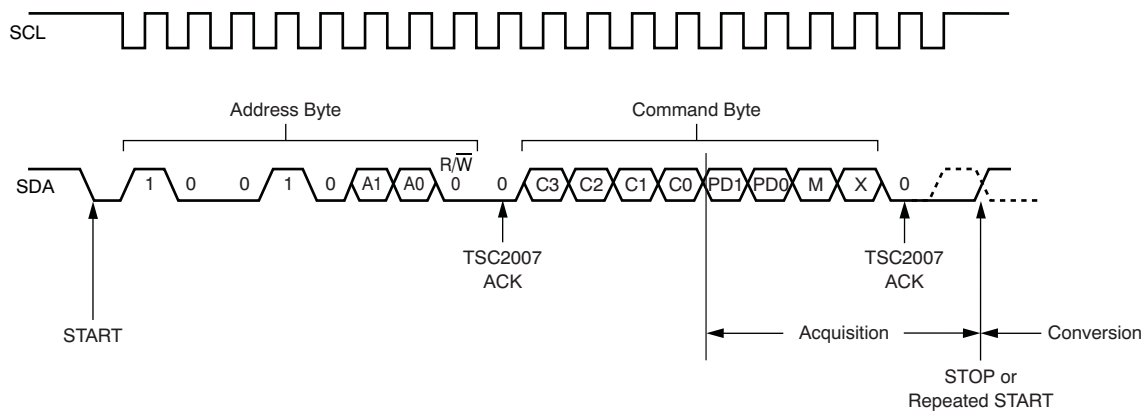


Figure 31. Complete I<sup>2</sup>C Serial Write Transmission

If the master sends additional command bytes after the initial byte, but before sending a STOP or repeated START condition, the TSC2007-Q1 does not acknowledge those bytes.

The input multiplexer channel for the A/D converter is selected when bits C3 through C0 are clocked in. If the selected channel is an X-, Y-, or Z-position measurement, the appropriate drivers turn on once the acquisition period begins.

When  $R/\overline{W} = 0$ , the input sample acquisition period starts on the falling edge of SCL when the C0 bit of the command byte has been latched, and ends when a STOP or repeated START condition has been issued. A/D conversion starts immediately after the acquisition period. The multiplexer inputs to the A/D converter are disabled once the conversion period starts. However, if an X-, Y-, or Z-position is being measured, the respective touch screen drivers remain on during the conversion period. A complete write cycle is shown in Figure 31.

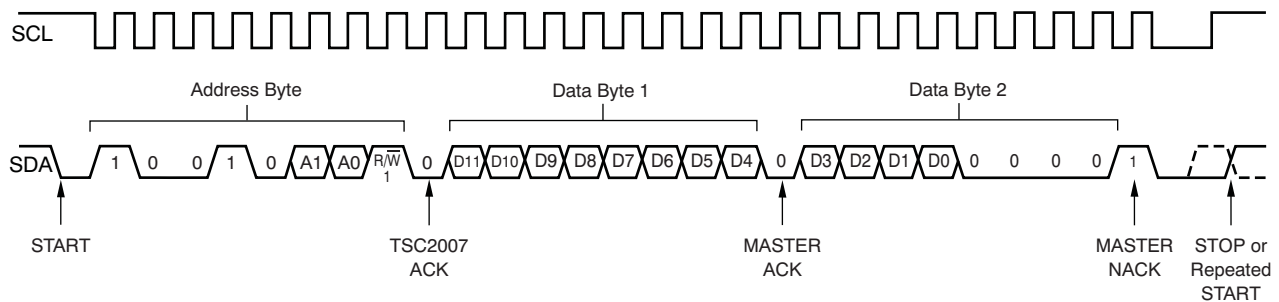
## READ A CONVERSION/READ CYCLE

For best performance, the I<sup>2</sup>C bus should remain in an idle state while an A/D conversion is taking place. This idling prevents digital clock noise from affecting the bit decisions being made by the TSC2007-Q1. The master should wait for at least 10µs before attempting to read data from the TSC2007-Q1 to realize this best performance. However, the master does not need to wait for a completed conversion before beginning a read from the slave, if full 12-bit performance is not necessary.

Data access begins with the master issuing a START condition followed by the address byte (see Table 1) with R/W = 1.

When the eighth bit has been received and the address matches, the slave issues an acknowledge. The first byte of serial data then follows (D11-D4, MSB first).

After the first byte has been sent by the slave, it releases the SDA line for the master to issue an acknowledge. The slave responds with the second byte of serial data upon receiving the acknowledge from the master (D3-D0, followed by four 0 bits). The second byte is followed by a NOT acknowledge bit (ACK = 1) from the master to indicate that the last data byte has been received. If the master somehow acknowledges the second data byte, invalid data are returned (FFh). This condition applies to both 12-and 8-bit modes. See Figure 32 for a complete I<sup>2</sup>C read transmission.



**Figure 32. Complete I<sup>2</sup>C Serial Read Transmission**

## THROUGHPUT RATE AND I<sup>2</sup>C BUS TRAFFIC

Although the internal A/D converter has a sample rate of up to 200kSPS, the throughput presented at the bus is much lower. The rate is reduced because preprocessing manages the redundant work of filtering out noise. The throughput is further limited by the I<sup>2</sup>C bus bandwidth. The effective throughput is approximately 20kSPS at 8-bit resolution, or 10kSPS at 12-bit resolution. This preprocessing saves a large portion of the I<sup>2</sup>C bandwidth for the system to use on other devices.

Each sample and conversion takes 19 CCLK cycles (12-bit), or 16 CCLK cycles (8-bit). For a typical internal 4MHz OSC clock, the frequency actually ranges from 3.66MHz to 3.82MHz. For  $V_{DD} = 1.2V$ , the frequency reduces to 3.19MHz, which gives a  $3.19MHz/16 = 199kSPS$  raw A/D converter sample rate.

### 12-Bit Operation

For 12-bit operation, sending the conversion result across the I<sup>2</sup>C bus takes 49 bus clocks (SCL clock). Each write cycle takes 20 I<sup>2</sup>C cycles (START, STOP, address byte, 2 ACKs, and command byte). Each read cycle takes 29 I<sup>2</sup>C cycles (START, STOP, address byte, 3 ACKs, and data bytes 1 and 2). Seven sample-and-conversions take  $19 \times 7$  internal clocks to complete. The MAV filter loop requires 19 internal clocks. For  $V_{DD} = 1.2V$ , the complete processed data cycle time calculations are shown in Table 5. Because the first acquisition cycle overlaps with the I/O cycle, four CCLKs should be deducted from the total CCLK cycles. For 12-bit mode,  $(19 \times 7 + 19) - 4 = 148$  CCLKs plus I/O are required.

### 8-Bit Operation

For 8-bit operation, sending the conversion result across the I<sup>2</sup>C bus takes 40 bus clocks (SCL clock). Each write cycle takes 20 I<sup>2</sup>C cycles (START, STOP, address byte, 2 ACKs, and command byte). Each read cycle takes 20 I<sup>2</sup>C cycles (START, STOP, address byte, 2 ACKs, and data byte 1). Seven sample-and-conversions takes  $16 \times 7$  internal clocks to complete. The MAV filter loop requires 19 internal clocks. For  $V_{DD} = 1.2V$ , the complete processed data cycle time calculations are shown in Table 5. Because the first acquisition cycle overlaps with the I/O cycle, four CCLKs should be deducted from the total CCLK cycles. For 8-bit mode,  $(16 \times 7 + 19) - 4 = 127$  CCLKs plus I/O are required.

**Table 5. Measurement Cycle Time Calculations**

<b>STANDARD MODE: 100kHz (Period = 10μs)</b>	
8-Bit	$40 \times 10\mu s + 127 \times 313ns = 439.8\mu s$ (2.27kSPS through the I <sup>2</sup> C bus)
12-Bit	$49 \times 10\mu s + 148 \times 625ns = 582.5\mu s$ (1.72kSPS through the I <sup>2</sup> C bus)
<b>FAST MODE: 400kHz (Period = 2.5μs)</b>	
8-Bit	$40 \times 2.5\mu s + 127 \times 313ns = 139.8\mu s$ (7.15kSPS through the I <sup>2</sup> C bus)
12-Bit	$49 \times 2.5\mu s + 148 \times 625ns = 215\mu s$ (4.65kSPS through the I <sup>2</sup> C bus)
<b>HIGH-SPEED MODE: 1.7MHz (Period = 588ns)</b>	
8-Bit	$40 \times 588ns + 127 \times 313ns = 63.3\mu s$ (15.79kSPS through the I <sup>2</sup> C bus)
12-Bit	$49 \times 588ns + 148 \times 625ns = 121.3\mu s$ (8.24kSPS through the I <sup>2</sup> C bus)
<b>HIGH-SPEED MODE: 3.4MHz (Period = 294ns)</b>	
8-Bit	$40 \times 294ns + 127 \times 313ns = 51.6\mu s$ (19.39kSPS through the I <sup>2</sup> C bus)
12-Bit	$49 \times 294ns + 148 \times 625ns = 106.9\mu s$ (9.35kSPS through the I <sup>2</sup> C bus)

As an example, use  $V_{DD} = 1.2V$  and 12-bit mode with the Fast-mode I<sup>2</sup>C clock ( $f_{SCL} = 400kHz$ ). The equivalent TSC throughput is at least seven times faster than the effective throughput across the bus ( $4.65k \times 7 = 32.55kSPS$ ). The supply current to the TSC for this rate and configuration is  $128\mu A$ . To achieve an equivalent sample throughput of 8.2kSPS using the device without preprocessing, the TSC2007-Q1 consumes only  $(8.2/32.55) \times 128\mu A = 32.24\mu A$ .

**Table 6. Effective and Equivalent Throughput Rates**

SUPPLY VOLTAGE	I <sup>2</sup> C BUS SPEED (f <sub>SCL</sub> )	RESOLUTION	TSC CONVERSION CYCLE TIME (μs)	EFFECTIVE THROUGHPUT (kSPS)	EQUIVALENT THROUGHPUT (kSPS)	NO. OF SCL	NO. OF CCLK	f <sub>CCLK</sub> (kHz)	CCLK PERIODS (ns)
2.7V	100kHz Standard	8-bit	433.6	2.31	16.14	40	127	3780	264.6
		12-bit	568.7	1.76	12.31	49	148	1880	531.9
	400kHz Fast	8-bit	133.6	7.49	52.40	40	127	3780	264.6
		12-bit	201.2	4.97	34.79	49	148	1880	531.9
	1.7MHz High-Speed	8-bit	57.1	17.50	122.53	40	127	3780	264.6
		12-bit	107.5	9.30	65.09	49	148	1880	531.9
	3.4MHz High-Speed	8-bit	45.4	22.04	154.31	40	127	3780	264.6
		12-bit	93.1	10.74	75.16	49	148	1880	531.9
1.8V	100kHz Standard	8-bit	434.7	2.30	16.10	40	127	3660	273.2
		12-bit	570.9	1.75	12.26	49	148	1830	546.4
	400kHz Fast	8-bit	134.7	7.42	51.97	40	127	3660	273.2
		12-bit	203.4	4.92	34.42	49	148	1830	546.4
	1.7MHz High-Speed	8-bit	58.2	17.17	120.22	40	127	3660	273.2
		12-bit	109.7	9.12	63.81	49	148	1830	546.4
	3.4MHz High-Speed	8-bit	46.5	21.52	150.65	40	127	3660	273.2
		12-bit	95.3	10.49	73.46	49	148	1830	546.4
1.2V	100kHz Standard	8-bit	439.8	2.27	15.92	40	127	3190	313.5
		12-bit	582.5	1.72	12.02	49	148	1600	625.0
	400kHz Fast	8-bit	139.8	7.15	50.07	40	127	3190	313.5
		12-bit	215.0	4.65	32.56	49	148	1600	625.0
	1.7MHz High-Speed	8-bit	63.3	15.79	110.51	40	127	3190	313.5
		12-bit	121.3	8.24	57.70	49	148	1600	625.0
	3.4MHz High-Speed	8-bit	51.6	19.39	135.72	40	127	3190	313.5
		12-bit	106.9	9.35	65.47	49	148	1600	625.0

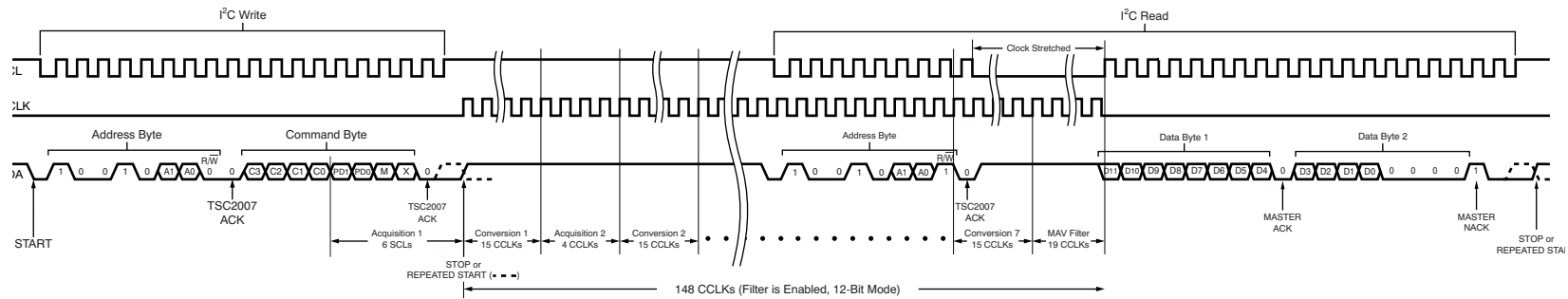


Figure 33. Data Acquisition Cycle (Filter Enabled)

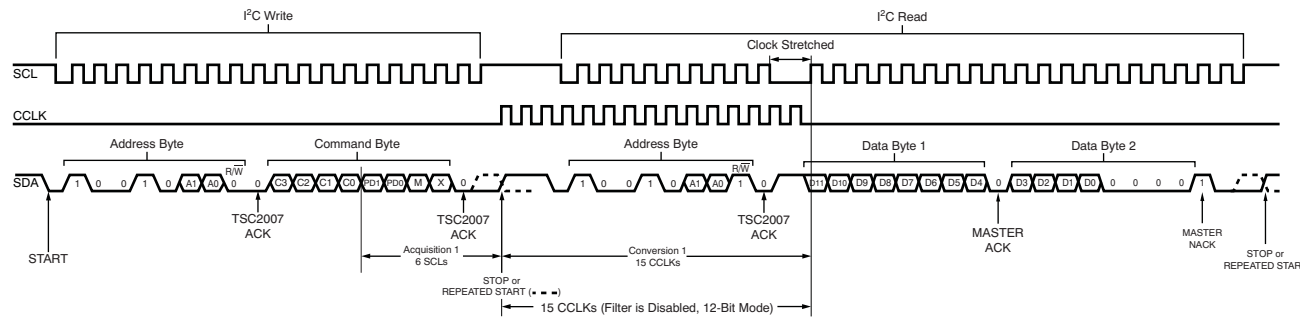
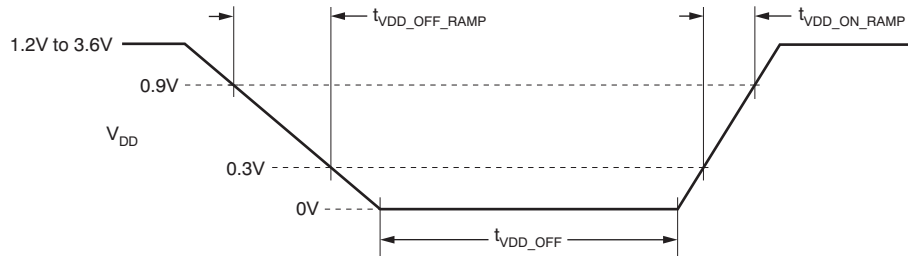


Figure 34. Data Acquisition Cycle (Filter Disabled)

## POWER-ON RESET (POR)

During TSC2007-Q1 power-up, an internal power-on reset (POR) is automatically implemented. The POR brings the TSC to the default working condition, and checks the A0 and A1 pins for the two LSBs of the I<sup>2</sup>C address. The TSC2007-Q1 senses the power-up curve to decide whether or not to implement a POR.

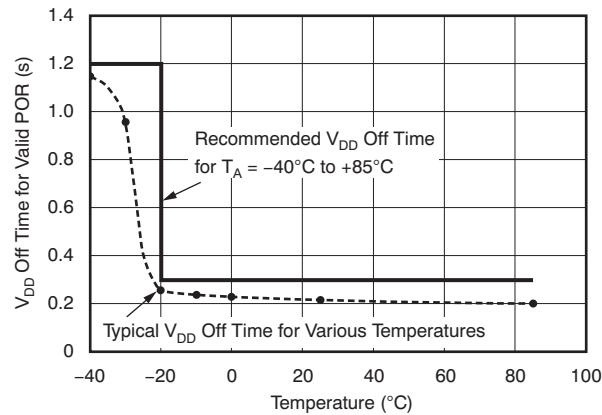
It is required to follow the power-on/off slope and interval requirements, as provided in the [Electrical Characteristics](#), in order to ensure a proper POR of the TSC2007-Q1.



**Figure 35. Power-On Reset Timing**

**Table 7. Timing Requirements for Figure 35**

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V <sub>DD</sub> off ramp	T <sub>A</sub> = -40°C to +85°C	2		kV/s
V <sub>DD</sub> off time	T <sub>A</sub> = -40°C to +85°C, V <sub>DD</sub> = 0V	1.2		s
	T <sub>A</sub> = -20°C to +85°C, V <sub>DD</sub> = 0V	0.3		s
V <sub>DD</sub> on ramp	T <sub>A</sub> = -40°C to +85°C	12		kV/s



**Figure 36. V<sub>DD</sub> Off Time vs Temperature**



## LAYOUT

The following layout suggestions should obtain optimum performance from the TSC2007-Q1. Keep in mind that many portable applications have conflicting requirements for power, cost, size, and weight. In general, most portable devices have fairly clean power and grounds because most of the internal components are very low power. This situation would mean less bypassing for the converter power and less concern regarding grounding. However, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the TSC2007-Q1 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur immediately before latching the output of the analog comparator. Therefore, during any single conversion for an  $n$ -bit SAR converter, there are  $n$  windows in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the SCL input.

With this consideration in mind, power to the TSC2007-Q1 should be clean and well-bypassed. A 0.1  $\mu\text{F}$  ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1  $\mu\text{F}$  to 10  $\mu\text{F}$  capacitor may also be needed if the impedance of the connection between VDD/REF and the power supply is high.

A bypass capacitor is generally not needed on the VDD/REF pin because the internal reference is buffered by an internal op amp. If an external reference voltage originates from an op amp, make sure that it can drive any bypass capacitor that is used without oscillation.

The TSC2007-Q1 architecture offers no inherent rejection of noise or voltage variation with regard to using an external reference input, which is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. While high-frequency noise can be filtered out, voltage variation because of line frequency (50Hz or 60Hz) can be difficult to remove. Some package options have pins labeled as VOID. Avoid any active trace going under any pin marked as VOID unless it is shielded by a ground or power plane.

The GND pin should be connected to a clean ground point. In many cases, this point is the analog ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery connection point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Resistive touch screens have fairly low resistance; therefore, the interconnection should be as short and robust as possible. Loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch-screen applications (for example, applications that require a back-lit LCD panel). This electromagnetic interference (EMI) noise can be coupled through the LCD panel to the touch screen and cause flickering of the converted A/D converter data. Several things can be done to reduce this error, such as using a touch screen with a bottom-side metal layer connected to ground, which couples the majority of noise to ground. Additionally, filtering capacitors, from Y+, Y–, X+, and X– to ground, can also help. Note, however, that the use of these capacitors increases screen settling time and requires a longer time for panel voltages to stabilize. The resistor value varies depending on the touch screen sensor used. The PENIRQ pull-up resistor ( $R_{\text{IRQ}}$ ) may be adequate for most of sensors.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TSC2007IPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF TSC2007-Q1 :**

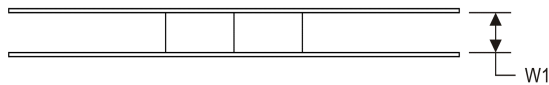
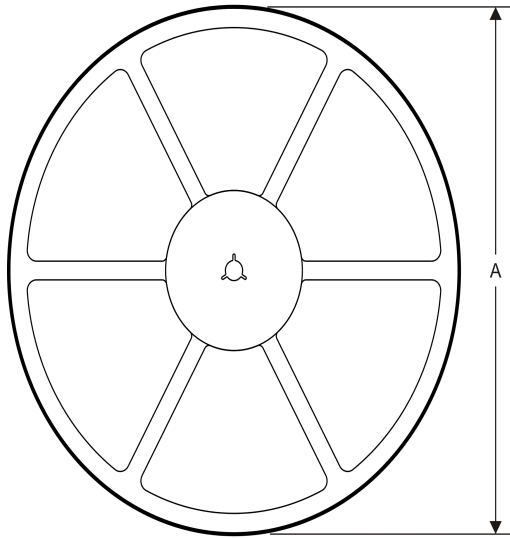
- Catalog: [TSC2007](#)

NOTE: Qualified Version Definitions:

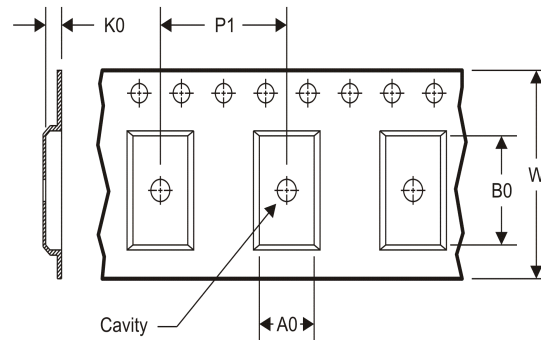
- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSC2007IPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

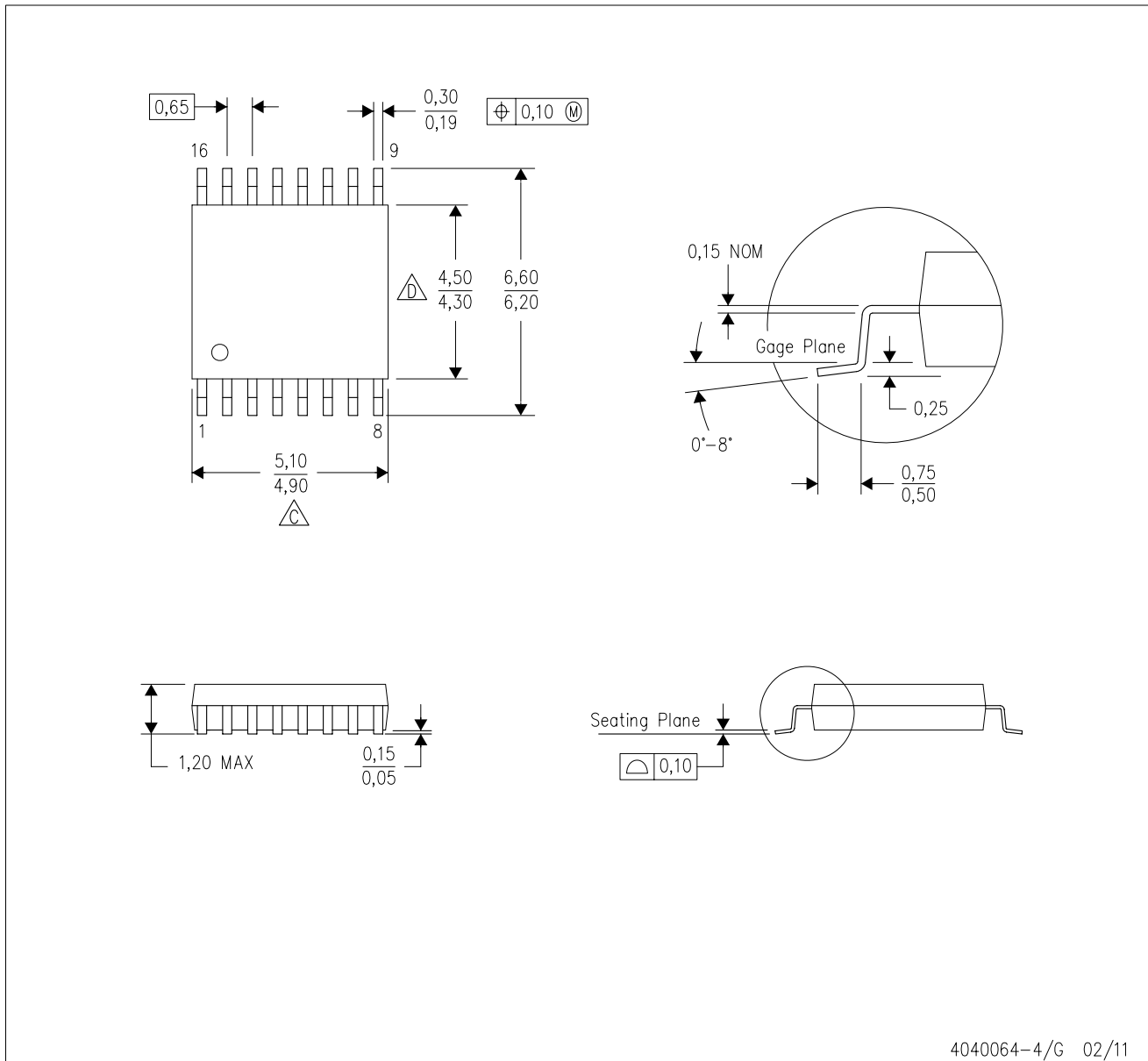


\*All dimensions are nominal



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSC2007IPWRQ1	TSSOP	PW	16	2000	346.0	346.0	29.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

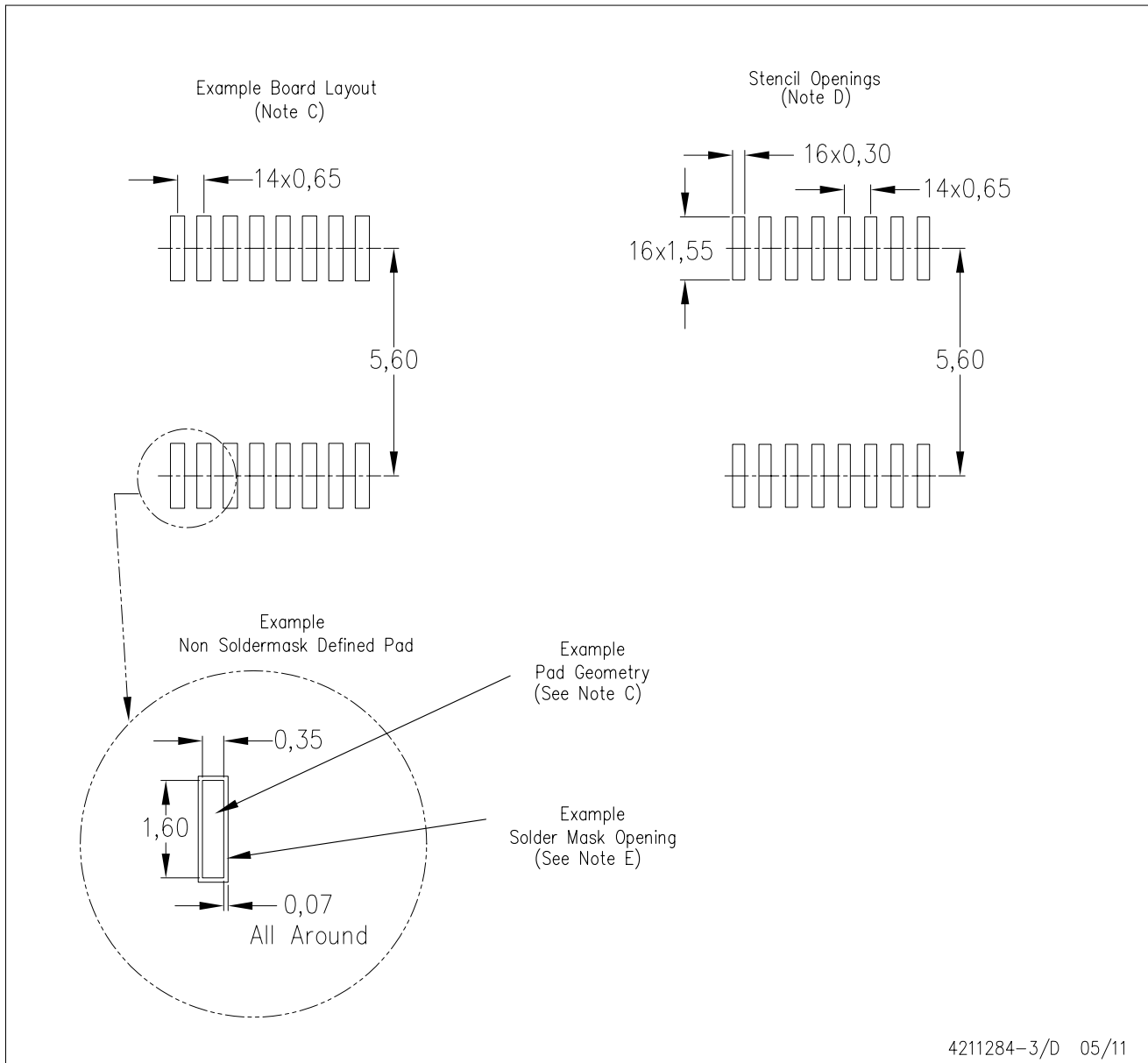


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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