8-Channel Serial to Parallel Converter with High Voltage Push-Pull Outputs, POL, Hi-Z, and Short Circuit Detect

Features

- ► HVCMOS® technology
- Operating output voltage of 250V
- ► Low power level shifting from 5.0 to 250V
- ► Shift register speed 8.0MHz @ V_{DD} = 5.0V
- 8 latch data outputs
- Output polarity and blanking
- Output short circuit detect
- Output high-Z control
- CMOS compatible inputs

Applications

- Piezoelectric transducer driver
- Braille driver
- Weaving applications
- Printer drivers
- MEMs
- Displays

General Description

The HV513 is a low voltage serial to high voltage parallel converter with 8 high voltage push-pull outputs. This device has been designed to drive small capacitve loads such as piezoelectric transducers. It can also be used in any application requiring multiple high voltage outputs, with medium current source and sink capabilities.

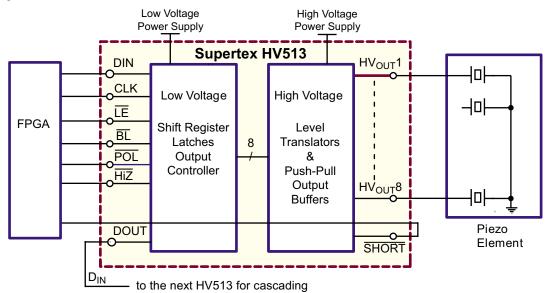
The device consists of an 8-bit shift register, 8 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the low to high transition of the clock. A data output buffer is provided for cascading devices. Operation of the shift register is not affected by the $\overline{\text{LE}}$, $\overline{\text{BL}}$, $\overline{\text{POL}}$, or the $\overline{\text{HI-Z}}$ control inputs. Transfer of data from the shift register to the latch occurs when the $\overline{\text{LE}}$ is high. The data in the latch is stored when $\overline{\text{LE}}$ is low. A high-Z (HI-Z) pin is provided to set all the outputs in a high-Z state.

All outputs have short circuit protection that detects if the outputs have reached the required output state. If output does not track the required state, then the SHORT pin will be low. This output will pulse low during the output transistion period under normal operation; see SC Timing Diagram for details.

All outputs will have a break-before-make circuitry to reduce cross-over current during output state changes.

The POL, BL, LE, and HI-Z inputs have an internal pull up resistor.

Typical Application Circuit



Ordering Information

	Package	Options
Device	32-Lead QFN 6.00x.600mm body 0.80mm height (max) 0.50 pitch	24-Lead SOW 15.40x7.50mm body 2.65mm height (max) 1.27 pitch
HV513	HV513K7-G	HV513WG-G

-G indicates package is RoHS compliant ('Green')





Absolute Maximum Ratings

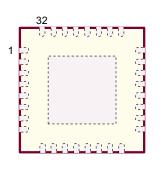
Parameter	Value
Logic supply, V _{DD}	-0.5V to 6.0V
High voltage supply, V _{PP}	V _{DD} to 275V
Logic input levels	-0.5V to V _{DD} +0.5V
Ground current ¹	0.3A
High voltage supply current¹	0.25A
Continuous total power dissipation ²	750mW
Operating junction temperature	-40°C to +85°C
Storage temperature range	-65°C to +150°C

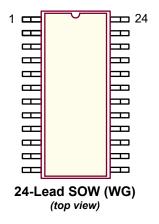
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

- by the total power dissipated in the package.
- 2. For operation above 25°C ambient derate linearly to 85°C at 12mW/°C.

Pin Configurations





32-Lead QFN (K7) (top view)

Product Marking



L = Lot Number YY = Year Sealed WW = Week Sealed A = Assembler ID C = Country of Origin _ = "Green" Packaging

Package may or may not include the following marks: Si or 🚮

32-Lead QFN (K7)





YY = Year Sealed WW = Week Sealed L = Lot Number

C = Country of Origin

Bottom Marking ccccccccc

A = Assembler ID* = "Green" Packaging

*May be part of top marking

1. Connection to all power and ground pads is required. Duty cycle is limited Package may or may not include the following marks: Si or 🚯

24-Lead SOW (WG)

Typical Operating Conditions

Sym	Parameter	Min	Тур	Max	Units	Conditions
V _{DD}	Logic supply voltage	4.5	5.0	5.5	V	
V _{PP}	High voltage supply	50	-	250	V	Note 1
V _{IH}	High-level input voltage	V _{DD} -0.9	-	V _{DD}	V	
V _{IL}	Low-level input voltage	0	-	0.9	V	
T	Operating junction temperature	-40	-	+85	°C	

Notes:

- 1. Below minimum V_{PP} the output may not switch.
- 2. Power-up sequence should be the following:
 - 1. Connect ground
 - 2. Apply $V_{\scriptscriptstyle DD}$
 - 3. Set all inputs (Data, CLK, Enable, etc.) to a known state
 - 4. Apply V_{PP}

Power-down sequence should be the reverse of the above

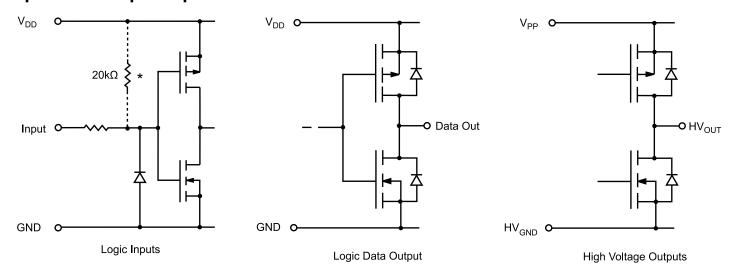
DC Electrical Characteristics (Over typical operating conditions unless otherwise specified, T_J = 25°C)

Sym	Parameter		Min	Тур	Max	Units	Conditions
I _{DD}	V _{DD} supply current		-	-	4.0	mA	$f_{CLK} = 8.0Hz, \overline{LE} = Low$
	Quioscont V supply	current	-	-	0.1	mA	$AII V_{IN} = V_{DD}$
DDQ	Quiescent V _{DD} supply	Current	-	-	2.0	IIIA	All V _{IN} = 0V
l _{PP}	V _{PP} supply current		-	-	100	μA	$V_{PP} = 250V, f_{OUT} = 300Hz,$ no load
l _{PPQ}	Quiescent V _{PP} supply	current	-	-	100	μΑ	V _{PP} = 240V, outputs are static
I _{IH}	High-level logic input	current	-	-	10	μΑ	$V_{IH} = V_{DD}$
			-		-10		V _{IL} = 0V
I _{IL}	Low-level logic input	current	-	-	-350	μA	$V_{\parallel} = 0V$, for inputs w/pull-up resistors
V	High lovel output	HV _{OUT}	140	-	-	V	$V_{PP} = 200V, I_{HVOUT} = -20mA$
V _{OH}	High level output	Data out	V _{DD} -1.0V	-	-	V	I _{DOUT} = -0.1mA
V	Low lovel output	HV _{OUT}	-	-	60	V	V _{DD} = 4.5V, I _{HVOUT} = 20mA
V _{OL}	V _{oL} Low level output	Data out	-	-	1.0	V	I _{DOUT} = 0.1mA

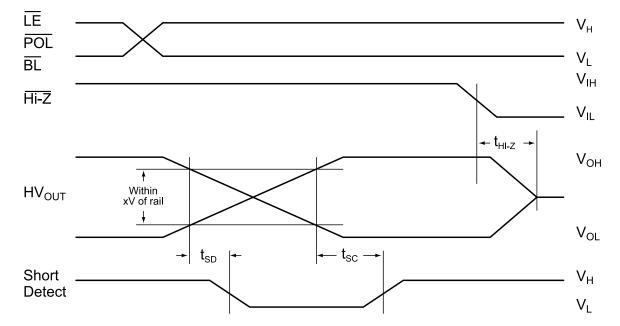
AC Electrical Characteristics (Over typical operating conditions unless otherwise specified, T, = 25°C)

	Porometer				Units	Conditions
Sym	Parameter	Min	Тур	Max	Units	Conditions
f _{CLK}	Clock frequency	0	-	8.0	MHz	
f _{out}	Output switching frequency (SOA limited)	-	300	-	Hz	C _L = 50nF, V _{PP} = 200V
t _w	Clock width high and low	62	-	-	ns	
t _{su}	Data setup time before clock rises	15	-	-	ns	
t _H	Data hold time after clock rises	30	-	-	ns	
t _{WLE}	Width of latch enable pulse	80	-	-	ns	
t _{DLE}	LE delay time after rising edge of clock	35	-	-	ns	
t _{SLE}	LE setup time before rising edge of clock	40	-	-	ns	
t_{OR}, t_{OF}	HV _{OUT} rise/fall time	-	-	1000	μs	C _L = 100nF, V _{PP} = 200V
t _{d ON/OFF}	Delay time for output to start rise/fall	-	-	500	ns	
t _{DHL}	Delay time clock to D _{OUT} high to low	-	-	110	ns	C _L = 15pF
t _{DLH}	Delay time clock to D _{OUT} low to high	-	-	110	ns	C _L = 15pF
t_R, t_F	All logic inputs	-	-	5.0	ns	
t _{sd}	Output short circuit detection	-	-	500	ns	$C_L = 15pF$, Short to output fall of SHORT
t _{sc}	Output short circuit clear	-	-	3000	ns	Short clear to output rise of SHORT
t _{HI-Z}	Output HI-Z state	-	-	500	ns	

Input and Output Equivalent Circuits



Short Circuit Detect Detail Timing



Note:

For V_{PP} greater than 150V:

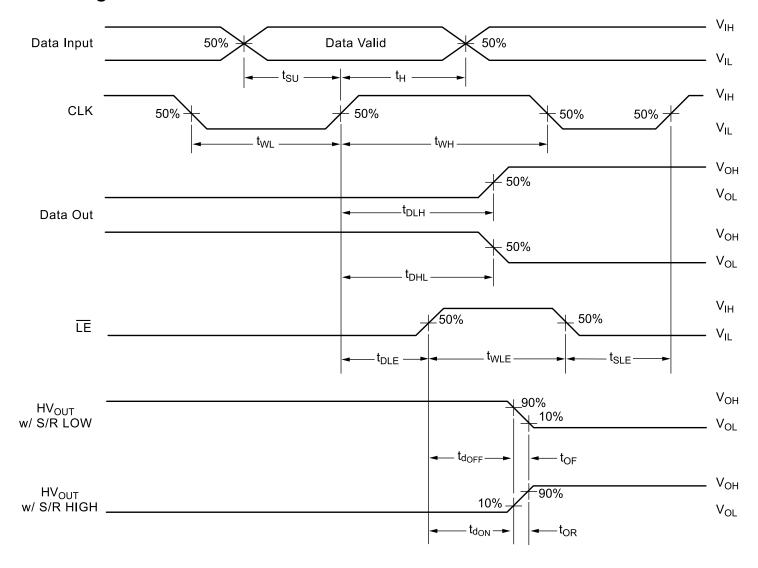
Short detect output will flag short conditions

- $HV_{\rm OUT}$ is higher than 10V when expected low $HV_{\rm OUT}$ is lower than $V_{\rm PP}$ 100V when expected high

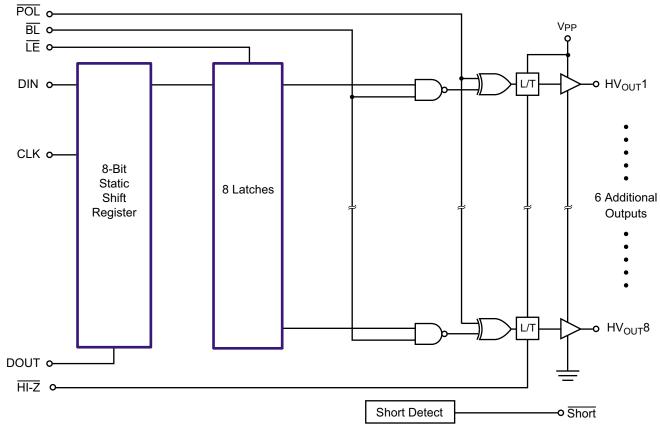
Short detect output will stay clear

- HV $_{\rm OUT}$ is lower than 2.0V when expected low HV $_{\rm OUT}$ is higher than V $_{\rm PP}$ 60V when expected high

Switching Waveforms



Functional Block Diagram



Note: — — POL, BL, LE, and Hi-Z have internal 20kΩ pull-up resistors.

Function Table

			Inpu	ıts			Outputs						
Function	Data	CLK	LE	BL	POL	HI-Z	Shift Reg 1 28	HV Outputs 1 28	Data Out				
All on	Х	Х	Х	L	L	Н	• ••	Н НН	•				
All off	Х	Х	Х	L	Н	Н	• ••	L LL	•				
Invert mode	Х	Х	L	Н	L	Н	• ••	• •• (b)	•				
Load S/R	H OR L	1	L	Н	Н	Н	HorL ••	• ••	•				
Store data in	Х	Х	L	Н	Н	Н	• ••	• ••	•				
latches	Х	Х	L	Н	L	Н	• ••	• •• (b)	•				
Transparent	L	1	Н	Н	Н	Н	L ••	L ••	•				
mode	Н	1	Н	Н	Н	Н	Н ••	Н ••	•				
Outputs High-Z	Х	Х	Х	Х	Х	L	• ••	High impedence outputs	•				
Outputs on	Х	Х	Х	Х	Х	Н	• ••	• ••	•				

Notes:

 $H = high level, L = low level, X = irrelevant, \uparrow = low-to-high transition$

• = dependent on previous stage's state before the last CLK or last \overline{LE} high.

Pin Description - 32-Lead QFN (K7)

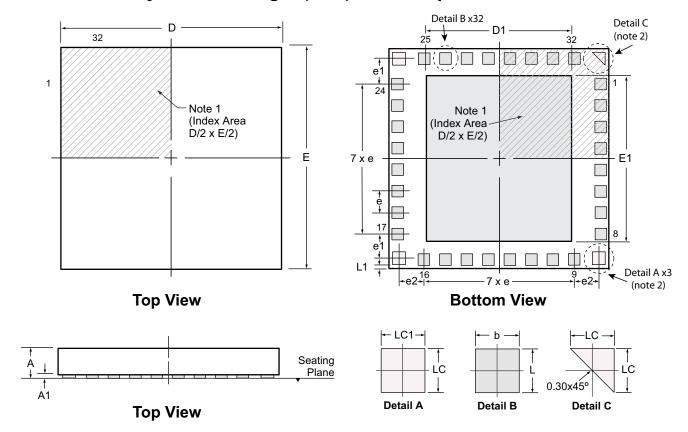
		52-Lead QI N (K7)					
Pin #	Function	Description					
1							
2	NC	No internal connection					
3							
4	LGND	Low voltage ground					
5	HVGND	High voltage ground					
6	1170110	Thigh voltage ground					
7	NC	No internal connection					
8	INC	No internal connection					
9	HV _{out} 1	High voltage push-pull output					
10	HV _{out} 2	High voltage push-pull output					
11	HV _{out} 3	High voltage push-pull output					
12	HV _{out} 4	High voltage push-pull output					
13	HV _{out} 5	High voltage push-pull output					
14	HV _{out} 6	High voltage push-pull output					
15	HV _{out} 7	High voltage push-pull output					
16	HV _{out} 8	High voltage push-pull output					
17	NC	No internal connection					
18	NC	No internal connection					
19	VDD	High voltage supply					
20	VPP						
21	VDD	Logic supply voltage					
22	DOUT	Data output					
23	NO	No internal compostion					
24	NC	No internal connection					
25	BL	Blanking pin, logic input low sets all HV _{OUTS} low					
26	NC	No internal connection					
27	POL	Polarity bar input logic					
28	CLK	Clock pin, shift registers shifts data on rising edge of input clock					
29	ĪĒ	Latch enable bar input logic					
30	SHORT	If output does not reach its required state, SHORT pin will output logic low					
31	HI-Z	High impedance pin, logic input low sets all outputs in a high impedance state					
32	DIN	Data input					
Center Pad	V _{PP}	Center pad is at V _{PP} potential. Connect to VPP or leave floating.					

Pin Description - 24-Lead SOW (WG)

Pin #	Function	Description
1	NC	No internal connection
2	VDD	Logic supply voltage
3	DOUT	Data output
4	BL	Blanking pin, logic input LOW sets all HV _{OUTS} low
5	POL	Polarity bar input logic
6	CLK	Clock pin, shift registers shifts data on rising edge of input clock
7	ĪĒ	Latch enable bar input logic
8	SHORT	If output does not reach its required state, SHORT pin will output logic LOW
9	HI-Z	High impedance pin, logic input LOW sets all outputs in a high impedance state
10	DIN	Data input
11	LGND	Low voltage ground
12	NC	No internal connection
13 14	HVGND	High voltage ground
15	HV _{out} 1	High voltage push-pull output
16	HV _{OUT} 2	High voltage push-pull output
17	HV _{OUT} 3	High voltage push-pull output
18	HV _{OUT} 4	High voltage push-pull output
19	HV _{OUT} 5	High voltage push-pull output
20	HV _{out} 6	High voltage push-pull output
21	HV _{out} 7	High voltage push-pull output
22	HV _{OUT} 8	High voltage push-pull output
23	VPP	High voltage cumply
24	VFF	High voltage supply

32-Lead QFN Package Outline (K7)

6.00x6.00mm body, 0.80mm height (max), 0.50mm pitch



Notes:

- A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
- 2. The 4 corner pads are for mechanical placement only, they are not internally connected.

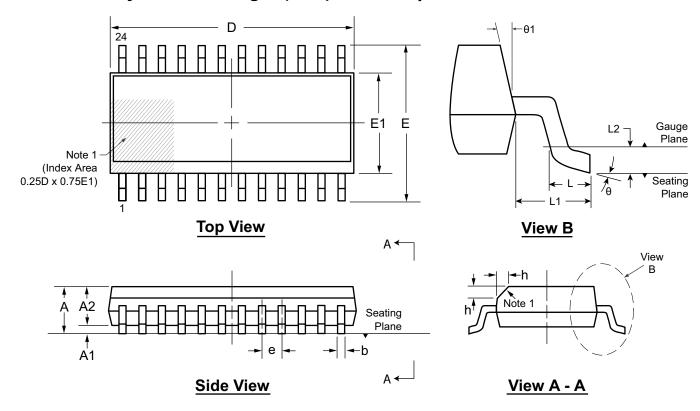
Symbol		Α	A1	b	D	D1	E	E1	е	e1	e2	L	L1	LC	LC1	
Dimension (mm)	MIN	0.70	0.00	0.20	5.90	3.20	5.90	4.30			4.00	0.075	0.20		0.20	0.25
	NOM	0.75	-	0.30	6.00	3.30	6.00	4.40	0.50 1.00 BSC REF	0.975 REF	0.30	0.10 REF	0.30	0.35		
(11111)	MAX	0.80	0.05	0.40	6.10	3.40	6.10	4.50			IXLI	0.40		0.40	0.45	

Drawings not to scale.

Supertex Doc. #: DSPD-32QFNK76X6P050, Version B101008.

24-Lead SOW (Wide Body) Package Outline (WG)

15.40x7.50 body, 2.65mm height (max), 1.27mm pitch



Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbo	ol	Α	A1	A2	b	D	E	E1	е	h	L	L1	L2	θ	θ1
	MIN	2.15*	0.10	2.05	0.31	15.20*	9.97*	7.40*		0.25	0.40			0 °	5 °
Dimension (mm)	NOM	-	-	-	-	15.40	10.30	7.50 1.27 BSC	-	-	1.40 REF	0.25 BSC	-	-	
()	MAX	2.65	0.30	2.55*	0.51	15.60*	10.63*	7.60*		0.75	1.27			8 º	15°

JEDEC Registration MS-013, Variation AD, Issue E, Sep. 2005.

Drawings are not to scale.

Supertex Doc. #: DSPD-24SOWWG, Version E041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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^{*} This dimension is not specified in the JEDEC drawing.