HIGH EFFICIENCY CHARGE PUMP FOR 7 WLEDs WITH I²C INTERFACE

FEATURES

- **3.0-V to 6.0-V Input Voltage Range**
- **×1 and ×1.5 Charge Pump**
- **Fully Programmable Current with I²C**
  - **64 Dimming Steps with 25mA Maximum (Sub and Main Display Banks)**
  - **4 Dimming Steps with 80mA Maximum (DM5 for Auxiliary Application)**
- **2% Current Matching for Sub LEDs at Light Load Condition (Each 100μA)**
- **750-kHz Charge Pump Frequency**
- **Continuous 230-mA Maximum Output Current**
- **Auto Switching Between ×1 and ×1.5 Mode for Maximum Efficiency**
- **Built-in Soft Start and Current Limit**
- **Hardware Enable/Disable**
- **Open Lamp Detection**
- **24-Pin 4mm x 4mm QFN**

APPLICATIONS

- **Cellular Phones**
- **PDA, PMP, GPS (Up To 4 Inch Display)**
- **Multidisplay Handheld Devices**

DESCRIPTION

The TPS60251 is a high efficiency, constant frequency charge pump DC/DC converter that uses a dual mode 1× and 1.5× conversion to maximize efficiency over the input voltage range. It drives up to five white LEDs for a main display and up to two white LEDs for a sub display with regulated constant current for uniform intensity. By utilizing adaptive 1×/1.5× charge pump modes and very low-dropout current regulators, the TPS60251 achieves high efficiency over the full 1-cell lithium-battery input voltage range.

Four enable inputs, ENmain, ENsub1, ENsub2, and ENaux, available through I²C, are used for simple on/off controls for the main, sub1, sub2, and DM5 displays, respectively. To lower operating current when using one sub display LED, the device provides independent operation in sub display LEDs.

The TPS60251 is available in a 24-pin 4mmx4mm thin QFN.

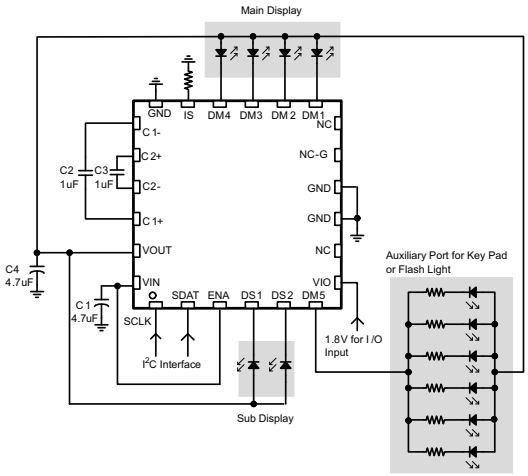


Figure 1. Typical Application for Sub and Main

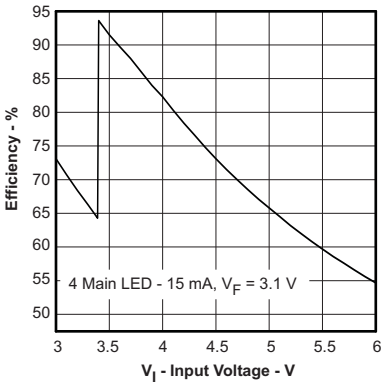


Figure 2. Efficiency vs Input Voltage

ORDERING INFORMATION(1)

PART NUMBER	PACKAGE	T_A
TPS60251RTW	24 Pin 4 mm × 4 mm QFN (RTW)	–40°C to +85°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_I	Input voltage range (all pins)	–0.3 to 7	V
	MAX Output current limit	650	mA
	HBM ESD Rating (2)	2	kV
	CDM ESD Rating(3)	500	V
	MM ESD Rating(4)	200	V
T_A	Operating temperature range	–40 to 85	°C
T_J	Maximum operating junction temperature	150	°C
T_{ST}	Storage temperature	–55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The Human body model (HBM) is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The testing is done according JEDECs EIA/JESD22-A114.
(3) Charged Device Model
(4) Machine Model (MM) is a 200-pF capacitor discharged through a 500-nH inductor with no series resistor into each pin. The testing is done according JEDECs EIA/JESD22-A115.

DISSIPATION RATINGS

PACKAGE	THERMAL RESISTANCE, $R_{\theta JC}$	THERMAL RESISTANCE, $R_{\theta JA}$	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
QFN 4×4 RTW	57.9°C/W	37.8°C/W	2.646 W	1.455 W	1.058 W

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	3.0		6.0	V
$I_{O(max)}$	Maximum output current		230		mA
C_I	Input capacitor		4.7		µF
C_O	Output capacitor		4.7		µF
C_1, C_2	Flying capacitor		1.0		µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C
$C_{IS(MAX)}$	Maximum capacitance on IS pin			100	pF

ELECTRICAL CHARACTERISTICS

V_I = 3.5 V, T_A = –40°C to 85°C, R_{IS} = 562 kΩ, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_I	Input voltage range		3.0		6.0	V
I_Q	Operating quiescent current	750-kHz Switching in 1.5× Mode (I_{MAIN_LED} = 15 mA × 4, I_O = 60 mA)			6.7	mA
		No switching in ×1 mode (I_O = 100 µA)			68	µA
I_{SD}	Shutdown current	Enable Control Register has 0x00			1.3	µA
V_{UVLO1}	UVLO Threshold voltage1(1)	V_I falling	2.2	2.4	2.6	V

(1) Shut down charge pump and power stage and keep I^2C content

ELECTRICAL CHARACTERISTICS (continued)

V_I = 3.5 V, T_A = –40°C to 85°C, R_{IS} = 562 kΩ, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO2}	UVLO Threshold voltage2 (2)	V_I falling	1.2	1.3	1.5	V
V_{hys}	Under-voltage lockout hysterisis	UVLO1		210		mV
V_{ENA_H}	Enable high threshold voltage		1.5		V_I	V
V_{ENA_L}	Enable low threshold voltage				0.4	V
T_S	Soft start time (3)	V_I = 3 V, C_O = 1 µF, I_{MAIN_LED} = 15 mA × 4		0.5		ms
CHARGE PUMP						
V_{out}	Overvoltage limit			6.5		V
F_s	Switching frequency			750		kHz
R_O	Open loop output impedance	×1 Mode, $(V_I – V_O)/I_O$			1.2	Ω
		×1.5 Mode, $(V_I × 1.5 – V_O)/I_O$ V_I = 3.0V (I_O = 120mA)		3.5	5.0	
CURRENT SINK						
K_{m_sub}	Current matching of sub LEDs at light load condition (4)	I_{SUB_LED} = 100 µA × 2, V_{DXX} = 0.4 V		0	±2%	
K_{m_main}	LED to LED Current matching (5)	I_{MAIN_LED} = 15 mA × 4, 3.0 V ≤ V_I ≤ 4.2 V		±0.1%	±5%	
K_a	Current accuracy	I_{LED} = 15 mA			±6%	
I_{D_MS}	Maximum LED current of DM1-4 and DS1-2	Main and Sub Display Current Register = 0×01&2(111111), V_{DXX} = 0.2 V		25.5		mA
I_{D_DM5}	Maximum LED current of DM5	Aux Display Current Register = 0×03 (XXXX11)		80		mA
V_{IS}	IS Pin voltage	3.0V ≤ V_I ≤ 6.0V	1.229	1.254	1.279	V
I_{sub}	Output current to current set ratio sub LEDs	I_{LED} = 100 µA (6)		44.8		
		I_{LED} = 15 mA (6)		6722		
I_{main}	Output current to current set ratio main LEDs	I_{LED} = 100 µA (6)		44.8		
		I_{LED} = 15 mA (6)		6722		
I_{DM5}	Output current to current set ratio DM5	I_{LED} = 80 mA (6)		35853		
$V_{DropOut}$	LED Drop out voltage	See (7)		80	120	mV
V_{TH_GU}	1× Mode to 1.5× mode transition threshold voltage (8)	V_{DXX} Falling, 15 mA × 4 measured on the lowest V_{DXX}	85	100	120	mV
V_{TH_GD}	Input voltage hysteresis for 1.5× to 1× mode transition	Measured as $V_I – (V_O – V_{DXX\_MIN})$, I_{MAIN_LED} = 15 mA × 4		550		mV
SERIAL INTERFACE TIMING REQUIREMENTS						
f_{max}	Clock frequency				400	kHz
$t_{wH(HIGH)}$	Pulse duration, clock high time			600		ns
$t_{wL(LOW)}$	Pulse duration, clock low time			1300		ns
t_r	DATA and CLK rise time				300	ns
t_f	DATA and CLK fall time				300	ns
$t_{h(STA)}$	High time (repeated) START condition(after this period the first clock pulse is generated)			600		ns
$t_{su(STA)}$	Setup time for repeated START condition			600		ns
$t_{h(DATA)}$	Data input hold time			0		ns
$t_{su(DATA)}$	Data input setup time			100		ns

(2) Shut down completely and come up with all 0's after device restart
(3) Measurement Condition: From enabling the LED driver to 90% output voltage after V_I is already up.
(4) LED current matching is defined as: $(I_{SUB\_LED\_WORST} – I_{AVG\_SUB}) / I_{AVG\_SUB}$
(5) LED to LED Current Matching is defined as: $(I_{MAIN\_LED\_WORST} – I_{AVG\_MAIN}) / I_{AVG\_MAIN}$
(6) See the *Setting the LED Current* section of the data sheet for details on calculating LED current given by dimming step and R_{IS}.
(7) Dropout Voltage is defined as V_{DXX} (WLED Cathode) to GND voltage at which current into the LED drops 10% from the LED current at V_{DXX} = 0.2 V, WLED current = 15 mA × 4.
(8) As V_I drops, V_{DXX} eventually falls below the switchover threshold of 100mV, and TPS60251 switches to 1.5× mode. See the *Operating Principle* section for details about the mode transition thresholds.

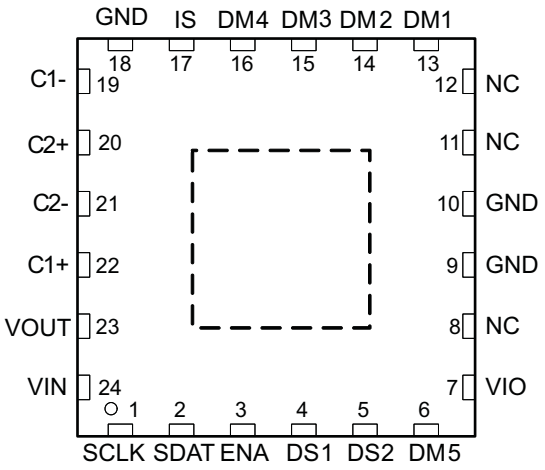
ELECTRICAL CHARACTERISTICS (continued)

V_I = 3.5 V, T_A = –40°C to 85°C, R_{IS} = 562 kΩ, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su(STO)}$	STOP condition setup time			600		ns
$t_{(BUF)}$	Bus free time			1300		ns
I²C COMPATIBLE INTERFACE VOLTAGE SPECIFICATION (SCLK, SDAT, VIO)						
V_{IO}	Serial bus voltage level		1.4		4.5	V
V_{IL}	Low-level input voltage	3.0V ≤ V_I ≤ 6.0V, 1.4 V < V_{IO} < 1.8 V	0		0.37×V_{IO}	V
V_{IH}	High-level input voltage	3.0V ≤ V_I ≤ 6.0V	0.87×V_{IO}			V
V_{OL}	Low-level output voltage	I_{LOAD} = 2 mA			0.4	V

PIN ASSIGNMENTS

QFN 24-PIN RTW
4mm x 4mm
(TOP VIEW)



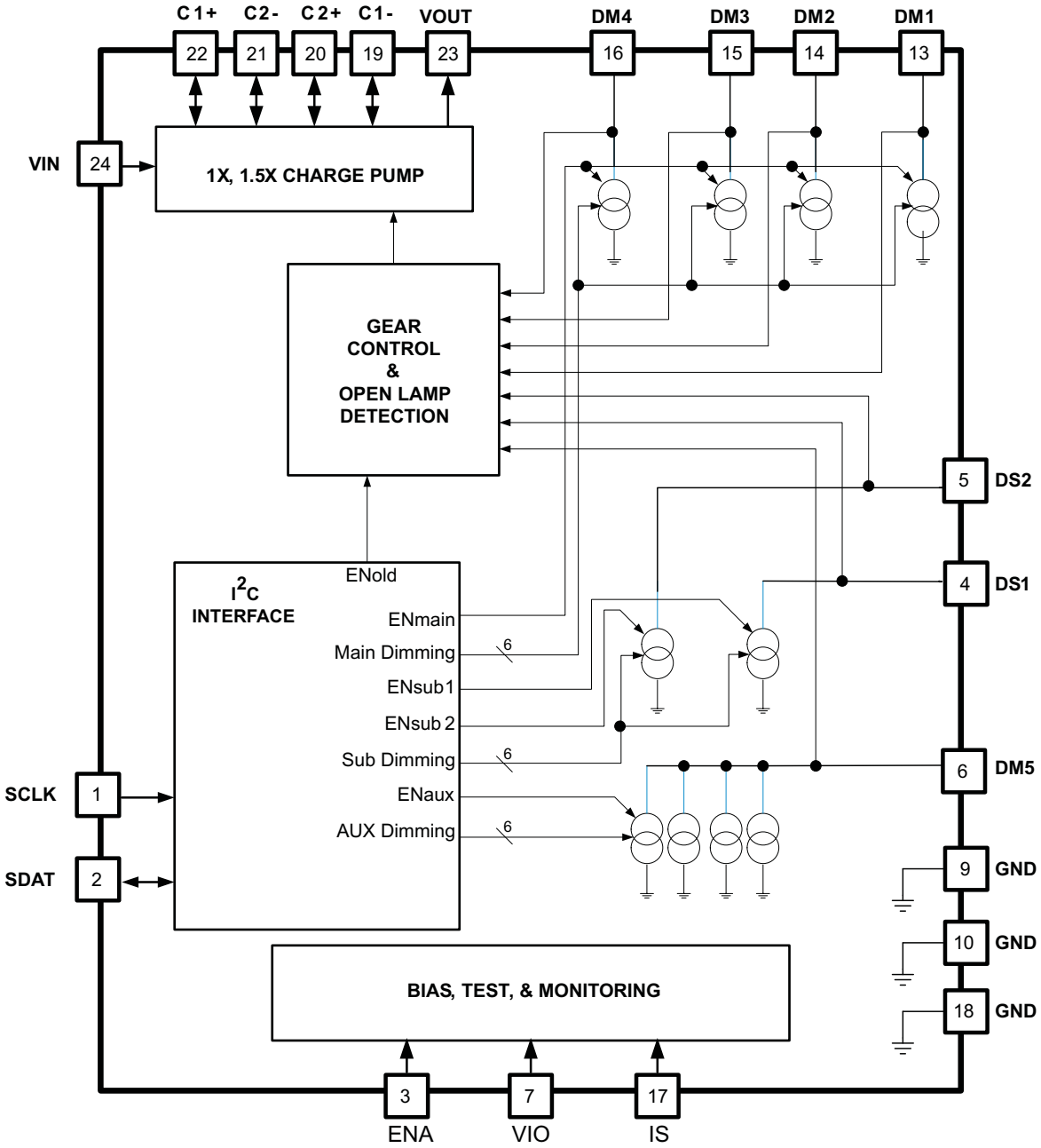
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
SCLK	1	I	I²C Interface
SDAT	2	I/O	I²C Interface
ENA	3	I	Hardware enable/disable pin. Connect this pin high to enable the device. Connect this pin low to disable the device. Do not leave this pin unconnected.
DS1	4	I	Current sink input. Connect the cathode of one of the sub display white LEDs to this pin.
DS2	5	I	
DM5	6	I	Current sink input. Connect the cathode of the aux display or the 5th main display white LED to this pin.
VIO	7	I	I/O Voltage input (1.8V). Connect an input voltage supply of 1.8V to VIN to set the logic levels for the I²C interface.
NC	8, 11, 12	–	No connection
GND	9, 10, 18	–	Ground
DM1	13	I	Current sink input. Connect the cathode of one of the main display white LED to this pin.
DM2	14	I	
DM3	15	I	
DM4	16	I	
IS	17	I	Maximum LED current setting input. Connect a resistor (R_{IS}) between this pin and GND to set the full-scale white LED current for sub (DS1, DS2), main (DM1, DM2, DM3, DM4), and DM5 LEDs. See the *Setting the LED Current* section for details on selecting the correct value for R_{IS}.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
C1–	19	–	Connect to the flying capacitor C1
C2+	20	–	Connect to the flying capacitor C2
C2–	21	–	Connect to the flying capacitor C2
C1+	22	–	Connect to the flying capacitor C1
VOUT	23	O	Connect the anodes of the sub, main, and aux display white LEDs to this pin. Bypass VOUT to GND with a 4.7-µF or greater ceramic capacitor.
VIN	24	I	Supply voltage input. Connect to a 3-V to 6-V input supply source. Bypass VIN to GND with a 4.7-µF or greater ceramic capacitor.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

DESCRIPTION		REF
Efficiency	Efficiency vs Input Voltage, 4 Main LED - 15mA, 25mA	Figure 3
	Efficiency vs Input Voltage, 2 Sub LED with Light Load Condition, ×1 Mode Operation	Figure 4
Output Impedance of ×1 and ×1.5 Mode	Switch Resistance vs Free-Air Temperature, ×1 Mode, I_{LED} = 230 mA	Figure 5
	Switch Resistance vs Free-Air Temperature, ×1 Mode, I_{LED} = 100 mA	Figure 6
	Switch Resistance vs Free-Air Temperature, ×1.5 Mode Charge Pump Open-Loop , I_{LED} = 230 mA	Figure 7
	Switch Resistance vs Free-Air Temperature, ×1.5 Mode Charge Pump Open-Loop, I_{LED} = 100 mA	Figure 8
Shutdown Current	Shutdown Current vs Input Voltage	Figure 9
Input Current	Input Current vs Supply Voltage, 4 Main LED	Figure 10
DM5 with Maximum 80 mA	DM5 Current vs Input Voltage, Programmed with 80 mA	Figure 11
Current Accuracy	WLED Current vs Input Voltage, 4 Main LED with 15 mA	Figure 12

EFFICIENCY vs INPUT VOLTAGE (4 Main LED - 15mA, 25mA)

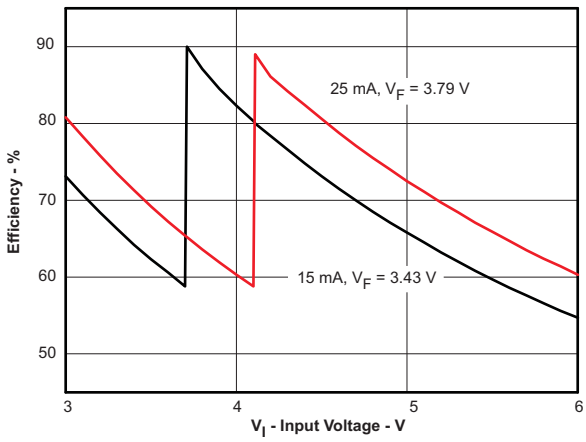


Figure 3.

EFFICIENCY vs INPUT VOLTAGE (2 Sub LED with Light Load Condition, ×1 Mode Operation)

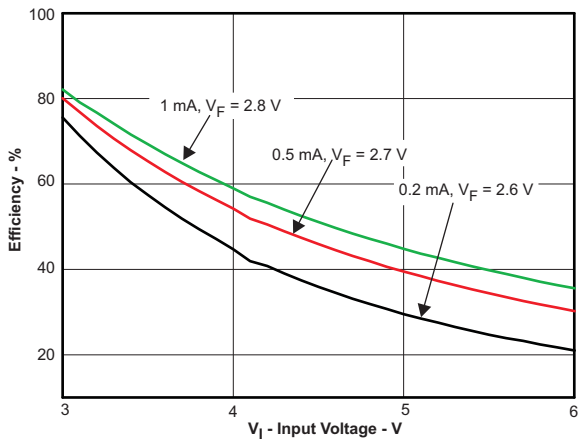


Figure 4.

SWITCH RESISTANCE vs FREE-AIR TEMPERATURE (×1 Mode)

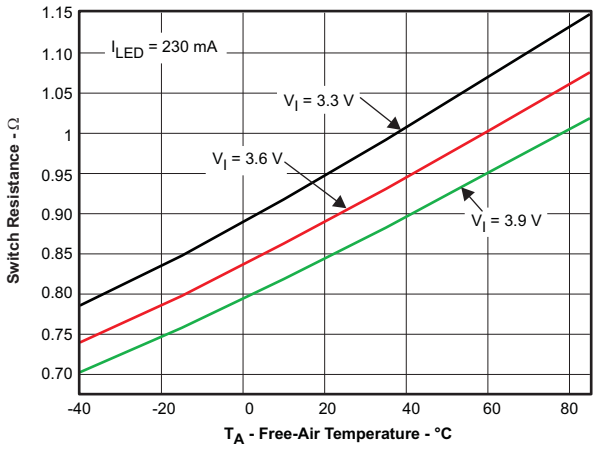


Figure 5.

SWITCH RESISTANCE vs FREE-AIR TEMPERATURE (×1 Mode)

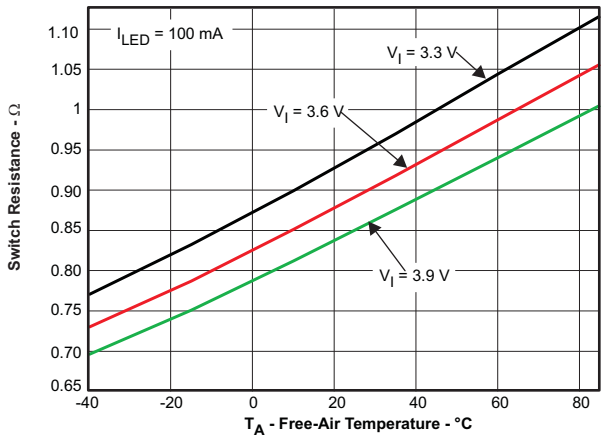


Figure 6.

SWITCH RESISTANCE vs FREE-AIR TEMPERATURE (×1.5 Mode Charge Pump Open-Loop)

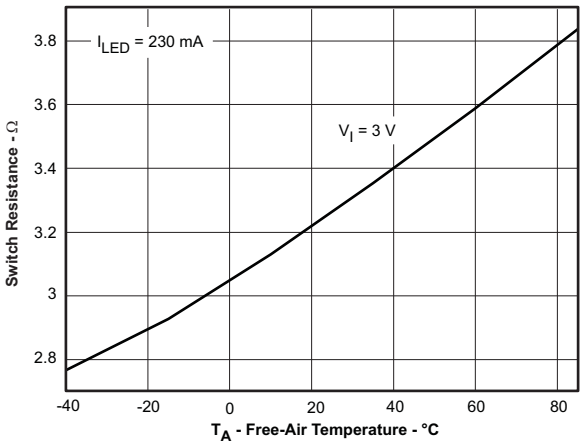


Figure 7.

SWITCH RESISTANCE vs FREE-AIR TEMPERATURE (×1.5 Mode Charge Pump Open-Loop)

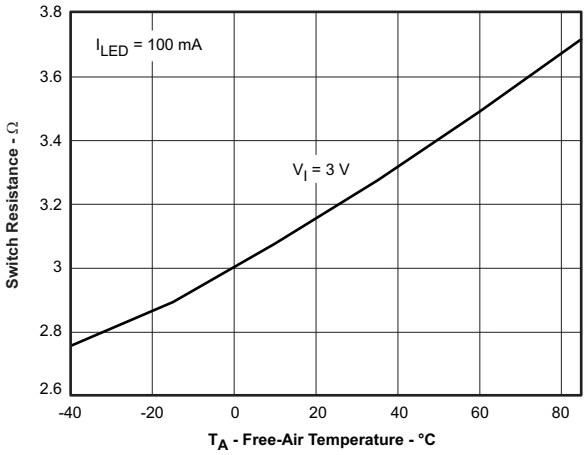


Figure 8.

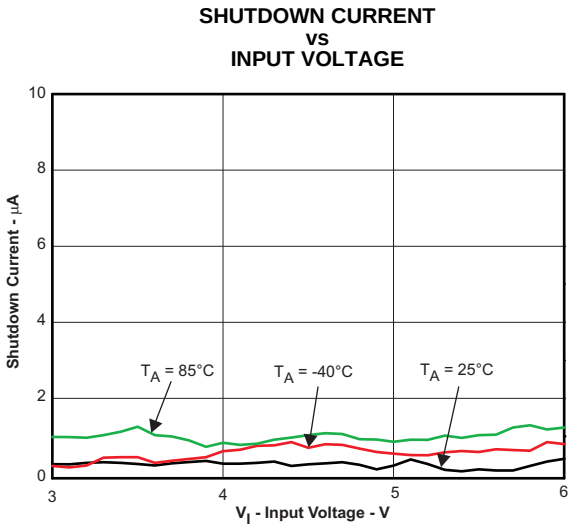


Figure 9.

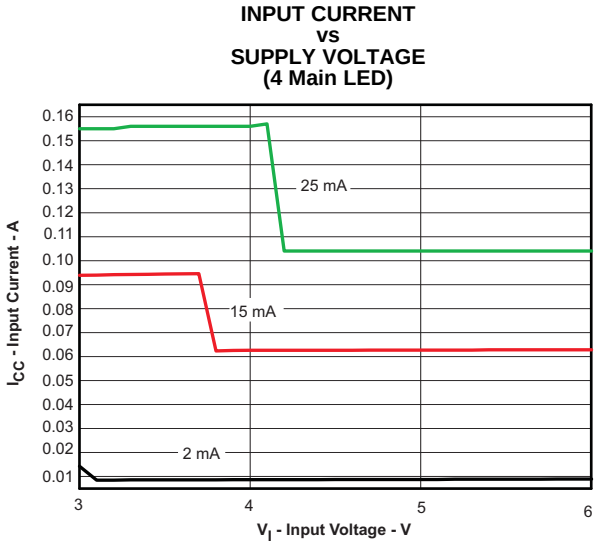


Figure 10.

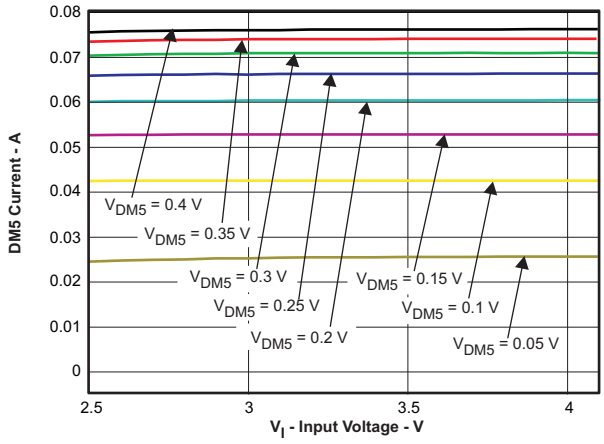


Figure 11.

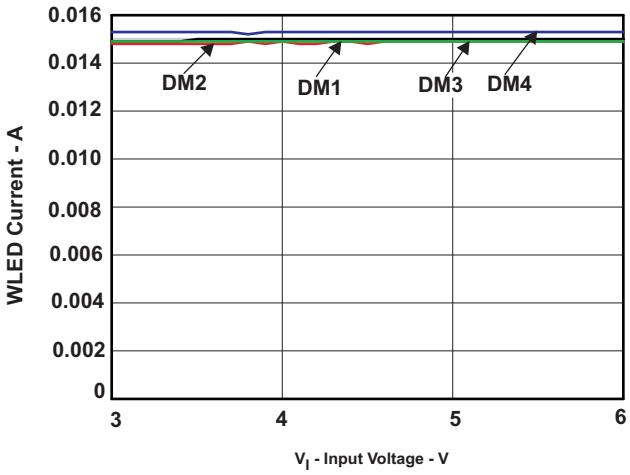


Figure 12.

APPLICATION INFORMATION

APPLICATION OVERVIEW

Most of the current handsets fall into one of three categories. First is the clamshell design, with a main display on the inside, a secondary display on the outside and a keypad backlight. Second is the bar design, with a main display and a keypad backlight. Third is the slide type (slide-up and slide-down) design, with a main display and two keypad banks (inside and outside). The TPS60251 is well suited for use in these three major phone designs because it has 7 individually regulated white LED current paths for driving up to five white LEDs in main display and up to two white LEDs in sub display with regulated constant current for uniform intensity. The main and sub display LED channels drive up to 25mA and an auxiliary LED output (DM5) drives up to 80mA that can be assigned for keypad backlight, torch light or low cost/weak camera flash application using the I^2C interface.

The TPS60251 circuit uses only 5 external components: the input/output capacitors, 2 chargepump flying capacitors, and one resistor that sets the maximum WLED current. The few external components combined with the small 4mm×4mm QFN package provide for a small total solution size. By combining independent control of three separate banks of backlight LEDs with low cost and weak flash capability, the TPS60251 helps designers minimize power consumption especially in light load conditions while reducing component count and package size.

OPERATING PRINCIPLE

Charge pumps are becoming increasingly attractive in battery-operated applications where board space and maximum height of the converter are critical constraints. The major advantage of a charge pump is the use of only capacitors as storage elements. The TPS60251 chargepump provides regulated LED current from a 3-V to 6-V input source. It operates in two modes. The 1× mode, where the input is connected to the output through a pass element, and a high efficiency 1.5× charge pump mode. The IC maximizes power efficiency by operating in 1× and 1.5× modes as input voltage and LED current conditions require. The mode of operation is automatically selected by comparing the forward voltage of the WLED plus the voltage of current sink for each LED with the input voltage. The IC starts up in 1× mode, and automatically transitions to 1.5× if the voltage at any current sink input (DM_or DS_) falls below the 100-mV transition voltage. The IC returns to 1× mode as the input rises. Figure 13 provides a visual explanation of the 1× to 1.5× transition.

In 1.5× mode, the internal oscillator determines the charge/discharge cycles for the flying capacitors. During a charge cycle, the flying capacitors are connected in series and charged up to the input voltage. After the on-time of the internal oscillator expires, the flying capacitors are reconfigured to be in parallel and then connected in series to the input voltage. This provides an output of 1.5× the input voltage. After the off-time of the internal oscillator expires, another charge cycle initiates and the process repeats.

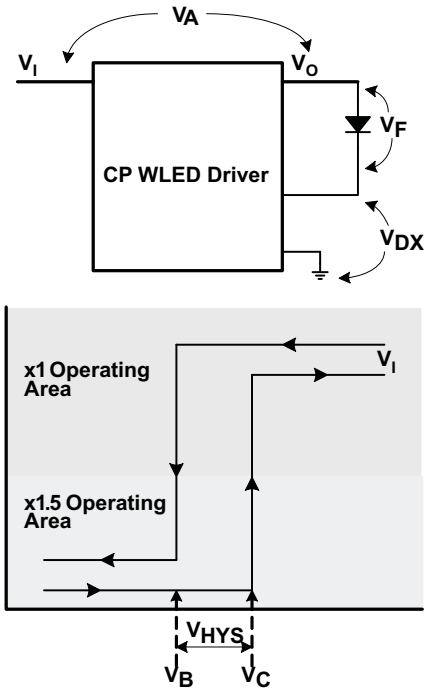


Figure 13. Input Voltage Hysteresis Between ×1 and ×1.5 Mode

As shown in Figure 13, there is input voltage hysteresis voltage between 1× and 1.5× mode to ensure stable operation during mode transition. For the 1 cell Li-Ion battery input voltage range, the TPS60251 operates in 1× mode when a fully charged battery is installed. Once the battery voltage drops below the V_B level, which is the mode transition voltage from 1× to 1.5×, the WLED driver operates in 1.5× mode. Once in 1.5× mode, the battery voltage must rise to the V_C level in order to transition from 1.5× to 1×. This hysteresis ensures stable operation when there is some input voltage fluctuation at the 1×/1.5× mode transition. The WLED driver provides a typical 280mV hysteresis voltage (V_{HYS}) that changes based on LED current, to prevent oscillating between modes.

The transition voltage, V_B, depends on V_{DX} (the mode transition threshold voltage), V_F (WLED forward voltage drop) and V_A (the drop out voltage of the charge pump stage) and is calculated as follows:

$V_B = V_A + V_F + V_{DX}$

$V_A = R_{OUT1X} \times I_{LEDTOTAL}$

Where R_{OUT1X} is the 1× mode output impedance of the IC. See the Electrical Characteristics table for output impedance specifications.

The TPS60251 switches to 1.5× mode when the input voltage is below V_B and remains in 1.5× mode as long as the input is lower than V_C. 1.5× Mode is exited when the input voltage rises above V_C. V_C is calculated as:

$V_C = V_F + 550$ mV

The input voltage mode transition hysteresis voltage (V_{HYS}) between 1× and 1.5× is calculated using the following equation.

$V_{HYS} = V_C – V_B = 550$ mV $– V_{DX} – V_A$, where $V_{DX} = 100$ mV

Note that V_A is the key factor in determining V_{HYS} and is dependant on the 1× mode charge pump output impedance and WLED current.

LED CURRENT SINKS (DM_, DS_)

The TPS60251 has constant current sinks which drive seven individual LED current paths. Each current sink regulates the LED current to a constant value determined by the I^2C interface. The internal register addressing allows the LED main channels DM1~DM5 to be controlled independently from the LED sub channels DS1~DS2. The maximum current is programmable by the user (see the *Setting the LED Current* section). All the LED channels sink up to 25mA of current except DM5 which has an 80-mA maximum current when configured as an

auxiliary output. Using the I^2C interface, the user may assign DM5 to the main display bank with up to 25-mA current or as an auxiliary output for torch or keypad light or low/weak camera flash with 80-mA current. DM5 has 64 dimming steps which is the main and sub display banks when assigned to the main display. However, it has its own current programming register and enable control. When assigned as an auxiliary, DM5 has 4 dimming steps (full scale, 70%, 40%, 20%).

These optimized current sinks minimize the voltage headroom required to drive each LED and maximize power efficiency by increasing the amount of time the controller stays in 1× mode before transitioning to 1.5× mode.

OPEN LAMP DETECTION

In system production it is often necessary to leave LED current paths open depending on the phone model. For example, one phone may use 2 LEDs to backlight the main display while another uses 4 LEDs. Rather than use two different ICs for these different phone applications, the TPS60251 may be used in both applications with no additional efficiency loss in the 2 LED applications. In traditional LED driver applications when an LED current path is open, the current sink voltage falls to ground and the current regulation circuitry drives the output to a maximum voltage in an attempt to regulate the current for the missing LED path. This severely reduces the system efficiency. The TPS60251 uses 7 internal comparators to detect when an open LED condition occurs and shut down the open current sink. The open lamp detection is enabled/disabled using the I^2C interface.

ENABLING THE DEVICE

The TPS60251 contains a hardware enable input for situations where the IC cannot be disabled using the I^2C interface. Connect the EN input high to enable the device for normal operation. Connect EN low to disable the device and place it in a low power shutdown. The hardware enable overrides the I^2C enable. When EN is pulled low, the TPS60251 is completely disabled (shutdown mode) and all internal registers are set to 0x00h while the software shutdown using I^2C keeps all internal registers.

ENABLING THE LED BANKS

The I^2C interface is used to enable/disable the LED banks. The MAIN, SUB, and AUX LEDs are individually controlled. Additionally, the two SUB LEDs (DS_) can be enabled independently.

CAPACITOR SELECTION

The TPS60251 is optimized to work with ceramic capacitors with a dielectric of X5R or better. The two flying capacitors must be the same value for proper operation. The 750-kHz switching frequency requires that the flying capacitor be less than 4.7µF. Use of 1-µF ceramic capacitors for both chargepump flying capacitors is recommended.

For good input voltage filtering, low ESR ceramic capacitors are recommended. A 1-µF ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering this value can be increased to 4.7 µF.

The output capacitor controls the amount of ripple on the output. Since small ripple is undetectable by the human eye, a 4.7-µF output capacitor works well. If better output filtering and lower ripple is desired, a larger output capacitor may be used.

I/O INPUT

The input logic low and high threshold voltage for I^2C interface is changed by supplying voltage to VIO. The voltage range of VIO is 1.8V to V_I. This allows the user to optimize the input logic low and high I^2C threshold voltages for the TPS60251 to cover different voltage levels for I^2C interface for the various phone models.

SETTING THE LED CURRENT

The maximum LED current is user programmable using the IS input. Connect a resistor from IS to GND to set the maximum LED current. The resistor value is calculated using the following equation between 2mA and 25.5mA:

$$I_{LED}(\mu A) = \left[\left(\frac{1.254}{R_{IS}} + 1.276 \times 10^{-6}\right) \times \frac{Step \times 500}{3.5 \times 10^{-6}}\right] - \left(\frac{1.254}{R_{IS}} + 1.276 \times 10^{-6}\right) \times 1714.29 \times 10^{6} \quad (1)$$

Where R_{IS} is the resistor from IS to GND, I_{LED} is the LED current in μA and Step is the dimming step set by the I^2C interface (1 to 63). I_{LED} may be set up to 25mA (R_{IS} = 562 kΩ).

R_{IS} has an effect on the current steps that are programmed using the I^2C. When the current is programmed below 1.5mA, the current is determined by the following equation:

$$I_{LED}(\mu A) = \left(\frac{1.254}{R_{IS}} + 1.276 \times 10^{-6}\right) \times \frac{Step \times 100}{3.5 \times 10^{-6}} \quad (2)$$

This equation provides a greater resolution in current steps at lower currents.

STEP	ILED	STEP	ILED	STEP	ILED	STEP	ILED
1	100μA	17	2.5mA	33	10.5mA	49	18.5mA
2	200μA	18	3.0mA	34	11.0mA	50	19.0mA
3	300μA	19	3.5mA	35	11.5mA	51	19.5mA
4	400μA	20	4.0mA	36	12.0mA	52	20.0mA
5	500μA	21	4.5mA	37	12.5mA	53	20.5mA
6	600μA	22	5.0mA	38	13.0mA	54	21.0mA
7	700μA	23	5.5mA	39	13.5mA	55	21.5mA
8	800μA	24	6.0mA	40	14.0mA	56	22.0mA
9	900μA	25	6.5mA	41	14.5mA	57	22.5mA
10	1.0mA	26	7.0mA	42	15.0mA	58	23.0mA
11	1.1mA	27	7.5mA	43	15.5mA	59	23.5mA
12	1.2mA	28	8.0mA	44	16.0mA	60	24.0mA
13	1.3mA	29	8.5mA	45	16.5mA	61	24.5mA
14	1.4mA	30	9.0mA	46	17.0mA	62	25.0mA
15	1.5mA	31	9.5mA	47	17.5mA	63	25.5mA
16	2.0mA	32	10.0mA	48	18.0mA		

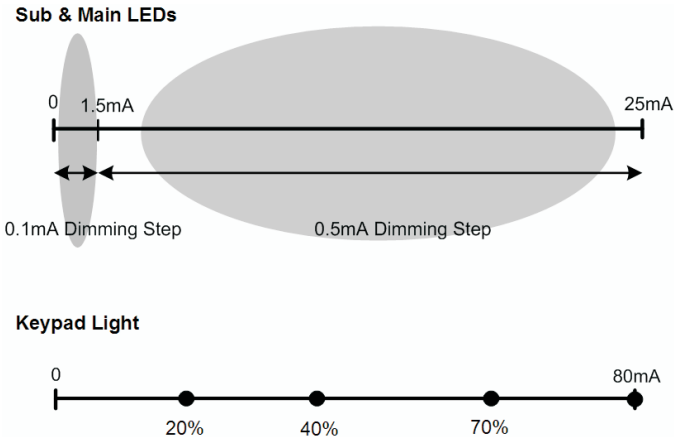


Figure 14. Dimming Steps for Sub, Main, and Keypad Backlight

Figure 14 shows the dimming steps for sub, main, and auxiliary display banks in the 25mA maximum current application. To satisfy today's requirements on LED current, the TPS60251 covers low LED current area from 100μA to 1.5mA with 100-μA dimming step (total 16 steps for 25-mA maximum current) for the new LCD panels which have improved transparency rates. For LED currents in the range from 2mA to 25mA, the device uses 48 dimming steps with 0.5mA step. Also, DM5 has 4 dimming steps once the current path is assigned for auxiliary applications with maximum 80-mA current.

R_{IS} also affects the current for the auxiliary application. The four current levels (20%, 40%, 70%, and 100%) are determined by the following equations:

$$I_{AUX}(100\%) = \left[\left(\frac{1.254}{R_{IS}} + 1.276 \times 10^{-6}\right) \times \frac{8000}{3.5 \times 10^{-6}}\right] \times 10 \quad (3)$$

$$I_{AUX}(70\%) = \left[\left(\frac{1.254}{R_{IS}} + 1.276 \times 10^{-6}\right) \times \frac{6000}{3.5 \times 10^{-6}}\right] \times 9.333 \quad (4)$$

$$I_{AUX}(40\%) = \left[\left(\frac{1.254}{R_{IS}} + 1.276 \times 10^{-6}\right) \times \frac{4000}{3.5 \times 10^{-6}}\right] \times 8 \quad (5)$$

$$I_{AUX}(20\%) = \left[\left(\frac{1.254}{R_{IS}} + 1.276 \times 10^{-6}\right) \times \frac{2000}{3.5 \times 10^{-6}}\right] \times 8 \quad (6)$$

SERIAL INTERFACE

The serial interface is compatible with the standard and fast mode I^2C specifications, allowing transfers at up to 400 kHz. The interface adds flexibility to the WLED driver solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as V_{CC} remains above UVLO2 (typical 1.3V) and ENA is high.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS60251 device generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TPS60251 device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS60251 device must leave the data line high to enable the master to generate the stop condition.

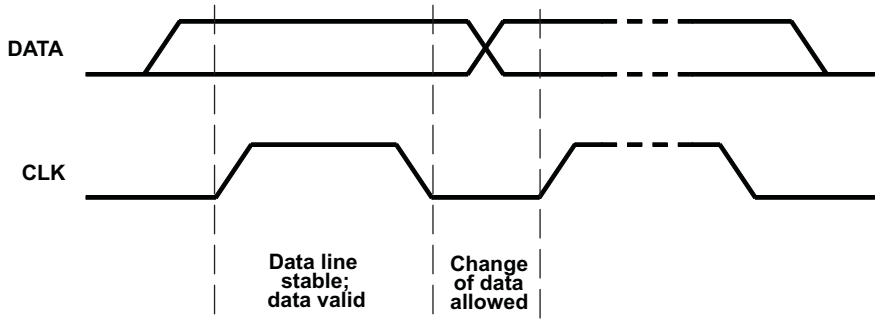


Figure 15. Bit Transfer on the Serial Interface

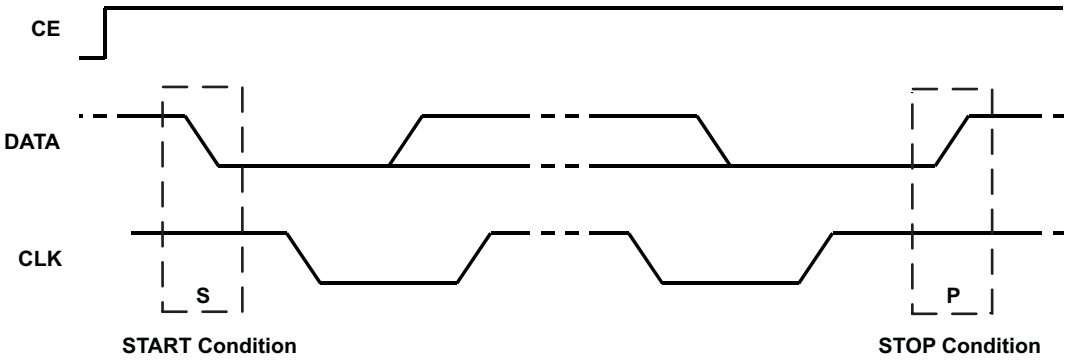


Figure 16. START and STOP Conditions

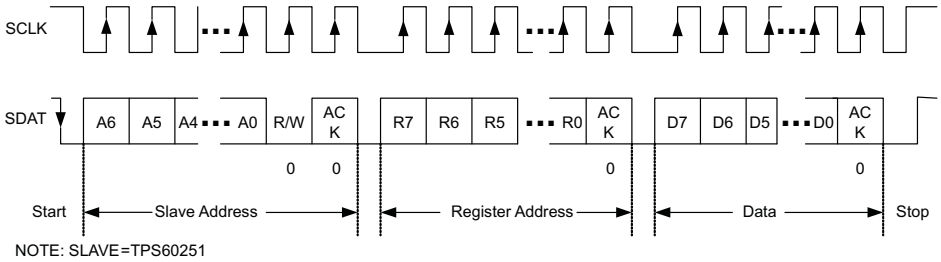


Figure 17. Serial I/F READ From TPS60251: Protocol A

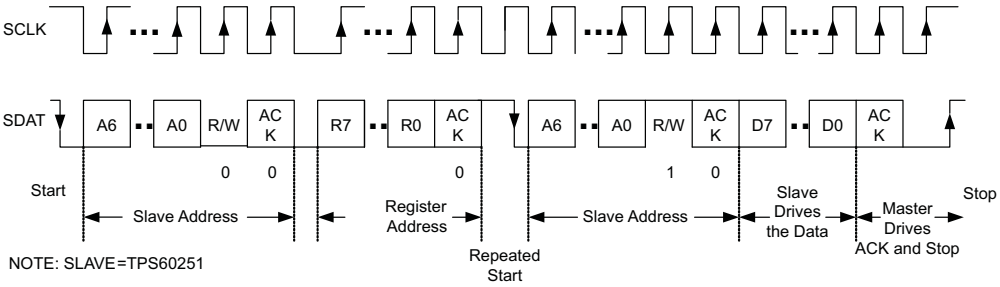


Figure 18. Serial I/F READ From TPS60251: Protocol B

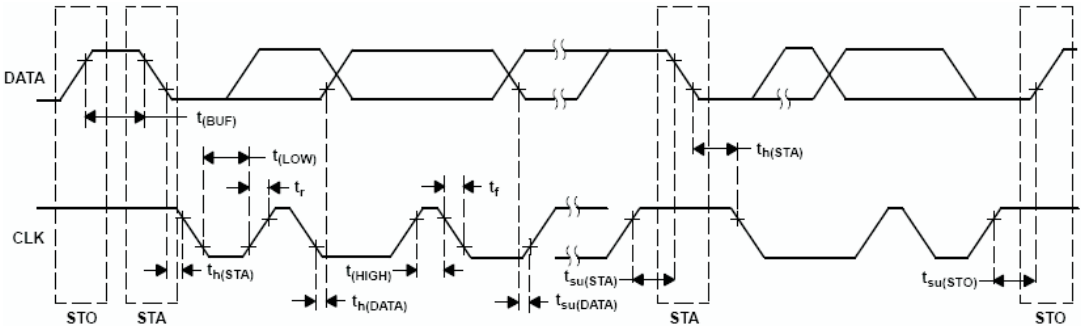


Figure 19. Serial I/F Timing Diagram

The I^2C interface uses a combined protocol in which the START condition and the Slave Address are both repeated. The TPS60251 provides 2 I^2C Slave Address using internal EEPROM in case more than 1 device is used in the system. The primary I^2C Slave Address is **1110111**. For the alternative I^2C address, contact the factory.

Enable Control Register (Address: 0x00h)

ENABLE	B7	B6	B5	B4	B3	B2	B1	B0
BIT NAME	X	ENold	ENmain	ENsub2	ENsub1	ENaux	DM5H	DM5L

Bit 6 ENold (Enable Open Lamp Detection)
1: Open Lamp Detection Enabled
0: Open Lamp Detection Disabled

Bit 5 ENmain
1: Enable Main Display LEDs (DM1-DM4)
0: Disable Main Display LEDs

Bit 4 ENsub2
1: Enable Sub Display LED 2 (DS2)
0: Disable Sub Display LED 2

Bit 3 ENsub1
1: Enable Sub Display LED 1 (DS1)
0: Disable Sub Display LED 1

Bit 2 ENaux
1: Enable Aux Display LED (DM5)
0: Disable Aux Display LED

Bits 1,0 DM5H, DM5L

DM5H (B1)	DM5L (B0)	DM5 Mode and Shutdown Mode
0	0	Shutdown mode. All outputs disabled, all internal registers set to 0x00h
0	1	Enable the IC and Group DM5 as main display with maximum current of 25mA
1	0	Enable the IC and set as Aux output with maximum current of 80mA. Dimming steps determined by Iaux0 and Iaux1 bits.
1	1	Shutdown mode. All outputs disabled, all internal registers set to 0x00h

Sub Display Current Control Register (Address: 0x01h)

SUB DISP CURRENT	B7	B6	B5	B4	B3	B2	B1	B0
BIT NAME	X	X	Isub5	Isub4	Isub3	Isub2	Isub1	Isub0

Bits 5 - 0 Isub5 - Isub0 (total 64 steps)
6-Bit command (64 steps) to these bits sets the current for DS1 and DS2.
For LED currents between 0 and 1.5mA, one step = 0.1mA increment
For LED currents between 1.5 and 25.5mA, one step = 0.5mA increment

Main Display Current Control Register (Address: 0x02h)

MAIN DISP CURRENT	B7	B6	B5	B4	B3	B2	B1	B0
BIT NAME	X	X	Imain5	Imain4	Imain3	Imain2	Imain1	Imain0

Bits 5 - 0 Imain5 - Imain0 (total 64 steps)
6-Bit command (64 steps) to these bits sets the current for DM1-DM4.
For LED currents between 0 and 1.5mA, one step = 0.1mA increment
For LED currents between 1.5 and 25.5mA, one step = 0.5mA increment

Aux Output Brightness and Operation Mode Control Register (Address: 0x03h)

AUX DISP CURRENT	B7	B6	B5	B4	B3	B2	B1	B0
BIT NAME	Iaux5	Iaux4	Iaux3	Iaux2	Iaux1	Iaux0	Mode1	Mode0

Bits 7 - 2 (DM5 set to Main Display Mode)

Iaux5 - Iaux0 (total 64 steps)
6-Bit command (64 steps) to these bits sets the current for DM5.
For LED currents between 0 and 1.5mA, one step = 0.1mA increment
For LED currents between 1.5 and 25.5mA, one step = 0.5mA increment

Bits 7 - 2 (DM5 set to Aux Display Mode)

Iaux5 (B7)	Iaux4 (B6)	Iaux3 (B5)	Iaux2 (B4)	Iaux1 (B3)	Iaux0 (B2)	Aux Dimming Step
X	X	X	X	0	0	20%
X	X	X	X	0	1	40%
X	X	X	X	1	0	70%
X	X	X	X	1	1	100%

Bits 1,0 Mode1, Mode0

Mode1 (B1)	Mode0 (B0)	TPS60251 Mode
0	0	Auto-Switchover Mode. The TPS60251 selects 1×/1.5× mode as described in the *Operating Principle* section.
0	1	1× Mode. TPS60251 remains in 1× mode regardless of the input voltage. LED current may not regulate at lower input voltages when in this mode.
1	0	1.5× Mode. TPS60251 remains in 1.5× mode regardless of the input voltage.
1	1	Auto-Switchover Mode. The TPS60251 selects 1×/1.5× mode as described in the *Operating Principle* section.

APPLICATION CIRCUITS

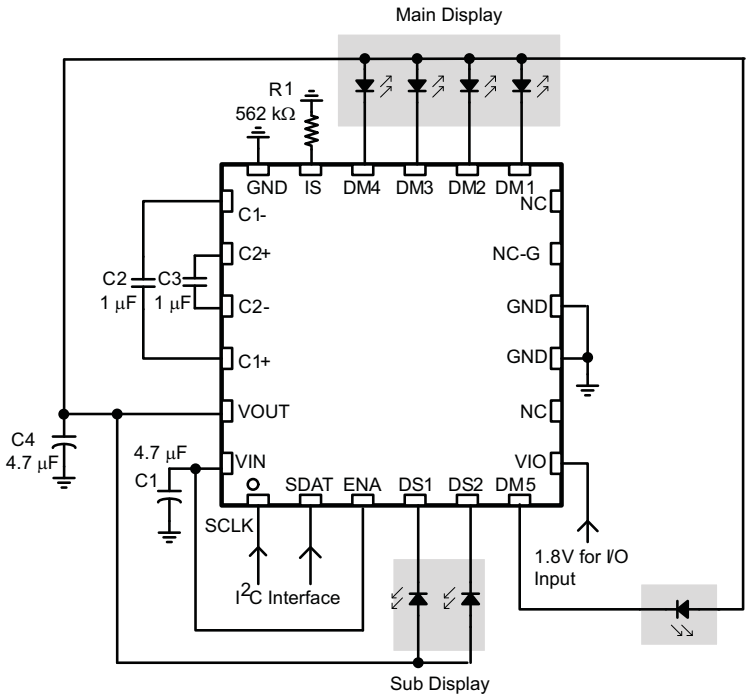


Figure 20. The Typical Application Circuit for Sub and Main Display

As shown in Figure 20, this is a typical application circuit for a clam shell phone with 5 main LEDs and 2 sub LEDs. Recently, the LCD panel makers have developed a new panel that has improved the transparency rate which makes system efficiency with a 100-µA LED current a critical load point. To meet system efficiency requirements with the light load conditions for the new LCD operating panel, the TPS60251 has a maximum 55-µA operating current with the 100-µA output load condition. In this application, the controller always operates in 1× mode due to the WLED's low forward voltage drop (about 2.6V_F with a 100-µA WLED current). Thus, the total efficiency at a light load condition is determined using Equation 7:

$$\eta_{Light} = \frac{I_O \times V_F}{V_{in} \times (I_O + I_{op})} \quad (7)$$

Where:

I_O: Output Load (WLED) Current
V_F: Forward Voltage Drop of WLED
V_{in}: Input Voltage
I_{op}: Operating Current of LED Driver

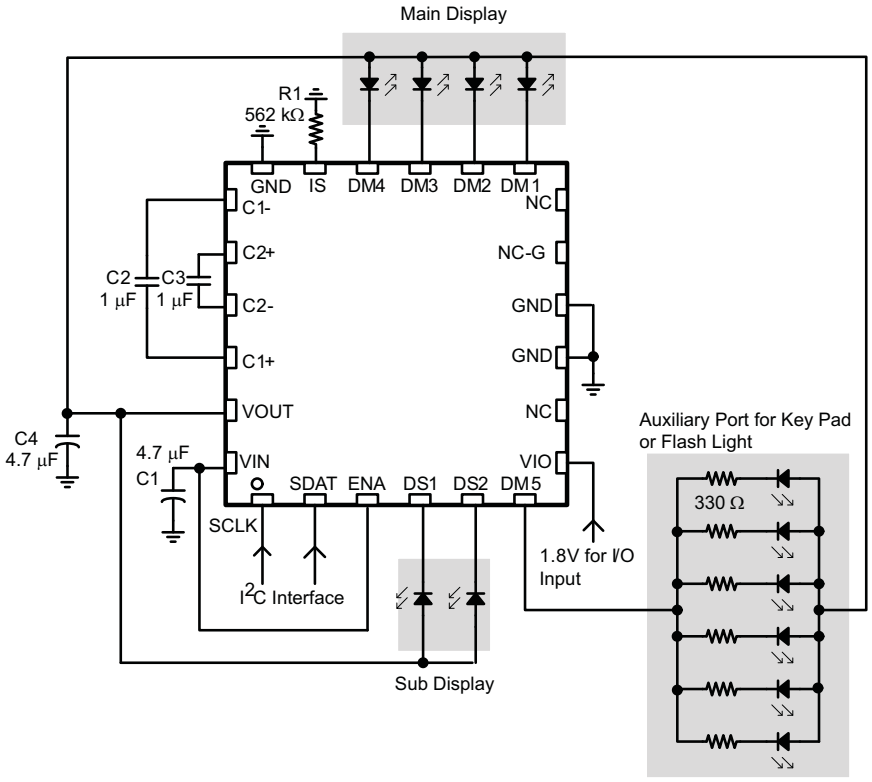


Figure 21. The Typical Application Circuit for Sub, Main, and Keypad Backlight

Figure 21 shows the typical application circuit for sub, main, and keypad backlight. In this application, DM5 is assigned as the auxiliary input for the keypad lighting application.

LAYOUT GUIDELINES

There are several points to consider when laying out a PCB for charge pump based solutions. In general, all capacitors should be as close as possible to the device. This is especially important when placing the flying capacitors (C2, C3 in Figure 20 and Figure 21). To provide accurate WLED current, the current path with the current setting resistor must be short to avoid any interference from other switching components. In cases where DM5 is assigned for torch/flash applications, with a maximum 80-mA WLED current, this current path must be kept wide to reduce the trace resistance.

Revision History

Changes from Revision B (October 2007) to Revision C	Page
• Changed LED to LED Current matching typ value from ±1% to ±0.1%	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS60251RTWR	ACTIVE	QFN	RTW	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60251RTWRG4	ACTIVE	QFN	RTW	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60251RTWT	ACTIVE	QFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60251RTWTG4	ACTIVE	QFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

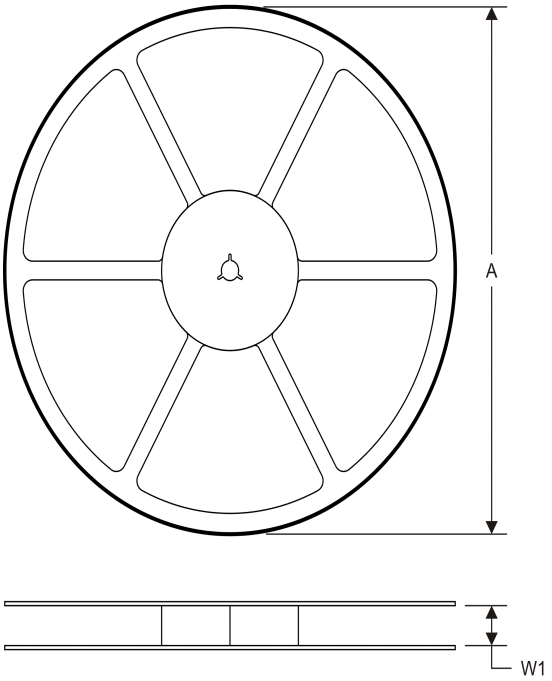
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

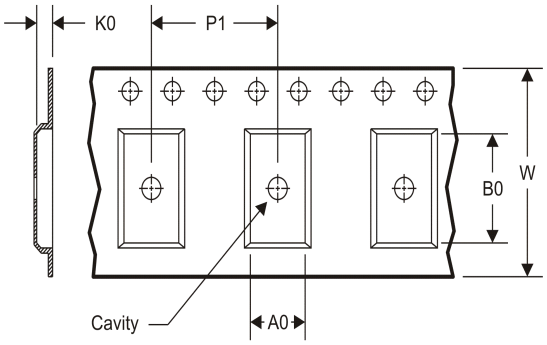
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



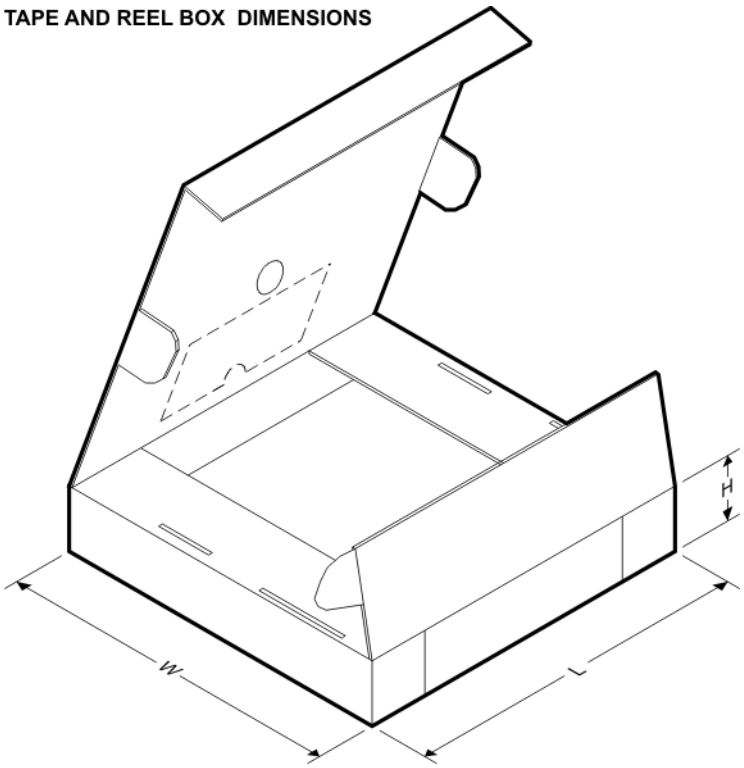
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60251RTWR	QFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS60251RTWT	QFN	RTW	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

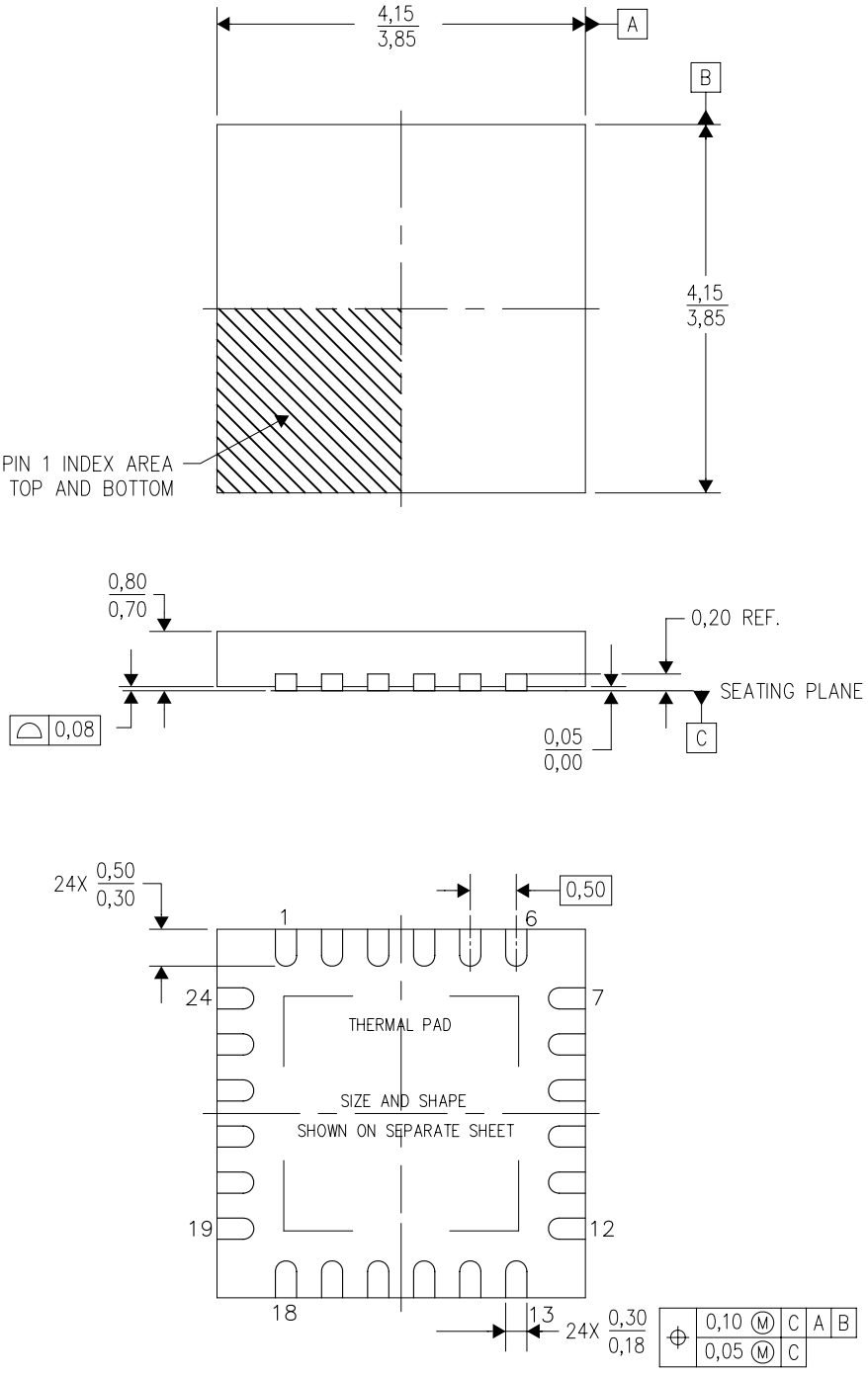
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60251RTWR	QFN	RTW	24	3000	346.0	346.0	29.0
TPS60251RTWT	QFN	RTW	24	250	210.0	185.0	35.0

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

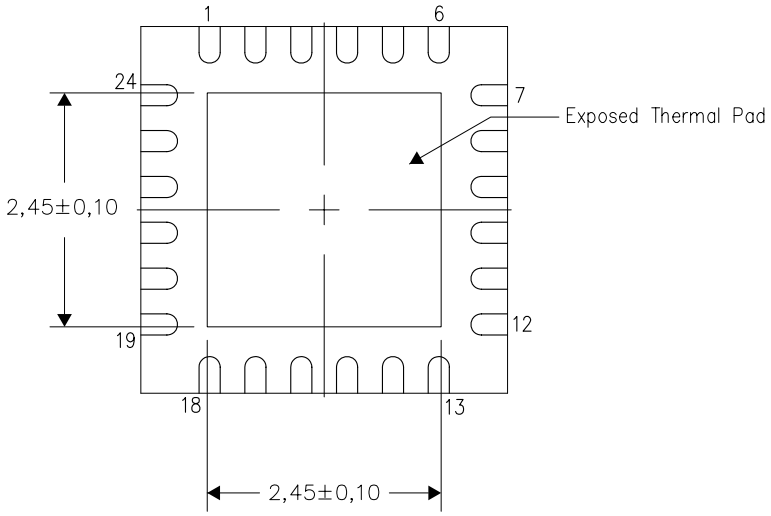
RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



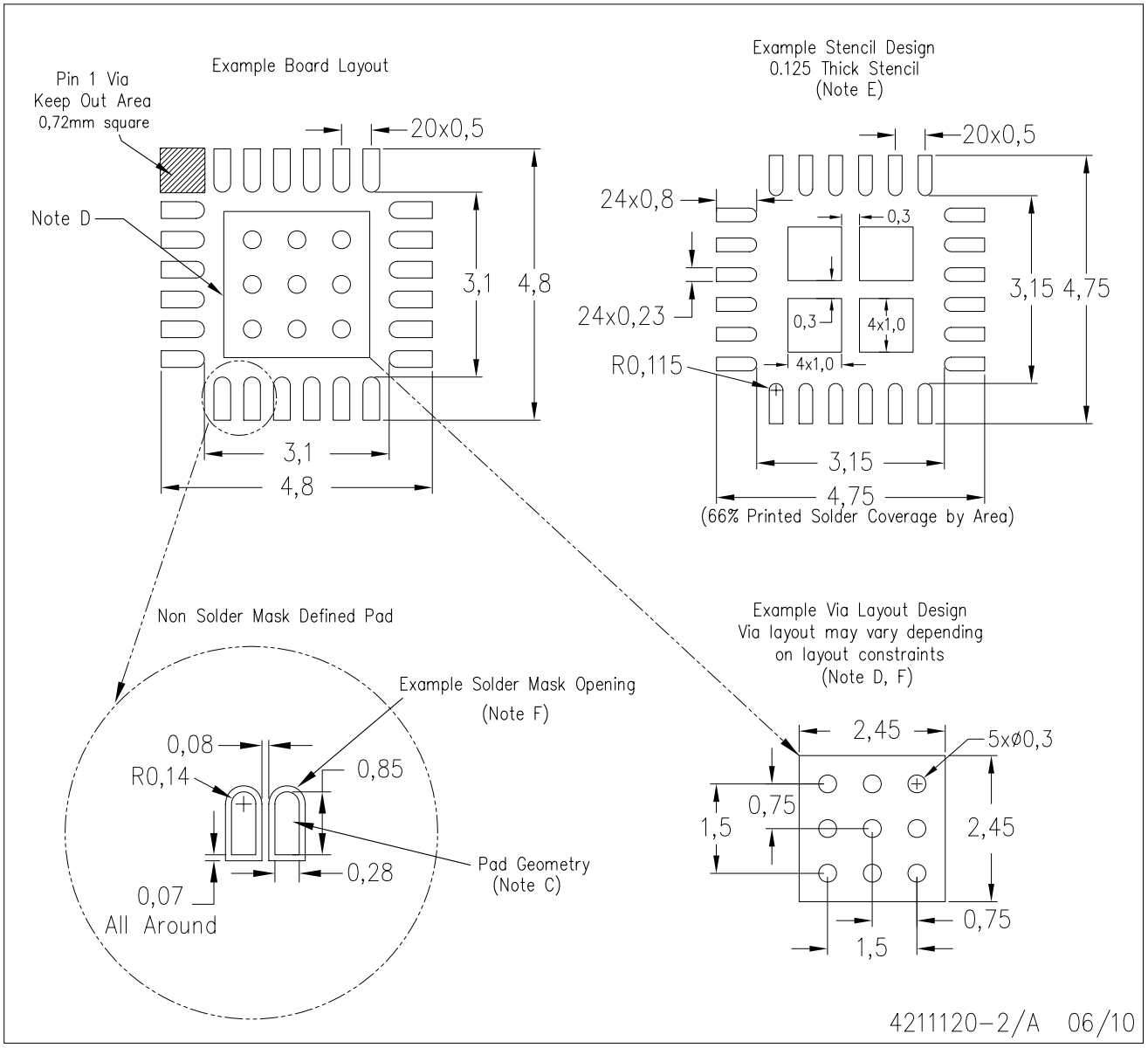
Bottom View

Exposed Thermal Pad Dimensions

4206249–3/L 07/11

NOTES: A. All linear dimensions are in millimeters

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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