#### SN54ALS576B, SN54AS576 SN74ALS576B, SN74ALS577A, SN74AS576 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS065B - DECEMBER 1982 - REVISED JANUARY 1995

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- SN74ALS577A Has Synchronous Clear
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N, NT) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages

#### description

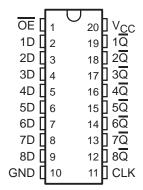
These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These flip-flops enter data on the low-to-high transition of the clock (CLK) input.

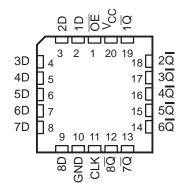
The output-enable  $(\overline{OE})$  input does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are disabled.

The SN54ALS576B and SN54AS576 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS576B, SN74ALS577A, and SN74AS576 are characterized for operation from 0°C to 70°C.

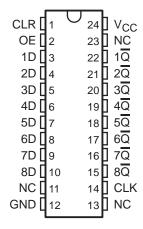
SN54ALS576B, SN54AS576 . . . J OR W PACKAGE SN74ALS576B, SN74AS576 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS576B, SN54AS576 . . . FK PACKAGE (TOP VIEW)



SN74ALS577A . . . DW OR NT PACKAGE (TOP VIEW)



NC – No internal connection

#### **Function Tables**

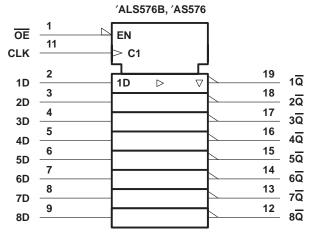
'ALS576B, 'AS576 (each flip-flop)

	INPUTS		OUTPUT
OE	CLK	D	Q
L	$\uparrow$	Н	L
L	$\uparrow$	L	Н
L	L	Χ	$\overline{Q}_0$
Н	X	Χ	Z

## SN74ALS577A (each flip-flop)

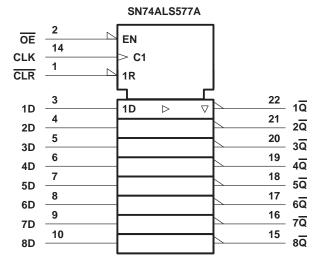
	INP	UTS		OUTPUT
OE	CLR	D	Q	
L	L	1	Χ	Н
L	Н	$\uparrow$	Н	L
L	Н	$\uparrow$	L	Н
L	Н	L	Χ	$\overline{Q}_0$
Н	Χ	Χ	Χ	Z

#### logic symbols†



<sup>†</sup> These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

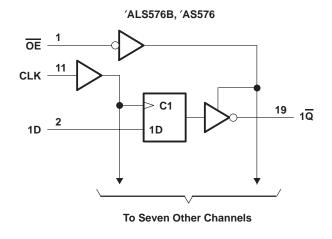
Pin numbers shown for the 'ALS576B and 'AS576 are for the DW, J, N, and W packages.

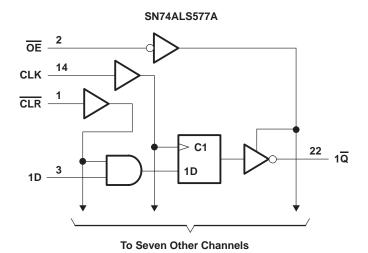


Pin numbers shown for the SN74ALS577A are for the DW and NT packages.

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#### logic diagrams (positive logic)





Pin numbers shown are for the DW, J, N, and W packages.

Pin numbers shown are for the DW and NT packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V <sub>CC</sub>	$\dots \dots \dots \ 7 \ V$
Input voltage, V <sub>I</sub>	$\dots \dots \dots \ 7 \ V$
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T <sub>A</sub> : SN54ALS576B	
SN74ALS576B, SN74ALS577A	0°C to 70°C
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

			SNS	54ALS57	′6B		74ALS57 74ALS57		UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
loн	High-level output current				-1			-2.6	mA
loL	Low-level output current				12			24	mA
,	Olarah (na marana	'ALS576B	0		22	0		30	N41.1-
fclock	Clock frequency	SN74ALS577A				0		30	MHz
	5	'ALS576B, CLK high or low	25			16.5			
t <sub>W</sub>	Pulse duration	SN74ALS577A, CLK high or low				16.5			ns
	2	Data	15			15			
t <sub>su</sub>	Setup time before CLK↑	SN74ALS577A CLR				15			ns
		Data	4			0			
th	Hold time after CLK↑	SN74ALS577A CLR				0			ns
TA	Operating free-air temperature		-55		125	0		70	°C



### SN54ALS576B, SN54AS576 SN74ALS576B, SN74ALS577A, SN74AS576 OCTAL D-TYPÉ EDGE-TRIGGÉRED FLIP-FLOPS WITH 3-STATE OUTPUTS

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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	SNS	4ALS57	'6B		4ALS57 4ALS57	-	UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX	
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = –18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	VCC -2	2		V <sub>CC</sub> -2			
VOН	V 45V	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	V <sub>CC</sub> = 4.5 V	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
V	V 45V	I <sub>OL</sub> = 12 mA		0.25	0.4		0.25	0.4	V
VOL	V <sub>CC</sub> = 4.5 V	$I_{OL} = 24 \text{ mA}$					0.35	0.5	V
lozh	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.7 \text{ V}$			20			20	μΑ
lozL	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.4 V			-20			-20	μΑ
lj	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V			0.1			0.1	mA
lН	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20			20	μΑ
I <sub>IL</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 0.4 V			-0.2			-0.2	mA
I <sub>O</sub> ‡	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.25 V	-20		-112	-30		-112	mA
		Outputs high		10	18		10	18	
Icc	V <sub>CC</sub> = 5.5 V	Outputs low		15	24		15	24	mA
		Outputs disabled		16	30		16	30	

#### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		(   	V <sub>CC</sub> = 4.5 C <sub>L</sub> = 50 pF R1 = 500 R2 = 500 T <sub>A</sub> = MIN t	<del>,</del> 2, 2,			UNIT
			SN54AL	S576B	SN74AL	S576B	SN74AL	S577A	
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			22		30		30		MHz
t <sub>PLH</sub>	OL IV	Any Q	4	24	3	14	4	14	
t <sub>PHL</sub>	CLK	Any Q	4	20	4	14	4	14	ns
<sup>t</sup> PZH	OE	Any Q	4	24	3	18	4	18	
t <sub>PZL</sub>	OE	Any Q	3	23	4	18	4	18	ns
<sup>t</sup> PHZ	ŌĒ	Any Q	2	14	1	10	2	10	ns
<sup>t</sup> PLZ	OE	Ally Q	3	29	2	15	3	15	115

<sup>§</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

## SN54ALS576B, SN54AS576 SN74ALS576B, SN74ALS577A, SN74AS576 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS065B - DECEMBER 1982 - REVISED JANUARY 1995

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub>	7 V
Voltage applied to a disabled 3-state output	
Operating free-air temperature range, T <sub>A</sub> : SN54AS576	-55°C to 125°C
SN74AS576	0°C to 70°C
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

			SI	N54AS57	'6	SN	174AS57	'6	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
loh	High-level output current				-12			-15	mA
l <sub>OL</sub>	Low-level output current				32			48	mA
fclock*	Clock frequency		0		100	0		125	MHz
	Podes donetes	CLK high	5			4			
t <sub>W</sub> *	Pulse duration	CLK low	4			2			ns
t <sub>su</sub> *	Setup time, data before CLK↑		3			2			ns
th*	Hold time, data after CLK↑		3			2			ns
TA	Operating free-air temperature		-55		125	0		70	°C

<sup>\*</sup> On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

#### SN54ALS576B, SN54AS576 SN74ALS576B, SN74ALS577A, SN74AS576 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS065B - DECEMBER 1982 - REVISED JANUARY 1995

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			SN	154AS57	6	SN	74AS57	6	
PARAMETER	TEST CON	NDITIONS	MIN	TYP†	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT
VIK	V <sub>CC</sub> = 4.5 V,	$I_{I} = -18 \text{ mA}$			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V <sub>CC</sub> -2	)		V <sub>CC</sub> -2			
VOH	V 45 V	$I_{OH} = -12 \text{ mA}$	2.4	3.2					V
	V <sub>CC</sub> = 4.5 V	$I_{OH} = -15 \text{ mA}$				2.4	3.3		
M	V 45V	I <sub>OL</sub> = 32 mA		0.29	0.5				V
VOL	V <sub>CC</sub> = 4.5 V	$I_{OL} = 48 \text{ mA}$					0.33	0.5	V
lozh	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.7 \text{ V}$			50			50	μΑ
lozL	V <sub>CC</sub> = 5.5 V,	$V_0 = 0.4 V$			-50			-50	μΑ
II	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V			0.1			0.1	mA
lн	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20			20	μΑ
, D	V 55V	V 0.4V			-3			-2	A
All others	$V_{CC} = 5.5 \text{ V},$	$V_{I} = 0.4 V$			-0.5			-0.5	mA
IO <sup>‡</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-30		-112	-30		-112	mA
		Outputs high		77	125		77	125	
ICC	V <sub>CC</sub> = 5.5 V	Outputs low		84	135		84	135	mA
		Outputs disabled		84	135		84	135	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

#### switching characteristics (see Figure 1)

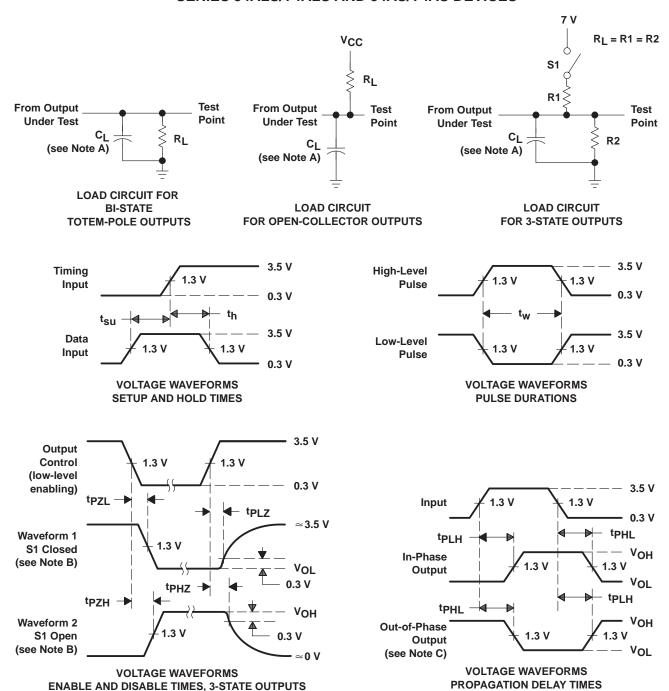
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>L</sub> R1 R2	CC = 4.5 = 50 pF = 500 Ω 2 = 500 Ω 1 = MIN to	<u>2,</u> <u>2,</u>	,	UNIT
			SN54A	S576	SN74A	S576	
			MIN	MAX	MIN	MAX	
fmax*			100		125		MHz
t <sub>PLH</sub>	CLK	Any Q	3	11	3	8	20
t <sub>PHL</sub>	CLK	Any Q	4	11	4	9	ns
<sup>t</sup> PZH	<del>OE</del>	A	2	7	2	6	20
<sup>t</sup> PZL	OE .	Any Q	3	11	3	10	ns
<sup>t</sup> PHZ	ŌĒ	Any Q	2	7	2	6	ns
t <sub>PLZ</sub>	OE .	Ally Q	2	7	2	6	115

<sup>\*</sup> On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

<sup>&</sup>lt;sup>‡</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

<sup>§</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

#### PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR  $\leq$  1 MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
84001022A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8400102RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
8400102SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
SN54ALS576BJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN74ALS576BDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS576BDWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS576BDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS576BDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS576BDWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS576BDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS576BN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS576BN3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	
SN74ALS576BNE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS576BNSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS576BNSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS576BNSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS577ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS577ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS577ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS577ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





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Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74ALS577ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS577ADWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS577ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS577ANT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	
SN74ALS577ANTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS576DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS576DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS576DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS576N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS576NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54ALS576BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS576BJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS576BW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
SNJ54AS576FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54AS576J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.





5-Sep-2011

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN54ALS576B, SN54AS576, SN74ALS576B, SN74AS576:

Catalog: SN74ALS576B, SN74AS576

Military: SN54ALS576B, SN54AS576

NOTE: Qualified Version Definitions:

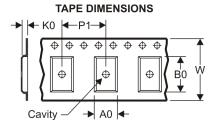
- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

#### PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All difficults are normal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS576BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS576BNSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74ALS577ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**PACKAGE MATERIALS INFORMATION** 

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\*All dimensions are nominal

7 III dilitoriorio di o Homina								
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74ALS576BDWR	SOIC	DW	20	2000	346.0	346.0	41.0	
SN74ALS576BNSR	SO	NS	20	2000	346.0	346.0	41.0	
SN74ALS577ADWR	SOIC	DW	24	2000	346.0	346.0	41.0	

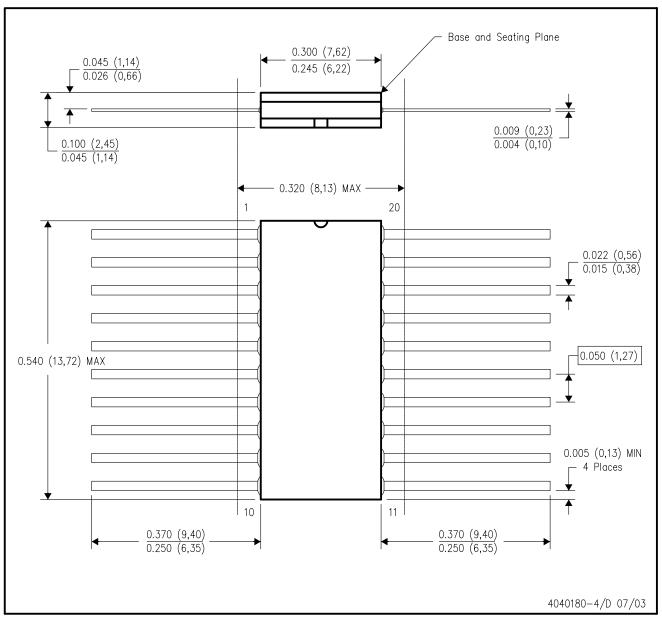
#### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## W (R-GDFP-F20)

### CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



## FK (S-CQCC-N\*\*)

#### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



## N (R-PDIP-T\*\*)

#### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



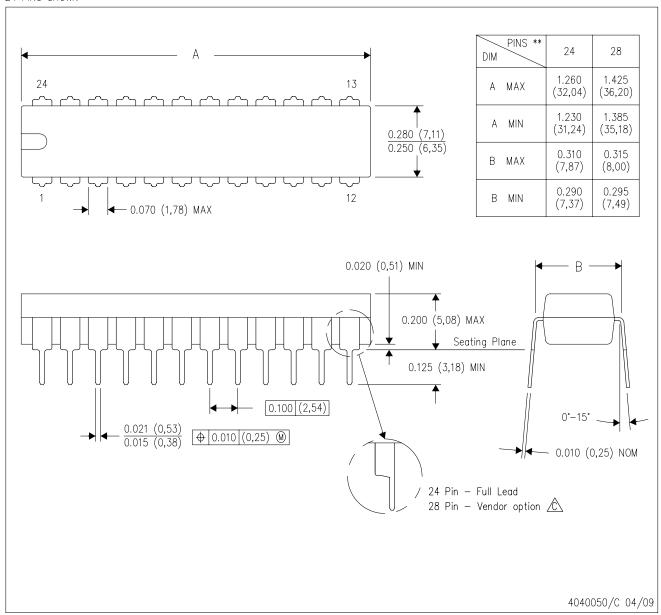
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



### NT (R-PDIP-T\*\*)

#### PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

The 28 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

#### PLASTIC SMALL OUTLINE



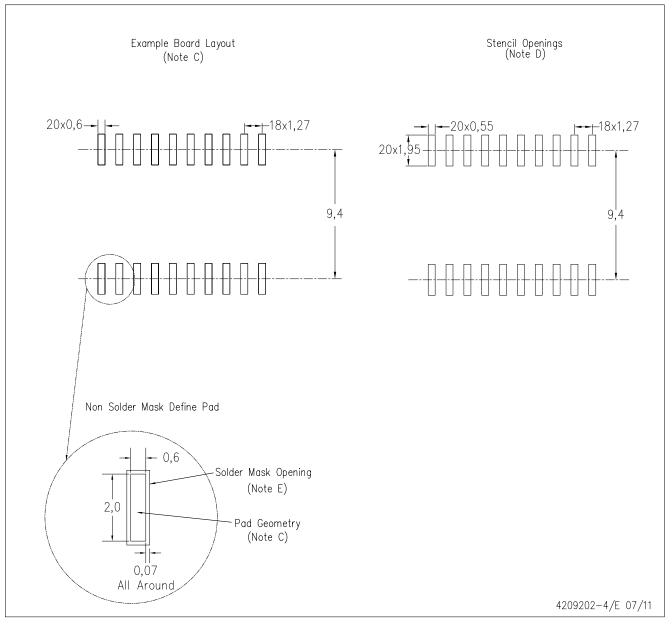
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DW (R-PDSO-G24)

#### PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



#### **MECHANICAL DATA**

#### NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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