# 32-Channel Serial to Parallel Converter With Open Drain Outputs

#### **Features**

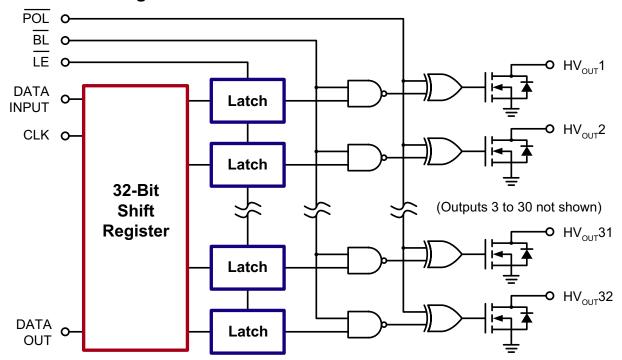
- Processed with HVCMOS® technology
- Sink current minimum 100mA
- Shift register speed 8.0MHz
- Polarity and Blanking inputs
- CMOS compatible inputs
- Forward and reverse shifting options
- Diode to VPP allows efficient power recovery

#### **General Description**

The HV5630 is a low-voltage serial to high-voltage parallel converter with open drain outputs. This device has been designed for use as a driver for AC-electroluminescent displays. It can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

This device consists of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the high to low transition of the clock. The HV5630 shifts in the clockwise direction when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the LE (latch enable), BL (blanking), or the POL (polarity) inputs. Transfer of data from the shift register to the latch occurs when the LE (latch enable) input is high. The data in the latch is stored when LE is low.

#### **Functional Block Diagram**



#### **Ordering Information**

<u>.                                     </u>								
	Package Option							
	44-Lead Quad							
Device	Plastic Chip Carrier							
	.653x.653in body							
	.180in height (max)							
	.050in pitch							
HV5630	HV5630PJ-G							
1173000	11700001 0-0							



#### Absolute Maximum Ratings

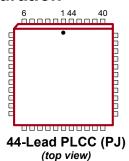
Parameter	Value
Supply voltage, V <sub>DD</sub> <sup>1</sup>	-0.5V to +15V
Output voltage, V <sub>PP</sub> <sup>1</sup>	-0.5V to +315V
Logic input levels <sup>1</sup>	-0.5V to V <sub>DD</sub> +0.5V
Ground current <sup>2</sup>	1.5A
Continuous total power dissipation <sup>3</sup>	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device

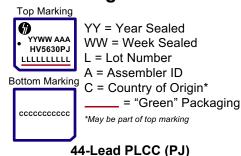
#### Notes:

- All voltages are referenced to  $\rm V_{ss}$  Duty cycle is limited by the total power dissipated in the package
- For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.

#### **Pin Configuration**



#### **Product Marking**



Package may or may not include the following marks: Si or \$\int\_{1}\$

#### **Recommended Operating Conditions**

Symbol	Parameter	Min	Max	Units	Conditions
V <sub>DD</sub>	Logic voltage supply	10.8	13.2	V	
HV <sub>out</sub>	High voltage output	-0.3	+300	V	
V <sub>IH</sub>	Input high voltage	V <sub>DD</sub> -2.0	$V_{_{\mathrm{DD}}}$	V	
V <sub>IL</sub>	Input low voltage	0	2.0	V	
f <sub>CLK</sub>	Clock frequency	-	8.0	MHz	
T <sub>A</sub>	Operating free-air temperature	-40	+85	°С	

#### **Power-Up Sequence**

Power-up sequence should be the following:

- 1. Connect ground
- 2. Apply  $V_{DD}$
- 3. Set all inputs to a known state

Power-down sequence should be the reverse of the above.

<sup>-</sup>G indicates package is RoHS compliant ('Green')

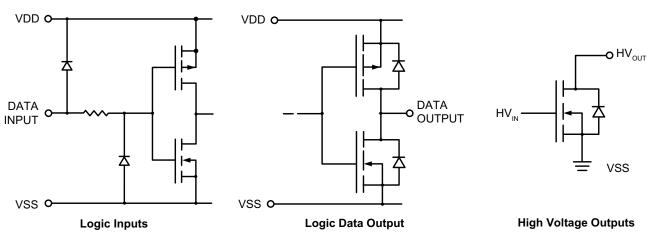
# **Electrical Characteristics** (over recommended operating conditions unless otherwise noted) **DC Characteristics**

Sym	Parameter		Min	Max	Units	Conditions
I <sub>DD</sub>	V <sub>DD</sub> supply current		-	15	mA	$f_{CLK} = 8.0MHz, F_{DATA} = 4.0MHz$
I <sub>DDQ</sub>	V <sub>DD</sub> supply current (quiesce	ent)	-	100	μA	V <sub>IN</sub> = 0V
I <sub>O(OFF)</sub>	Off state output current	-	10	μA	All outputs high, all SWS parallel	
I <sub>IH</sub>	High-level logic input curre	-	1.0	μA	$V_{IH} = V_{DD}$	
I <sub>IL</sub>	Low-level logic input curre	-	-1.0	μA	V <sub>IL</sub> = 0V	
V <sub>OH</sub>	High-level output data out		V <sub>DD</sub> -1.0V	-	V	I <sub>DOUT</sub> = -100μA
V		HV <sub>out</sub>	-	15	V	I <sub>HVOUT</sub> = +100mA
V <sub>OL</sub>	Low-level output voltage	DATA OUT	-	1.0	V	I <sub>DOUT</sub> = +100μA
V <sub>oc</sub>	HV <sub>out</sub> clamp voltage	-	-1.5	V	I <sub>OL</sub> = -100mA	

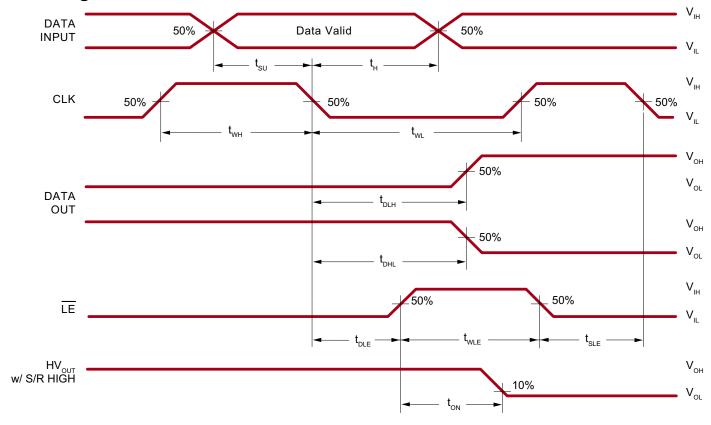
# AC Characteristics $(V_{DD} = 12V, T_c = 25^{\circ}C)$

Sym	Parameter	Min	Max	Units	Conditions
f <sub>CLK</sub>	Clock frequency	-	8.0	MHz	
t <sub>w</sub>	Clock width, high or low	62	-	ns	
t <sub>su</sub>	Data set-up time before CLK falls	25	-	ns	
t <sub>H</sub>	Data hold time after CLK falls	10	-	ns	
t <sub>on</sub>	Turn-on time, HV <sub>OUT</sub> from enable	-	500	ns	$R_L = 2.0K\Omega$ to $V_{PP}$ max.
t <sub>DHL</sub>	Delay time clock to data high to low	-	100	ns	C <sub>L</sub> = 15pF
t <sub>DLH</sub>	Delay time clock to data low to high	-	100	ns	C <sub>L</sub> = 15pF
t <sub>DLE</sub>	Delay time clock to $\overline{LE}$ low to high	50	-	ns	
t <sub>wle</sub>	Width of LE pulse	50	-	ns	
t <sub>SLE</sub>	LE setup time before clock falls	50	-	ns	

#### **Input and Output Equivalent Circuits**



## **Switching Waveforms**



#### **Functional Table**

			Inputs			Outputs					
Function	Data	CLK	LE	BL	POL	Shift	Shift Reg		HV Outputs		
	Data	OLK			FOL	1	232	1	232	*	
All on	Х	Х	Х	L	L	*	* *	On	OnOn	*	
All off	Х	Х	Х	L	Н	*	**	Off	OffOff	*	
Invert mode	Х	Х	L	Н	L	*	*	*	* *	*	
Load S/R	H or L	↓	L	Н	Н	H or L	**	*	*	*	
Load latches	Х	H or L	1	Н	Н	*	*	*	*	*	
Load latenes	Х	H or L	1	Н	L	*	**	*	* *	*	
Transparent latch mode	L	<b>↓</b>	Н	Н	Н	L	**	Off	**	*	
	Н	<b>↓</b>	Н	Н	Н	Н	**	On	* *	*	

#### Notes:

 $H = high\ level,\ L = low\ level,\ X = irrelevant,\ \downarrow = high-to-low\ transition,\ \uparrow = low-to-high\ transistion.$ 

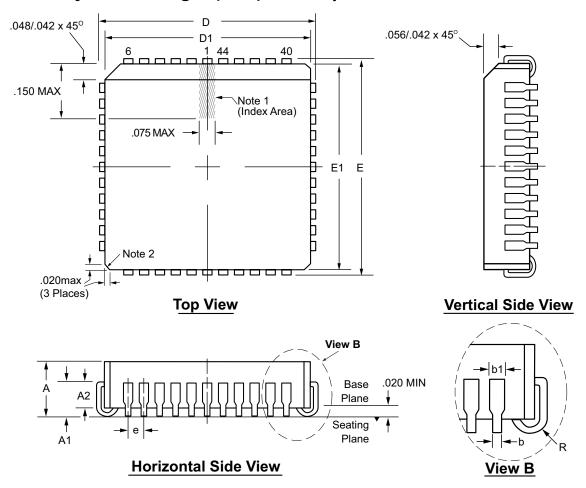
<sup>\*</sup> dependent on previous stage's state before the last CLK  $\downarrow$  or last  $\overline{LE}$  high.

# 44-Lead PLCC Pin Assignment (PJ)

Pin	Function	Description
1	HV <sub>оυт</sub> 17	
2	HV <sub>оит</sub> 16	
3	HV <sub>оит</sub> 15	
4	HV <sub>оит</sub> 14	
5	HV <sub>out</sub> 13	
6	HV <sub>out</sub> 12	
7	HV <sub>out</sub> 11	
8	HV <sub>out</sub> 10	
9	HV <sub>OUT</sub> 9	High voltage outputs.
10		Tight Voltage outputs.
11	HV <sub>OUT</sub> 8	
12	HV <sub>OUT</sub> 7	
13	HV <sub>OUT</sub> 6	
	HV <sub>OUT</sub> 5	
14	HV <sub>OUT</sub> 4	
15	HV <sub>OUT</sub> 3	
16	HV <sub>OUT</sub> 2	
17	HV <sub>OUT</sub> 1	Different states
18	DATA OUT	Data output pin.
19	N/C	<b>-</b>
20	N/C	No internal connection.
21	N/C	
22	POL	Inverts the polarity of the HV <sub>OUT</sub> pins
23	CLK	Clock pin, shift registers shift data on falling edge of input clock.
24	VSS	Reference voltage, usually ground.
25	VDD	Logic supply voltage.
26	ĪĒ	Latch enable pin, data is shifted from shift register to latches on logic input high.
27	DATA IN	Data input pin.
28	BL	Blanking pin sets all HV <sub>OUT</sub> pins low or high depending upon state of polarity. See function table.
29	N/C	No internal connection.
30	HV <sub>OUT</sub> 32	
31	HV <sub>out</sub> 31	
32	HV <sub>out</sub> 30	
33	HV <sub>out</sub> 29	
34	HV <sub>out</sub> 28	
35	HV <sub>out</sub> 27	
36	HV <sub>out</sub> 26	
37	HV <sub>out</sub> 25	High voltage outputs.
38	HV <sub>out</sub> 24	
39	HV <sub>out</sub> 23	
40	HV <sub>out</sub> 22	
41	HV <sub>OUT</sub> 21	
42	HV <sub>оит</sub> 20	
43	HV <sub>оит</sub> 19	
44	HV <sub>OUT</sub> 18	

## 44-Lead PLCC Package Outline (PJ)

.653x.653in body, .180in height (max), .050in pitch



#### Notes:

- A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
- 2. Actual shape of this feature may vary.

Symb	ol	Α	A1	A2	b	b1	D	D1	E	E1	е	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650		.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653	.050 BSC	.035
	MAX	.180	.120	.083	.021	.036 <sup>†</sup>	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-44PLCCPJ, Version F031111.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <a href="http://www.supertex.com/packaging.html">http://www.supertex.com/packaging.html</a>.)

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