SCHS105C - Revised October 2003

# CD40175B Types

# CMOS Quad 'D'-Type Flip-Flop

## High-Voltage Types (20-Volt Rating)

#### **Features**

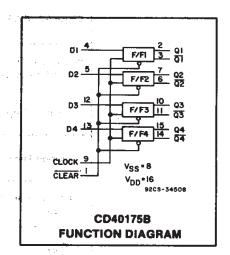
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full packagetemperature range; 100 nA at 18 V and 25° C
- Noise margin (full packagetemperature range) =
  - 1 V at VDD = 5 V 2 V at VDD = 10 V 2.5 V at VDD = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

SAME BUILDING

- Output compatible with two HTL loads, two low power TTL loads, or one low power Schottky TTL load
- Functional equivalent to TTL 74175
- Standardized symmetrical output characteristics

#### **Applications:**

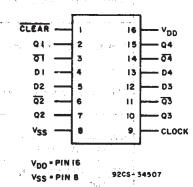
- Shift registers
- Buffer/storage registers
- Pattern generators



CD40175B consists of four identical D-type flipflops. Each flip-flop has an independent DATA D input and complementary Q and Q outputs. The CLOCK and CLEAR inputs are common to all flip-flops. Data are transferred to the Q outputs on the positive-going transition of the clock pulse. All four flip-flops are simultaneously reset by a low level on the CLEAR input.

These devices can function as shift register elements or as T-type flip-flops for toggle and counter applications.

The CD40175B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).



**TERMINAL ASSIGNMENT** 

MAXIMUM RATINGS, Absolute-Maximum Values:	- '	28 ± 1	the second second	
DC SUPPLY-VOLTAGE RANGE, (VDD)	MG -	**		
MAXIMUM RATINGS, Absolute-Maximum Values: DC SUPPLY-VOLTAGE RANGE, (VDD) Voltages referenced to VSS Terminal)		********		0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS				0.5V to VDD +0.5V
DC INPUT CURRENT, ANY ONE INPUT				
POWER DISSIPATION PER PACKAGE (PD):				
For $T_A = -55^{\circ}C$ to $+100^{\circ}C$				500mW
For T <sub>A</sub> = +100°C to +125°C		* * * * * * * * * * * * * * * * * * * *	Derate Linearity at	12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	3.44.1	in the gar		**
FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package)	kage-Types)	: 		100mW
OPERATING-TEMPERATURE RANGE (TA)		*****	27	55°C to +125°C
STORAGE TEMPERATURE RANGE (Tstg)				
At distance $1/16 \pm 1/32$ inch $(1.59 \pm 0.79$ mm) from case for 1	0s max			+265°C

## RECOMMENDED OPERATING CONDITIONS at TA = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

QUADACTED:	14	LIN			
CHARACTERISTIC	Vod (V)	MIN.	MAX.	UNITS	
Supply-Voltage Range (For TA = Full Package-Tempe	erature Range)		3	18	· v
		5	120		
Data Setup Time	tsu	10	50	_	ns
	e e e e	15	40	_	
	,	5	80		
Data Hold Time	tH	10	40	_	ns
		15	30	_	
		- 5	_	2	1.5
Clock Input Frequency	fCL	10	dc	5	MHz
<u> </u>		15	_	6.5	
		5	-	15	
Clock Input Rise or Fall Time	troL, troL	10	· —	15	μs
		15	<u> </u>	15	
		5	250		
Clock Input Pulse Width	tw., twn	10	100	–	ns
		15	75	_	
		5	200	-	
Clear Pulse Width	tWL	10	80	_	ns
		15	60	_	
		5	250	_	
Clear Removal Time	trem	10	100	_	ns
		15	80	_	

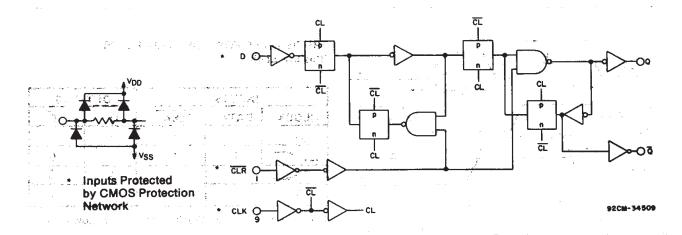


Fig. 1 - Logic diagram (1 of 4 flip-flops).

### STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC CON		NDITIO	NS	LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
		V <sub>0</sub>	3.5							+25		
		(V)	VIN (V)	VDD (V)	-55	-40	+85	+125	Min.	Тур.	Max.	
Quiescent			0, 5	5	1	1	30	30		0.02	1	
Device		_	0, 10	10	2	2	60	60	_	0.02	2	1.
Current		_	0, 15	15	4	4	120	120	_	0.02	4	μΑ
Max.	DD	_	0, 20	20	20	20	600	600	_	0.04	20	1
Output Low		0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	_	
(Sink) Current		0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	_	
Min.	IOL	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	_	1
Output High		4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1		mA
(Source)		2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	<u> </u>	1
Current		9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	_	1
Min.	Юн	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	_	1
Output Voltage:		-	0, 5	5		0.	05			0	0.05	
Low-Level		_	0, 10	10		0.	05			0	0.05	1
Max.	VOL	-,	0, 15	15		0.	05		_	0	0.05	1
Output Voltage:		_	0, 5	5		4.	95		4.95	5	_	v
High-Level		_	0, 10	10		9.	95		9.95	10	-	1
Min.	Vон		0, 15	15		14	.95	· · · · ·	14.95	15	_	1
Input Low		0.5,4.5	_	5		1	.5		_	_	1.5	
Voltage		1, 9	_	10	3			_	l –	3	1	
Max.	VIL	1.5,13.5	_	15	4			-	1 -	4	1	
Input High		0.5,4.5		5	3.5			3.5	_	_	V	
Voltage		1, 9	<u> </u>	10			7		7	_		
Min.	Vін	1.5,13.5	. —	15	1,1			11.	_	. —	1	
Input Current Max	c. lin	_	0, 18	18	±0.1	±0.1	±1	±1	_	±10-5	±0.1	μΑ

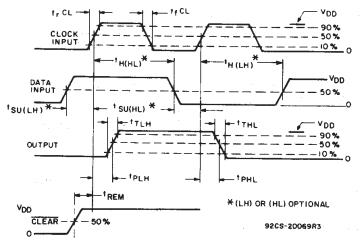


Fig. 2 - Definition of setup, hold, propagation delay, and removal times.

# TRUTH TABLE FOR 1 OF 4 FLIP-FLOPS (Positive Logic)

	INPUTS	OUT	PUTS	
CLOCK	DATA	CLEAR	Q	ā
\	0	1	0	1
\	1	1	1	0
	Х	1,,	Q	ব
X	×	0 10 12	0	1

1=High Level X=Don't Care 0=Low Level

### DYNAMIC ELECTRICAL CHARACTERISTICS at TA = 25°C; input tr, tr = 20 ns, CL = 50 pF, RL = 200 k $\Omega$

CHARACTERISTIC	TEST CONDITIONS VDD (V)			TYP. MAX.	
	5	_	100	200	
Transition Time tTHL, tTLH	10	_	50	100	
	15	_	40	80	
Propagation Delay Time	5	<u></u>	220	400	7
Clock to Q Output tPHL, tPLH	10	<u> </u>	90	160	
,	15	_	70	120	
Propagation Delay Time	5	_	325	500	7
CLEAR to Q Output tPHL	10		130	200	ns
	15		100	150	
Minimum Pulse Width	5		110	250	
Clock twh	10	_	45	100	
	15	_	35	75	
	5		100	200	1
Clear	10		40	80	1
	15	_	30	60	
	5	2	4.5		1
Maximum Clock Frequency fcL	10	5	11	l _	MH
	15	6.5	14	_	'''' "
	5	15			+
Maximum Clock Rise or Fall Time trCL, trCL	10	15	_		μs
waxiiidiii Olook 1130 Ol 1 kii 111110	15	15		_	"
	5		60	120	+
Minimum Data Setup Time tsu	10	_	25	50	1
minimum data detap rinie (od	15		20	40	
	5		40	80	-
Minimum Data Hold Time tH	10	_	20	40	ns
minimum pata noto nine (n	15	_	15	30	113
	5		125	250	┨
Minimum Clear Removal Time ‡ tREM	10		50	100	
Millian Creat Lethoval Line + (KEW	15		40	i	-
	15	<del></del>	40	80	+
Input Capacitance CIN	_		5	7.5	pF

### ‡ CLEAR signal must be high prior to positive-going transition of CLOCK pulse.

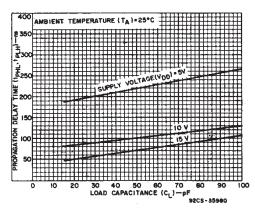


Fig. 3 - Typical propagation delay time (CLOCK to OUTPUT) as a function of load capacitance.

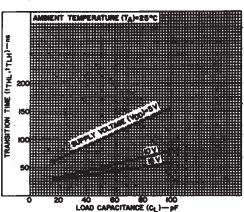


Fig. 4 - Typical transition time as a function of load capacitance.

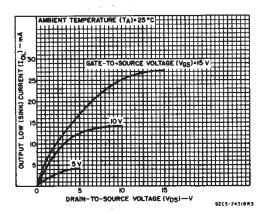


Fig. 5 – Typical output low (sink) current characteristics.

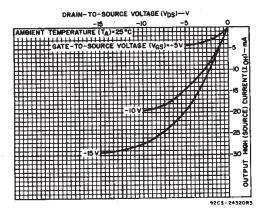


Fig. 7 – Typical output high (source) current characteristics.

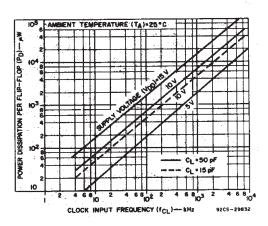


Fig. 9 – Typical dynamic power dissipation as a function of CLOCK frequency.

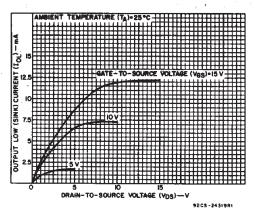


Fig. 6 - Minimum output low (sink) current characteristics.

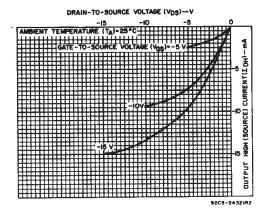


Fig. 8 - Minimum output high (source) current characteristics.

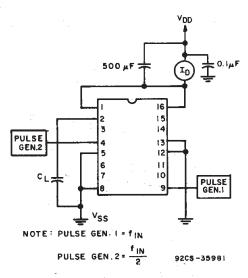
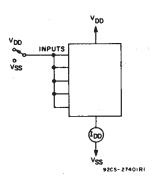


Fig. 10 - Dynamic power dissipation test circuit.



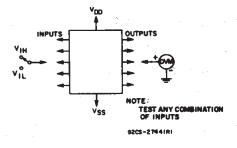


Fig. 11 - Quiescent device current test circuit.

Fig. 12 - Noise immunity test circuit.

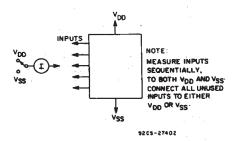
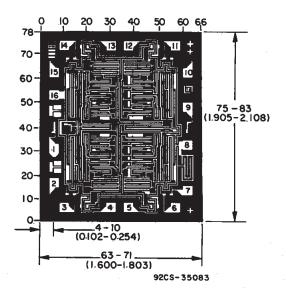


Fig. 13 - Input leakage current test circuit.



Dimensions and pad layout for CD40175BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10<sup>-3</sup> inch).

### PACKAGE OPTION ADDENDUM

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### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD40175BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD40175BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD40175BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD40175BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BMTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BW	OBSOLETE	WAFER SALE	YS	0		TBD	Call TI	Call TI

<sup>&</sup>lt;sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



### PACKAGE OPTION ADDENDUM

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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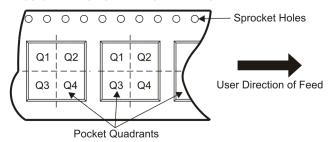
## TAPE AND REEL INFORMATION





Α	0	Dimension designed to accommodate the component width
В	0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
٧	٧	Overall width of the carrier tape
ГР	1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All differsions are normal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40175BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD40175BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD40175BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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\*All dimensions are nominal

7 III GITTIOTOTOTO GITO TIOTTIITIGI							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40175BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD40175BNSR	SO	NS	16	2000	346.0	346.0	33.0
CD40175BPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

## 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



## D (R-PDS0-G16)

## PLASTIC SMALL OUTLINE

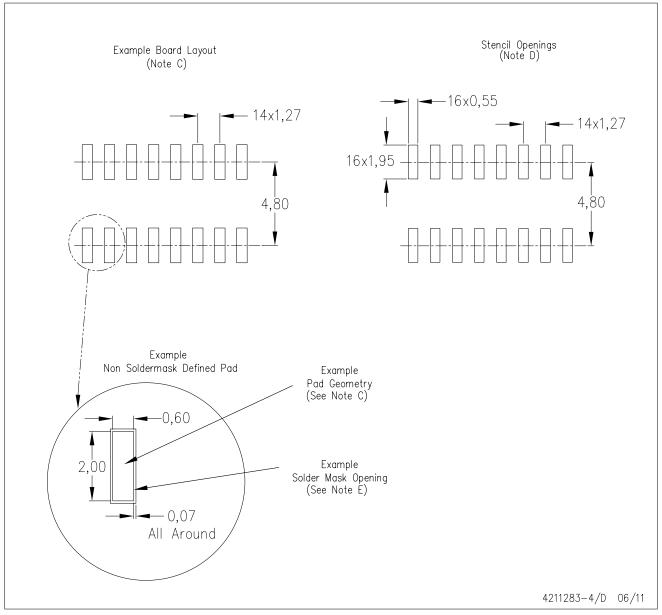


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



## D (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

## PLASTIC SMALL OUTLINE

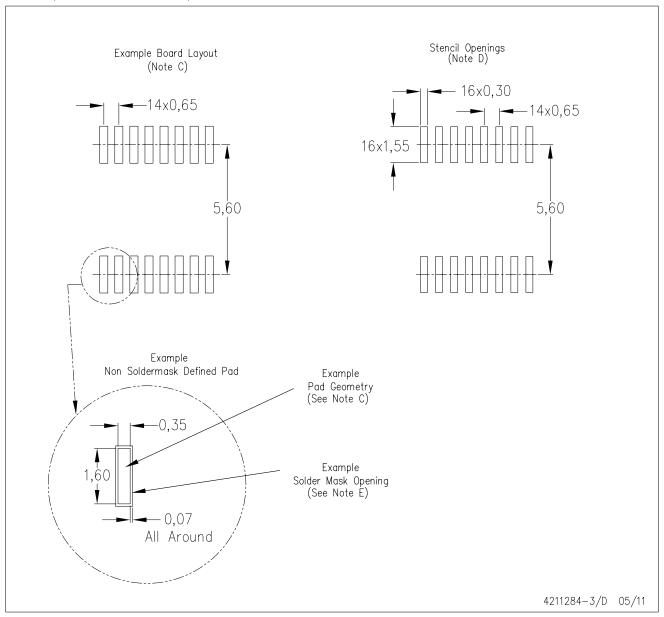


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



## PW (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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