

100MHz, 80-Channel Serial to Parallel Converter with Push-Pull Outputs

Features

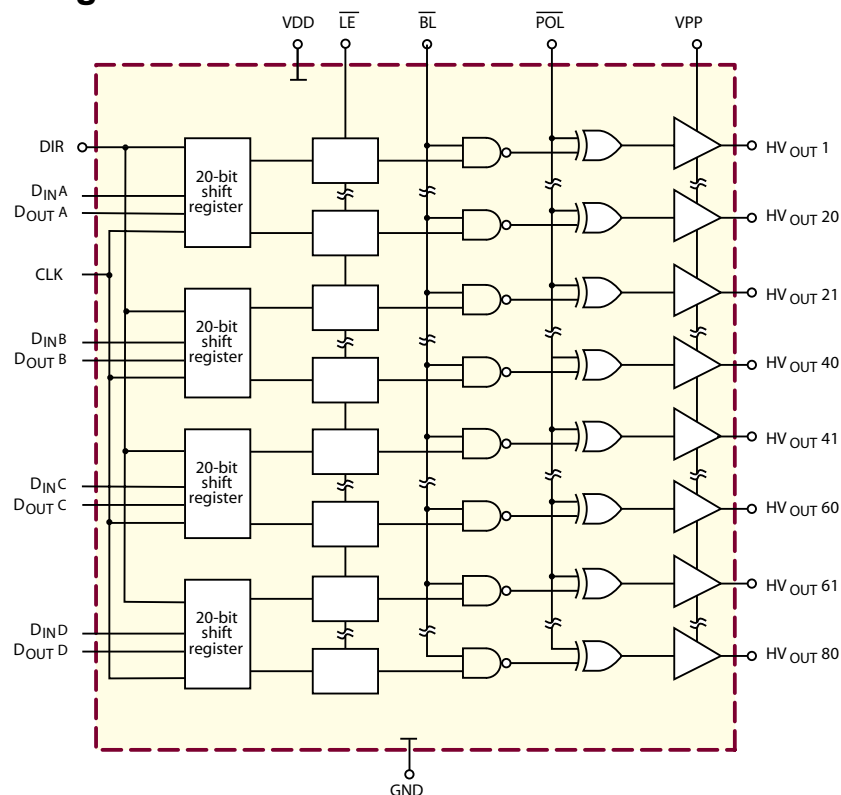
- ▶ HVCMOS® technology
- ▶ 5.0V CMS Logic
- ▶ Output voltage up to 80V
- ▶ Low power level shifting
- ▶ 100MHz equivalent data rate using four dynamic shift registers
- ▶ Latched data outputs
- ▶ Forward and reverse shifting options (DIR pin)
- ▶ Diode to VPP allows efficient power recovery
- ▶ Outputs may be hot switched
- ▶ Hi-Rel processing available

General Description

The HV574 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for printer applications. It can also be used in any application requiring multiple output high-voltage current sourcing and sinking capability such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays.

The device has 4 parallel 20-bit dynamic shift registers, permitting data rates 4X the speed of one (they are clocked together). There are 80 static latches and control logic to perform the polarity select and blanking of the outputs. HV_{OUT} 1 is connected to the first stage of the first shift register through the polarity and blanking logic. Data is shifted through the shift registers on the logic low to high transition of the clock. The DIR pin causes CCW shifting when connected to GND, and CW shifting when connected to VDD. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HV_{OUT} 80). Operation of the shift register is not affected by the \overline{LE} (latch enable), \overline{BL} (blanking), or the \overline{POL} (polarity) inputs. Transfer of data from the shift registers to the latches occurs when the \overline{LE} (latch enable) input is high. The data in the latches is stored when \overline{LE} is low.

Functional Block Diagram



Ordering Information

| Device | Package Options |
|--------|---|
| | 100-Lead PQFP 20.00x14.00mm body 3.40mm height (max) 0.65mm pitch |
| HV574 | HV574PG-G |



-G indicates package is RoHS compliant ("Green")

Absolute Maximum Ratings

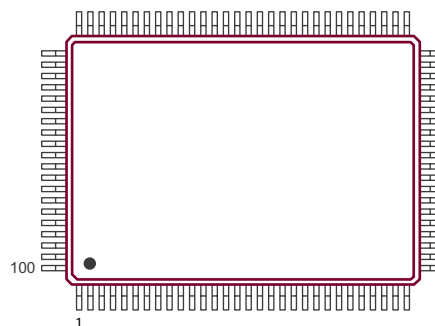
| Parameter | Value |
|---|--------------------------|
| Supply voltage, V_{DD} | -0.5V to +7.5V |
| Output voltage, V_{PP} | -0.5V to +90V |
| Logic input levels | -0.3V to $V_{DD} + 0.3V$ |
| Ground current ¹ | 1.5A |
| Continuous total power dissipation ² | 1200mW |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -65°C to +150°C |
| Lead temperature ³ | 260°C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

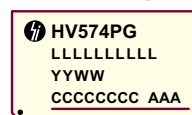
- Limited by the total dissipated in the package.
- For operation above 25°C ambient derate linearly to 85°C at 20mW/°C.
- 1.6mm from case for 10 seconds.

Pin Configuration



100-Lead PQFP (PG)
(top view)

Product Marking



L = Lot Number
 YY = Year Sealed
 WW = Week Sealed
 C = Country of Origin
 A = Assembler ID
 * = "Green" Packaging

100-Lead PQFP (PG)

Recommended Operating Conditions

| Sym | Parameter | Min | Max | Units |
|-----------|--------------------------------|-----------------|-----|-------|
| V_{DD} | Logic supply voltage | 4.5 | 5.5 | V |
| V_{PP} | Output voltage | 12 | 80 | V |
| V_{IH} | High-level input voltage | $V_{DD} - 0.5V$ | - | V |
| V_{IL} | Low-level input voltage | 0 | 0.5 | V |
| f_{CLK} | Clock frequency per register | 0.001 | 25 | MHz |
| T_A | Operating free-air temperature | -40 | +85 | °C |

Notes:

Power-up sequence should be the following:

- Apply ground
- Apply V_{DD}
- Set all inputs (Data, CLK, Enable etc.) to a known state
- Apply V_{PP}

The V_{PP} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.

DC Electrical Characteristics (Over recommended operating conditions unless otherwise noted)

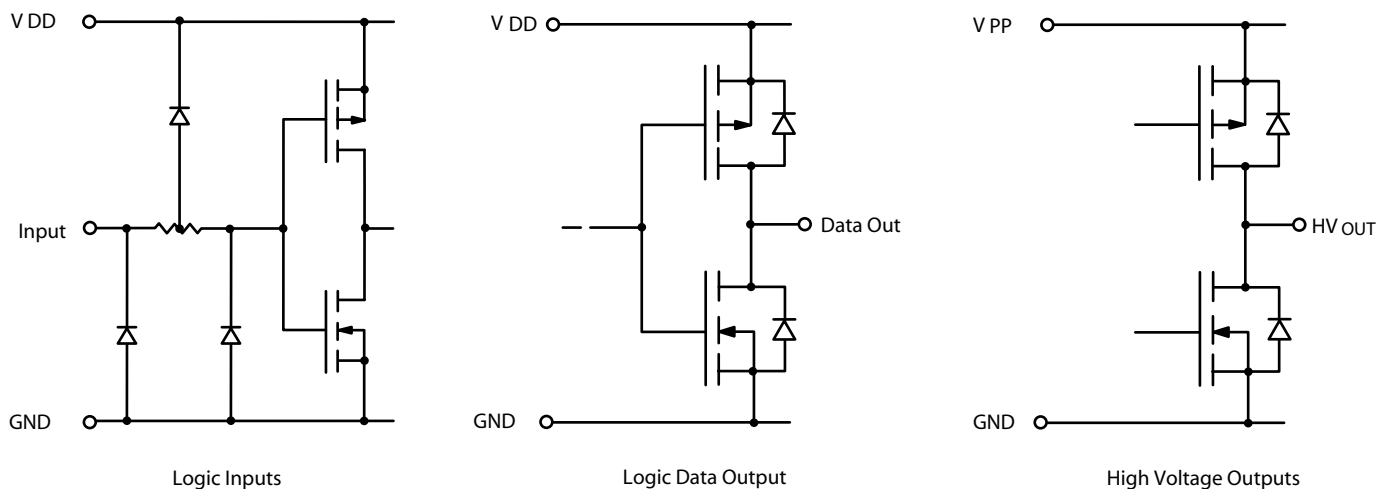
| Sym | Parameter | Min | Max | Units | Conditions | |
|-----------|-----------------------------------|-------------------|----------------|---------------|---|--|
| I_{DD} | V_{DD} supply current | - | 30 | mA | $V_{DD} = V_{DD\ max}$, $f_{CLK} = 25\text{MHz}$ | |
| I_{PP} | Quiescent V_{PP} supply current | - | 100 | μA | Outputs high | |
| | | - | 100 | μA | Outputs low | |
| I_{DDQ} | Quiescent V_{DD} supply current | - | 100 | μA | All $V_{IN} = V_{DD}$ | |
| V_{OH} | High-level output | HV _{OUT} | $V_{PP} - 9.0$ | - | V | $I_O = -30\text{mA}$, $V_{PP} = +80\text{V}$ |
| | | Data out | $V_{DD} - 0.5$ | - | V | $I_O = -100\mu\text{A}$ |
| V_{OL} | Low-level output | HV _{OUT} | - | 3.75 | V | $I_O = +15\text{mA}$, $V_{DD} = +5.0\text{V}$ |
| | | Data out | - | 0.5 | V | $I_O = +100\mu\text{A}$ |
| I_{IH} | High-level logic input current | - | 1.0 | μA | $V_{IH} = V_{DD}$ | |
| I_{IL} | Low-level logic input current | - | -1.0 | μA | $V_{IL} = 0\text{V}$ | |

AC Electrical Characteristics ($T_A = 85^\circ\text{C max}$. Logic signal inputs and data inputs have $t_r, t_f \leq 5.0\text{ns}$ [10% and 90% points])

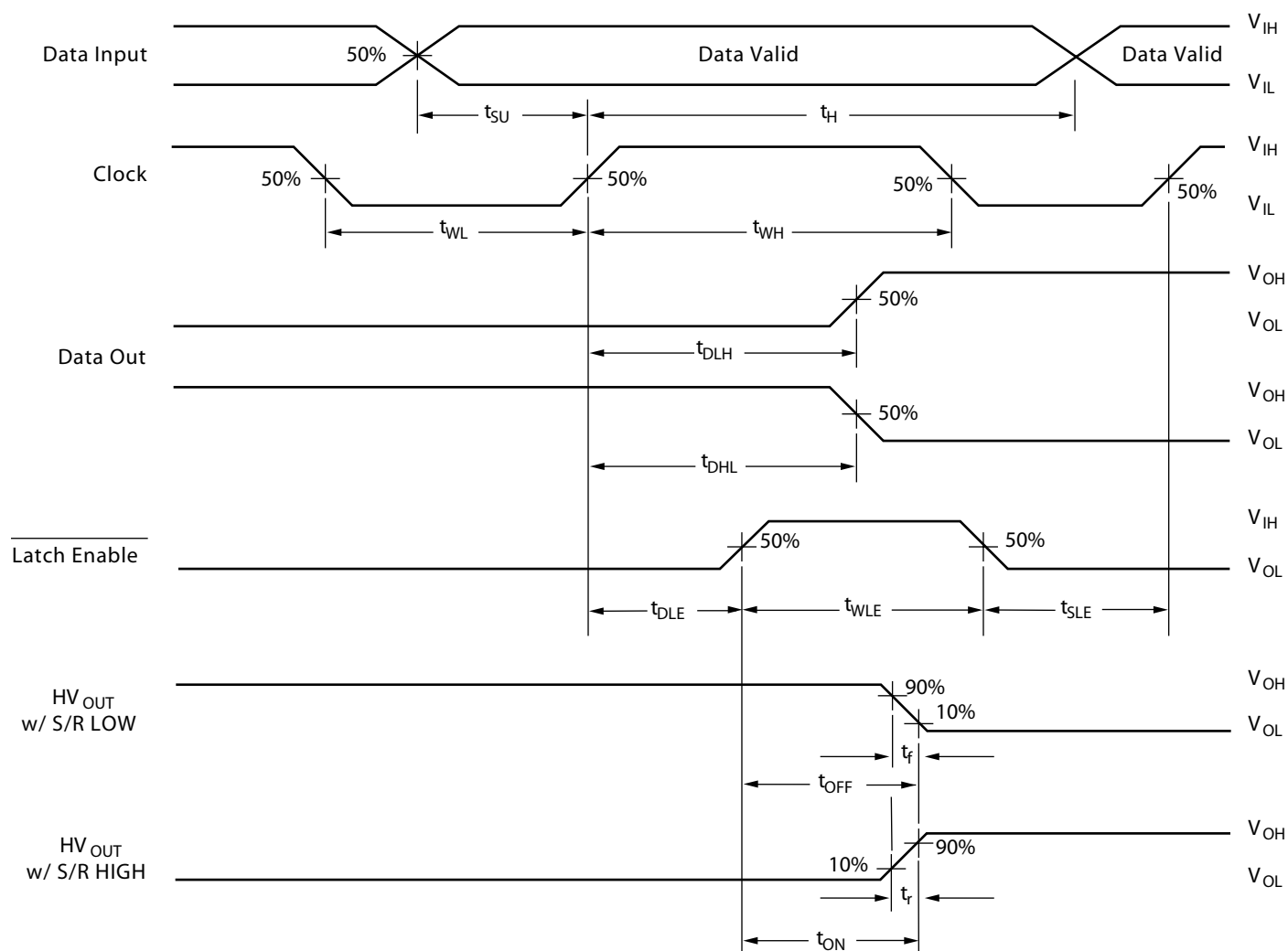
| Sym | Parameter | Min | Max | Units | Conditions |
|-------------------|--|-------|-----|---------------|---|
| f_{CLK} | Clock frequency | 0.001 | 25 | MHz | $V_{DD} = 4.5\text{V}$, $T_J = 25^\circ\text{C}$ |
| | | 0.001 | 20 | | $V_{DD} = 4.5\text{V}$, $T_J = 125^\circ\text{C}$ |
| t_{WL}, t_{WH} | Clock width high or low | 20 | - | ns | --- |
| t_{SU} | Data set-up time before clock rises | 0 | - | ns | --- |
| t_H | Data hold time after clock rises | 15 | - | ns | --- |
| t_{ON}, t_{OFF} | Time from latch enable to HV _{OUT} | - | 500 | ns | $C_L = 15\text{pF}$ |
| t_{DHL} | Delay time clock to data high to low | - | 38 | ns | $C_L = 15\text{pF}$, $V_{DD} = 5.0\text{V}$ |
| t_{DLH} | Delay time clock to data low to high | - | 38 | ns | $C_L = 15\text{pF}$, $V_{DD} = 5.0\text{V}$ |
| t_{DLE}^* | Delay time clock to $\overline{\text{LE}}$ low to high | 25 | - | ns | --- |
| t_{WLE} | $\overline{\text{LE}}$ pulse width | 25 | - | ns | --- |
| t_{SLE} | $\overline{\text{LE}}$ set-up time before clock rises | 0 | - | ns | --- |
| t_r, t_f | Output rise/fall time | - | 1.0 | μs | $C_L = 600\text{pF}$, HV _{OUT} from 0 - 60V |

* t_{DLE} is not required but is recommended to produce stable HV outputs and thus minimize power dissipation and current spikes (allows internal SR output to stabilize).

Input and Output Equivalent Circuits



Switching Waveforms



Function Table

| Function | Inputs | | | | | | Outputs | | |
|--|------------|-----|-----------------|-----------------|------------------|-----|---------------------------|--------------------------|------------|
| | Data | CLK | \overline{LE} | \overline{BL} | \overline{POL} | DIR | Shift Reg | HV Outputs | Data Out |
| All O/P high | X | X | X | L | L | X | - | H | - |
| All O/P low | X | X | X | L | H | X | - | L | - |
| O/P normal | X | X | X | H | H | X | - | No inversion | - |
| O/P inverted | X | X | X | H | L | X | - | Inversion | - |
| Data falls through (latches transparent) | L | ↑ | H | H | H | X | L | L | - |
| | H | ↑ | H | H | H | X | H | H | - |
| | L | ↑ | H | H | L | X | L | H | - |
| | H | ↑ | H | H | L | X | H | L | - |
| Data stored/ latches loaded | X | X | L | H | H | X | * | Stored Data | - |
| | X | X | L | H | L | X | * | Inversion of stored data | - |
| I/O relation | $D_{IN}X$ | ↑ | H | H | H | H | $Q_n \rightarrow Q_{n+1}$ | New H or L | $D_{OUT}X$ |
| | $D_{IN}X$ | ↑ | L | H | H | H | $Q_n \rightarrow Q_{n+1}$ | Previous H or L | $D_{OUT}X$ |
| | $D_{OUT}X$ | ↑ | L | H | H | L | $Q_n \rightarrow Q_{n-1}$ | Previous H or L | $D_{IN}X$ |
| | $D_{OUT}X$ | ↑ | H | H | H | L | $Q_n \rightarrow Q_{n-1}$ | New H or L | $D_{IN}X$ |

Note:

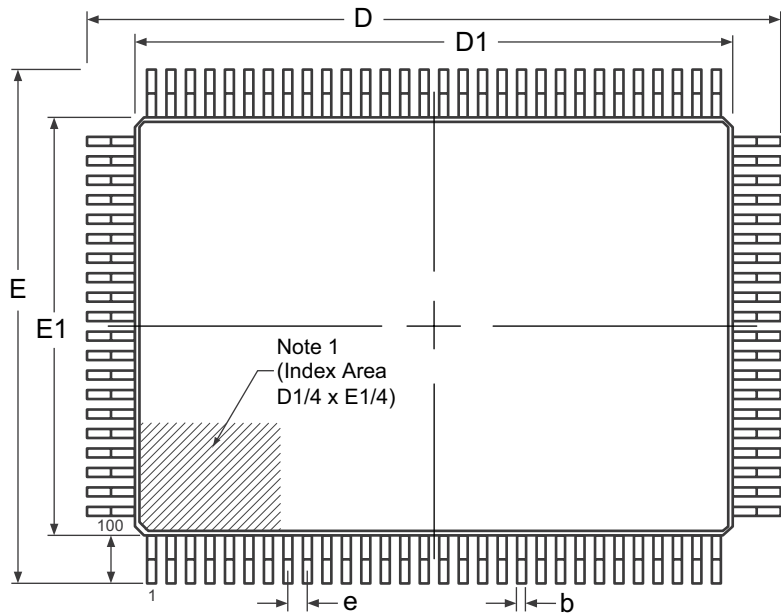
* = dependent on previous stage's state. See Pin configuration for DIN and DOUT pin designation for CW and CCW shift.

Pin Function

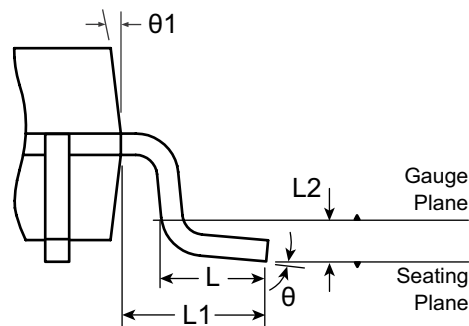
| Pin # | Function | Pin # | Function | Pin # | Function | Pin # | Function |
|-------|----------------------|-------|-------------------------|-------|----------------------|-------|----------------------|
| 1 | HV _{OUT} 30 | 26 | HV _{OUT} 5 | 51 | HV _{OUT} 80 | 76 | HV _{OUT} 55 |
| 2 | HV _{OUT} 29 | 27 | HV _{OUT} 4 | 52 | HV _{OUT} 79 | 77 | HV _{OUT} 54 |
| 3 | HV _{OUT} 28 | 28 | HV _{OUT} 3 | 53 | HV _{OUT} 78 | 78 | HV _{OUT} 53 |
| 4 | HV _{OUT} 27 | 29 | HV _{OUT} 2 | 54 | HV _{OUT} 77 | 79 | HV _{OUT} 52 |
| 5 | HV _{OUT} 26 | 30 | HV _{OUT} 1 | 55 | HV _{OUT} 76 | 80 | HV _{OUT} 51 |
| 6 | HV _{OUT} 25 | 31 | NC | 56 | HV _{OUT} 75 | 81 | HV _{OUT} 50 |
| 7 | HV _{OUT} 24 | 32 | VPP | 57 | HV _{OUT} 74 | 82 | HV _{OUT} 49 |
| 8 | HV _{OUT} 23 | 33 | HVGND | 58 | HV _{OUT} 73 | 83 | HV _{OUT} 48 |
| 9 | HV _{OUT} 22 | 34 | D _{IN} A | 59 | HV _{OUT} 72 | 84 | HV _{OUT} 47 |
| 10 | HV _{OUT} 21 | 35 | D _{IN} B | 60 | HV _{OUT} 71 | 85 | HV _{OUT} 46 |
| 11 | HV _{OUT} 20 | 36 | D _{IN} C | 61 | HV _{OUT} 70 | 86 | HV _{OUT} 45 |
| 12 | HV _{OUT} 19 | 37 | D _{IN} D | 62 | HV _{OUT} 69 | 87 | HV _{OUT} 44 |
| 13 | HV _{OUT} 18 | 38 | VDD | 63 | HV _{OUT} 68 | 88 | HV _{OUT} 43 |
| 14 | HV _{OUT} 17 | 39 | $\overline{\text{POL}}$ | 64 | HV _{OUT} 67 | 89 | HV _{OUT} 42 |
| 15 | HV _{OUT} 16 | 40 | $\overline{\text{LE}}$ | 65 | HV _{OUT} 66 | 90 | HV _{OUT} 41 |
| 16 | HV _{OUT} 15 | 41 | CLK | 66 | HV _{OUT} 65 | 91 | HV _{OUT} 40 |
| 17 | HV _{OUT} 14 | 42 | DIR | 67 | HV _{OUT} 64 | 92 | HV _{OUT} 39 |
| 18 | HV _{OUT} 13 | 43 | $\overline{\text{BL}}$ | 68 | HV _{OUT} 63 | 93 | HV _{OUT} 38 |
| 19 | HV _{OUT} 12 | 44 | GND | 69 | HV _{OUT} 62 | 94 | HV _{OUT} 37 |
| 20 | HV _{OUT} 11 | 45 | D _{OUT} D | 70 | HV _{OUT} 61 | 95 | HV _{OUT} 36 |
| 21 | HV _{OUT} 10 | 46 | D _{OUT} C | 71 | HV _{OUT} 60 | 96 | HV _{OUT} 35 |
| 22 | HV _{OUT} 9 | 47 | D _{OUT} B | 72 | HV _{OUT} 59 | 97 | HV _{OUT} 34 |
| 23 | HV _{OUT} 8 | 48 | D _{OUT} A | 73 | HV _{OUT} 58 | 98 | HV _{OUT} 33 |
| 24 | HV _{OUT} 7 | 49 | HVGND | 74 | HV _{OUT} 57 | 99 | HV _{OUT} 32 |
| 25 | HV _{OUT} 6 | 50 | VPP | 75 | HV _{OUT} 56 | 100 | HV _{OUT} 31 |

100-Lead PQFP Package Outline (PG)

20.00x14.00mm body, 3.40mm height (max), 0.65mm pitch, 3.90mm footprint



Top View



View B



Side View

Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 Identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | A | A1 | A2 | b | D | D1 | E | E1 | e | L | L1 | L2 | θ | θ1 | |
|----------------|-----|-------|-------|------|------|--------|--------|--------|--------|----------|------|----------|----------|------|-----|
| Dimension (mm) | MIN | 2.80* | 0.25 | 2.55 | 0.22 | 23.65* | 19.80* | 17.65* | 13.80* | 0.65 BSC | 0.73 | 1.95 REF | 0.25 BSC | 0 | 5° |
| | NOM | - | - | 2.80 | - | 23.90 | 20.00 | 17.90 | 14.00 | | 0.88 | | | 3.5° | - |
| | MAX | 3.40 | 0.50* | 3.05 | 0.38 | 24.15* | 20.20* | 18.15* | 14.20* | | 1.03 | | | 7° | 16° |

JEDEC Registration MO-112, Variation CC-1, Issue B, Sept. 1995.

* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

Drawings not to scale.

Supertex Doc. #: DSPD-100PQFP, Version A090608.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." Supertex inc. does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the Supertex inc. website: <http://www.supertex.com>.