32-Channel Serial to Parallel Converter With Open Drain Outputs

Features

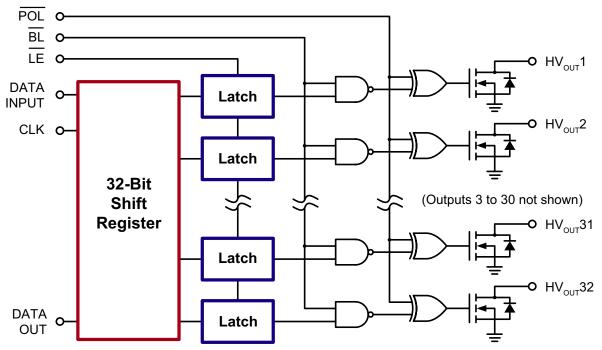
- Processed with HVCMOS® technology
- Sink current minimum 100mA
- Shift register speed 8.0MHz
- Polarity and Blanking inputs
- CMOS compatible inputs
- ► Forward and reverse shifting options
- ▶ Diode to VPP allows efficient power recovery

General Description

The HV5622 is a low-voltage serial to high-voltage parallel converter with open drain outputs. This device has been designed for use as a driver for AC-electroluminescent displays. It can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

This device consists of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the high to low transition of the clock. The HV5622 shifts in the clockwise direction when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the LE (latch enable), BL (blanking), or the POL (polarity) inputs. Transfer of data from the shift register to the latch occurs when the LE (latch enable) input is high. The data in the latch is stored when LE is low.

Functional Block Diagram



Ordering Information

	Package Options							
Device	44-Lead Quad Plastic Gullwing 10.00x10.00mm body 2.45mm height (max) 0.80mm pitch	44-Lead Quad Plastic Chip Carrier .653x.653in body .180in height (max) .050in pitch						
HV5622	HV5622PG-G	HV5622PJ-G						





-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
Supply voltage, V _{DD} ¹	-0.5V to +15V
Output voltage, V _{PP} ¹	-0.5V to +230V
Logic input levels ¹	-0.5V to V _{DD} +0.5V
Ground current ²	1.5A
Continuous total power dissipation ³	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

- All voltages are referenced to V_{ss}
- 2. Duty cycle is limited by the total power dissipated in the package
- For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.

Recommended Operating Conditions

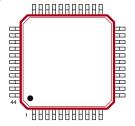
Sym	Parameter	Min	Max	Units
V _{DD}	Logic voltage supply	10.8	13.2	V
HV _{OUT}	High voltage output	-0.3	+220	V
V _{IH}	Input high voltage	V _{DD} -2.0	V _{DD}	V
V _{IL}	Input low voltage	0	2.0	V
f _{CLK}	Clock frequency	-	8.0	MHz
T _A	Operating free-air temperature	-40	+85	οС

Power-Up Sequence

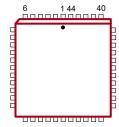
Power-up sequence should be the following:

- Connect ground
- 2. Apply V_{DD}
- 3. Set all inputs to a known state

Pin Configurations



44-Lead PQFP (PG) (top view)



44-Lead PLCC (PJ) (top view)

Product Marking

Top Marking



Bottom Marking

CCCCCCC

YY = Year Sealed WW = Week Sealed

L = Lot Number

C = Country of Origin*

A = Assembler ID*

= "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si or 🌎

44-Lead PQFP (PG)

Top Marking

Tyww AAA

HV5622PJ

LLLLLLLLL

Bottom Marking

ccccccccc

YY = Year Sealed WW = Week Sealed

L = Lot Number A = Assembler ID

C = Country of Origin*

= "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si or

44-Lead PLCC (PJ)

Power-down sequence should be the reverse of the above.

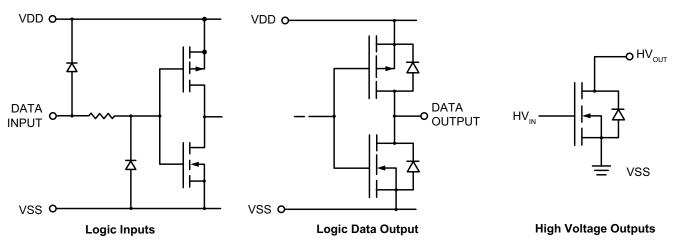
Electrical Characteristics (over recommended operating conditions unless otherwise noted) **DC Characteristics**

Sym	Parameter		Min	Max	Units	Conditions
I _{DD}	V _{DD} supply current		-	15	mA	$f_{CLK} = 8.0MHz, F_{DATA} = 4.0MHz$
I _{DDQ}	V _{DD} supply current (quiesce	nt)	-	100	μA	D _{IN} = 0V, all outputs off
I _{O(OFF)}	Off state output current	-	10	μA	All outputs high, all SWS parallel	
I _{IH}	High-level logic input currer	-	1.0	μA	$V_{IH} = V_{DD}$	
I _{IL}	Low-level logic input curren	Low-level logic input current			μA	V _{IL} = 0V
V _{OH}	High-level output data out		V _{DD} -1.0V	-	V	I _{DOUT} = -100μA
V	Low lovel output voltage	HV _{out}	-	15	V	I _{HVOUT} = +100mA
V _{OL}	Low-level output voltage	DATA OUT	-	1.0	V	I _{DOUT} = +100μA
V _{oc}	HV _{OUT} clamp voltage	-	-1.5	V	I _{OL} = -100mA	

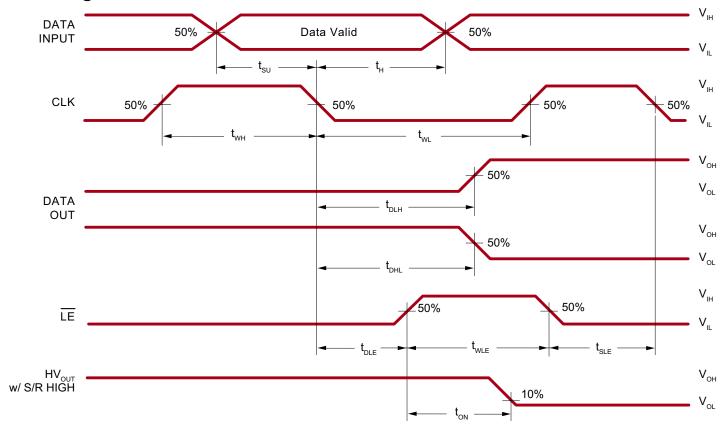
AC Characteristics $(V_{DD} = 12V, T_C = 25^{\circ}C)$

Sym	Parameter	Min	Max	Units	Conditions
f _{CLK}	Clock frequency	-	8.0	MHz	
t _w	Clock width, high or low	62	-	ns	
t _{su}	Data set-up time before CLK falls	25	-	ns	
t _H	Data hold time after CLK falls	10	-	ns	
t _{on}	Turn-on time, HV _{OUT} from enable	-	500	ns	$R_L = 2.0 K\Omega$ to V_{PP} max.
t _{DHL}	Delay time clock to data high to low	-	100	ns	C _L = 15pF
t _{DLH}	Delay time clock to data low to high	-	100	ns	C _L = 15pF
t _{DLE}	Delay time clock to LE low to high	50	-	ns	
t _{WLE}	Width of LE pulse	50	-	ns	
t _{SLE}	LE setup time before clock falls	50	-	ns	

Input and Output Equivalent Circuits



Switching Waveforms



Functional Table

diotoliai labic												
			Inputs			Outputs						
Function	Data	CLK	LE	BL	POL	Shift	Reg	HV Outputs		Data Out		
	Dala	CLK	LE	DL	POL	1	232	1	232	*		
All on	Х	Х	Х	L	L	*	**	On	OnOn	*		
All off	Х	Х	Х	L	Н	*	**	Off	OffOff	*		
Invert mode	Х	Х	L	Н	L	*	**	*	**	*		
Load S/R	H or L	1	L	Н	Н	H or L	**	*	**	*		
Load latabas	Х	H or L	1	Н	Н	*	**	*	**	*		
Load latches	Х	H or L	1	Н	L	*	**	*	**	*		
Transparent latch	L	↓	Н	Н	Н	L	**	Off	**	*		
mode	Н	↓	Н	Н	Н	Н	**	On	**	*		

Notes

 $H = high\ level,\ L = low\ level,\ X = irrelevant,\ \downarrow = high-to-low\ transition,\ \uparrow = low-to-high\ transistion.$

^{*} dependent on previous stage's state before the last $CLK \downarrow or$ last \overline{LE} high.

44-Lead PQFP Pin Assignment (PG)

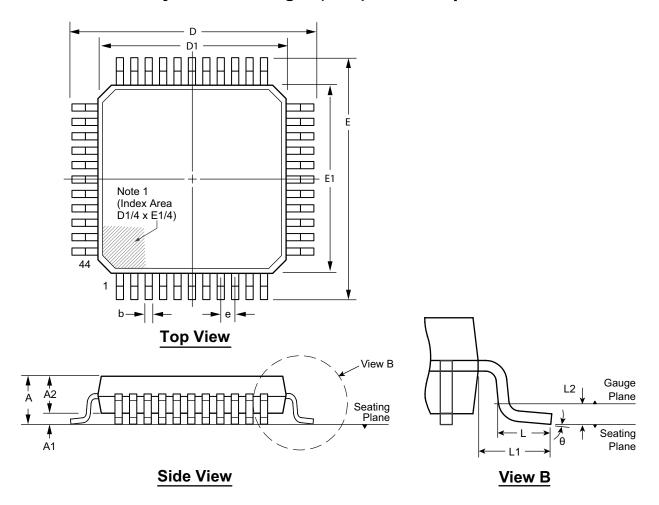
		Din #
Description	Function	Pin #
	HV _{OUT} 22	1
	HV _{OUT} 21	2
	HV _{OUT} 20	3
	HV _{out} 19	4
	HV _{out} 18	5
	HV _{out} 17	6
	HV _{out} 16	7
	HV _{out} 15	8
	HV _{OUT} 14	9
	HV _{out} 13	10
High voltage outputs.	HV _{out} 12	11
- Ingri voltage outpate.	HV _{out} 11	12
	HV _{out} 10	13
	HV _{out} 9	14
	HV _{out} 8	15
	HV _{out} 7	16
	HV _{out} 6	17
	HV _{out} 5	18
	HV _{out} 4	19
	HV _{OUT} 3	20
	HV _{OUT} 2	21
	HV _{out} 1	22
Data output pin.	DATA OUT	23
	N/C	24
No internal connection.	N/C	25
	N/C	26
Inverts the polarity of the HV _{OUT} pins	POL	27
Clock pin, shift registers shifts data on falling edge of input clock.	CLK	28
Reference voltage, usually ground.	VSS	29
Logic supply voltage.	VDD	30
Latch enable pin, data is shifted from shift register to latches on logic input high.	LE.	31
Data input pin.	DATA IN	32
 Blanking pin sets all HV _{OUT} pins low or high depending upon state of polarity. See function table.	BL	33
No internal connection.	N/C	34
	HV _{OUT} 32	35
		36
		37
		38
High voltage outputs	HV _{OUT} 28	39
nign voitage outputs.		40
	HV _{OUT} 26	41
	HV _{оυт} 25	42
	1	43
		44
Data input pin. Blanking pin sets all HV _{OUT} pins low or high depending upon state of polarity. See function table.	N/C HV _{OUT} 32 HV _{OUT} 31 HV _{OUT} 30 HV _{OUT} 29 HV _{OUT} 28 HV _{OUT} 27 HV _{OUT} 26	33 34 35 36 37 38 39 40 41 42 43

44-Lead PLCC Pin Assignment (PJ)

Pin#	Function	Description
		Description
1	HV _{OUT} 17	
2	HV _{OUT} 16	
3	HV _{OUT} 15	
4	HV _{OUT} 14	
5	HV _{out} 13	
6	HV _{out} 12	
7	HV _{out} 11	
8	HV _{out} 10	
9	HV _{OUT} 9	High voltage outputs.
10	HV _{OUT} 8	
11	HV _{out} 7	
12	HV _{out} 6	
13	HV _{out} 5	
14	HV _{out} 4	
15	HV _{out} 3	
16	HV _{out} 2	
17	HV _{out} 1	
18	DATA OUT	Data output pin.
19	N/C	
20	N/C	No internal connection.
21	N/C	
22	POL	Inverts the polarity of the HV _{OUT} pins
23	CLK	Clock pin, shift registers shifts data on falling edge of input clock.
24	VSS	Reference voltage, usually ground.
25	VDD	Logic supply voltage.
26	<u>LE</u>	Latch enable pin, data is shifted from shift register to latches on logic input high.
27	DATA IN	Data input pin.
28	BL	Blanking pin sets all HV _{OUT} pins low or high depending upon state of polarity. See function table.
29	N/C	No internal connection.
30	HV _{OUT} 32	
31	HV _{OUT} 31	
32	HV _{OUT} 30	
33	HV _{out} 29	
34	HV _{OUT} 28	
35	HV _{OUT} 27	
36	HV _{out} 26	
37	HV _{OUT} 25	High voltage outputs.
38	HV _{OUT} 24	
39	HV _{OUT} 23	
40	HV _{OUT} 22	
41	HV _{OUT} 21	
42	HV _{OUT} 20	
43	HV _{out} 19	
44	HV _{оит} 18	
	1 001	

44-Lead PQFP Package Outline (PG)

10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch



Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbo	ol	Α	A1	A2	b	D	D1	E	E1	е	L	L1	L2	θ
Dimension (mm)	MIN	1.95*	0.00	1.95	0.30	13.65*	9.80*	13.65*	9.80*	0.80 BSC 0.88				0 °
	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00		1.95 0.25 REF BSC	3.5°		
	MAX	2.35	0.25	2.10	0.45	14.15*	10.20*	14.15*	10.20*		1.03			7 °

JEDEC Registration MO-112, Variation AA-2, Issue B, Sep.1995.

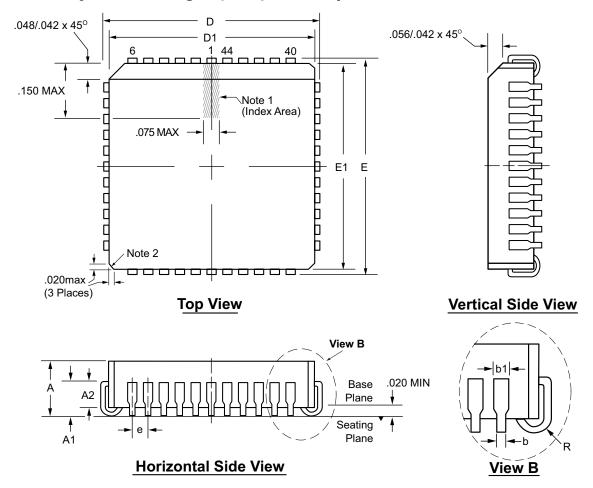
Drawings not to scale.

Supertex Doc. #: DSPD-44PQFPPG, Version C041309.

^{*} This dimension is not specified in the JEDEC drawing.

44-Lead PLCC Package Outline (PJ)

.653x.653in body, .180in height (max), .050in pitch



Notes:

- A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
- 2. Actual shape of this feature may vary.

Symb	ol	Α	A1	A2	b	b1	D	D1	E	E1	е	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650		.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653	.050 BSC	.035
	MAX	.180	.120	.083	.021	.036 [†]	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-44PLCCPJ, Version F031111.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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