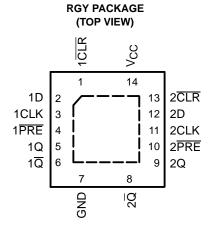
FEATURES

- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 1.8 ns at 1.8 V
- Low Power Consumption, 10-µA Max I_{cc}
- ±8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION



This dual positive-edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs. To better optimize the flip-flop for higher frequencies, the CLR input overrides the PRE input when they are both low.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T _A	PACKAG	E ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 85°C	QFN – RGY	Tape and reel	SN74AUC74RGYR	MS74	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

	INP	UTS		OUTI	PUTS
PRE	CLR	CLK	D	Q	Q
L	Н	Х	Х	Н	L
Х	L	Х	Х	L	Н
н	Н	\uparrow	н	н	L
н	Н	\uparrow	L	L	Н
н	н	L	Х	Q ₀	

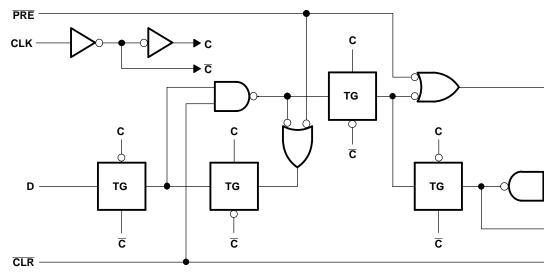
FUNCTION TABLE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SCES483A-AUGUST 2003-REVISED MARCH 2005

LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	3.6	V
VI	Input voltage range ⁽²⁾		-0.5	3.6	V
Vo	Voltage range applied to any output in the hig	h-impedance or power-off state ⁽²⁾	-0.5	3.6	V
Vo	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance ⁽³⁾			47	°C/W
T _{stg}	Storage temperature range				

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed. (2) (3)

The package thermal impedance is calculated in accordance with JESD 51-5.

SCES483A-AUGUST 2003-REVISED MARCH 2005

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	2.7	V
		V _{CC} = 0.8 V	V _{CC}		
V _{IH}	High-level input voltage	V _{CC} = 1.1 V to 1.95 V	$0.65 imes V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 0.8 V		0	
V _{IL}	Low-level input voltage	V _{CC} = 1.1 V to 1.95 V		$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
VI	Input voltage		0	3.6	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 0.8 V		-0.7	
		V _{CC} = 1.1 V		-3	
I _{OH}	High-level output current	V _{CC} = 1.4 V		-5	mA
		V _{CC} = 1.65 V		-8	
		V _{CC} = 2.3 V		-9	
		V _{CC} = 0.8 V		0.7	
		V _{CC} = 1.1 V		3	
I _{OL}	Low-level output current	V _{CC} = 1.4 V		5	mA
		V _{CC} = 1.65 V		8	
		V _{CC} = 2.3 V		9	
$\Delta t/\Delta v$	Input transition rise or fall rate			20	ns/V
T _A	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CON	IDITIONS	V _{cc}	MIN	TYP ⁽¹⁾ MAX	UNIT
		I _{OH} = −100 μA		0.8 V to 2.7 V	V _{CC} – 0.1		
		I _{OH} = -0.7 mA		0.8 V		0.55	
v		I _{OH} = -3 mA		1.1 V	0.8		V
V _{OH}		I _{OH} = -5 mA		1.4 V	1		V
		I _{OH} = -8 mA		1.65 V	1.2		
		I _{OH} = -9 mA		2.3 V	1.8		
		I _{OL} = 100 μA		0.8 V to 2.7 V		0.2	
		I _{OL} = 0.7 mA		0.8 V		0.25	
v		I _{OL} = 3 mA		1.1 V		0.3	V
V _{OL}		I _{OL} = 5 mA		1.4 V		0.4	V
		I _{OL} = 8 mA		1.65 V		0.45	
		I _{OL} = 9 mA		2.3 V		0.6	
I _I		$V_{I} = V_{CC}$ or GND		0 to 2.7 V		±5	μΑ
I _{off}		$V_{I} \text{ or } V_{O} = 2.7 \text{ V}$		0		±10	μA
I_{CC}		$V_I = V_{CC}$ or GND,	$I_{O} = 0$	0.8 V to 2.7 V		10	μA
C	D inputs	$V_I = V_{CC}$ or GND	2.5 V 2		2		۶Ē
Ci	Control inputs	$V_I = V_{CC}$ or GND		2.5 V		2.5	pF

(1) All typical values are at $T_A = 25^{\circ}C$.

SCES483A-AUGUST 2003-REVISED MARCH 2005

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V _{CC} = 0.8 V	8 V V _{CC} = 1.2 V ± 0.1 V		V_{CC} = 1.5 V \pm 0.1 V		V V _{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		100		225		250		300		350	MHz
		CLK high or low	4.6	1.3		0.6		0.5		0.5		
tw	Pulse duration	CLR low	6.6	2		1.5		1.5		1.5		ns
		PRE low	4.8	1.8		1.5		1.5		1.5		
		Data	2.3	1		0.6		0.6		0.7		
t _{su}	t _{su} Setup time before CLK↑	CLR inactive	0	0		0		0		0.3		ns
	OERT	PRE inactive	0	0		0		0.2		0.3		
t _h	Hold time, data aft	er CLK↑	2.1	0.3		0.3		0.3		0.3		ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = ± 0.	1.2 V 1 V	V _{CC} = ± 0.			_c = 1.8 0.15 V		V _{CC} = ± 0.		UNIT
	(INPUT)	(001901)	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f _{max}			100	225		250		300			350		MHz
	CLK		9.5	1.3	4	0.7	2.5	0.5	1.2	2.1	0.5	1.4	
t _{pd}	CLR	Q or Q	10.5	1.5	4.1	1.1	2.9	0.9	1.4	2.4	0.7	1.6	ns
	PRE		12	1.6	4.7	1.1	2.8	0.9	1.4	2.4	0.7	1.6	

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	v _c	_c = 1.8 0.15 V	v,	V_{CC} = 2.5 V ± 0.2 V		UNIT
	(INFOT)	(001P01)	MIN	TYP	MAX	MIN	MAX	
f _{max}			300			350		MHz
	CLK		1.2	1.9	2.8	1	2.2	
t _{pd}	CLR	Q or Q	1.3	2.1	3	1.1	2.4	ns
	PRE		1.3	2.1	3.1	1.1	2.5	

Operating Characteristics

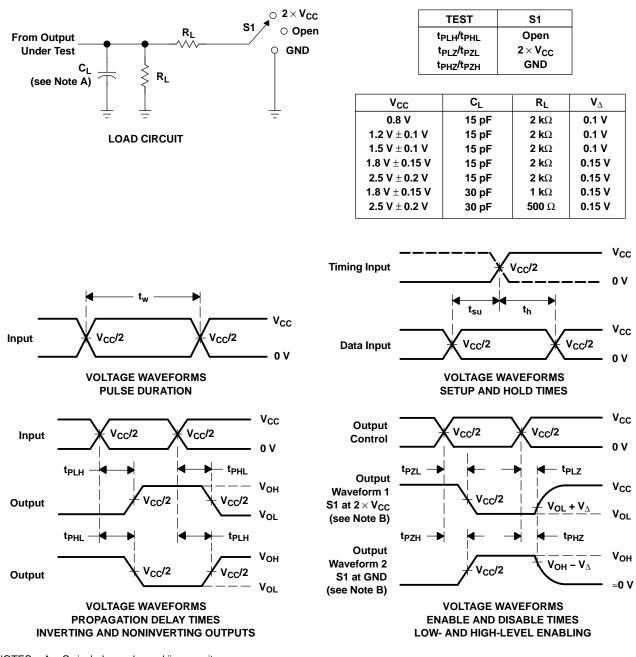
 $T_A = 25^{\circ}C$

· A _									
	PARAMETER	TEST	$V_{CC} = 0.8 V$	V _{CC} = 1.2 V	V_{CC} = 1.5 V	V _{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT	
	FARAMETER	CONDITIONS	ТҮР	TYP	TYP	TYP	TYP	UNIT	
C _{pd}	Power dissipation capacitance	f = 10 MHz	36	36	36	37	41	pF	



SCES483A-AUGUST 2003-REVISED MARCH 2005





NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , slew rate \geq 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins I	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AUC74RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74AUC74RGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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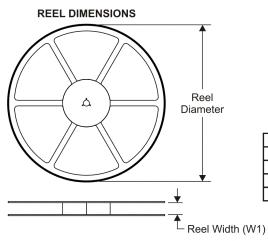
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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC74RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

20-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC74RGYR	VQFN	RGY	14	3000	346.0	346.0	29.0

MECHANICAL DATA



- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- earrow Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
- The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



RGY (S-PVQFN-N14)

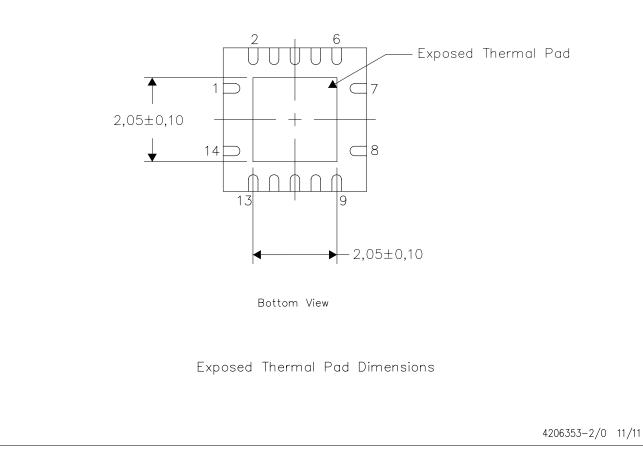
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

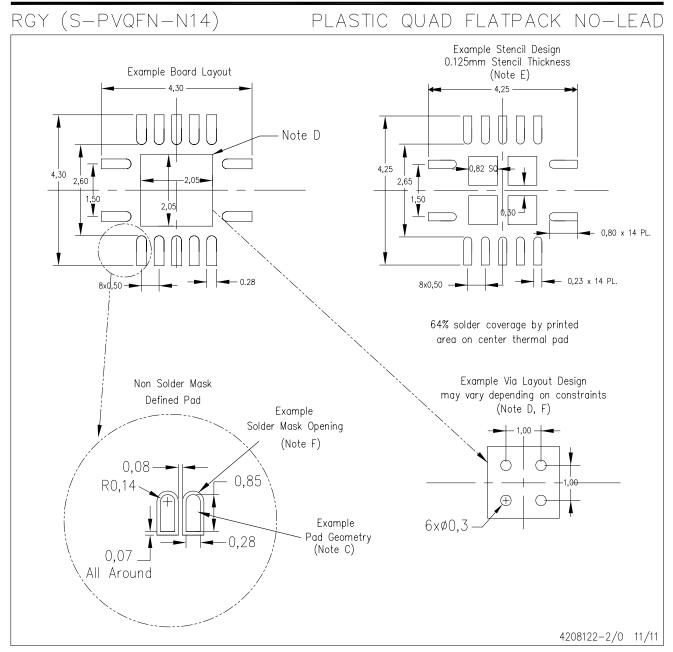
For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.

- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



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