AUDIO MODULATED LED DRIVER

November 2011

GENERAL DESCRIPTION

The IS31FL3189 is an LED driver with an audio synchronization mode that virtually eliminates the need of real time software processing for LED lighting effects.

The OUT0~9 can be operated at 4 basic modes:

Audio synchronization mode, top-down scan mode, constant current mode, combination of audio synchronization and top-down scan mode.

Each of the OUT0~2, OUT7~9 is a constant current sink pulse width modulated in 256 steps, featuring One Shot Programming mode and Interface Intensity Control mode for RGB lighting effects. The output current is user selectable to be one of 5 levels, 17.5mA, 28.9mA, 38.9mA, 46.7mA or 66.5mA (typical). At 38.9mA the IS31FL3189 outputs require only 0.4V of headroom voltage.

In One Shot Programming mode, the timing characteristics for output current - current ramping up, holding, ramping down and off time, can be adjusted individually so that each output can independently maintain a pre-established pattern without requiring any additional interface activity, thus saving valuable system resources.

In Interface Intensity Control mode, the PWM duty cycle of each output can be independently programmed and controlled in 256 steps to simplify color mixing.

APPLICATIONS

- Cellular phones
- MP3/MP4/CD/minidiskplayers
- Digital picture frame/toys

FEATURES

- 10 outputs each with 38.9mA at 0.4V headroom.
- 2 independently controlled, 6 channels of 256 steps PWM RGB LED drivers with programmable brightness and blinking patterns for LED's lighting effects
- Fully programmable operating modes:
- Audio synchronization mode
- Audio synchronization +Top-down scan mode
- Top-down scan mode
- Constant current mode
- One Shot Programming mode with Gamma correction
- Interface intensity control mode with 256 steps current level setting for RGB lighting effects
- RGB blink/not blink with audio mode
- Each outputs enable/disable individually
- Programmable parameter setting:
- Audio gain setting
- Top-down scan mode output current setting
- Top-down scan mode scan rate setting
- RGB mode output current setting
- Programmable Output Current Level settings
- For Anode-common LEDs
- VDD Range: 3.0V to 5.5V
- Package: QFN-20, 3mm × 3mm

TYPICAL APPLICATION CIRCUIT

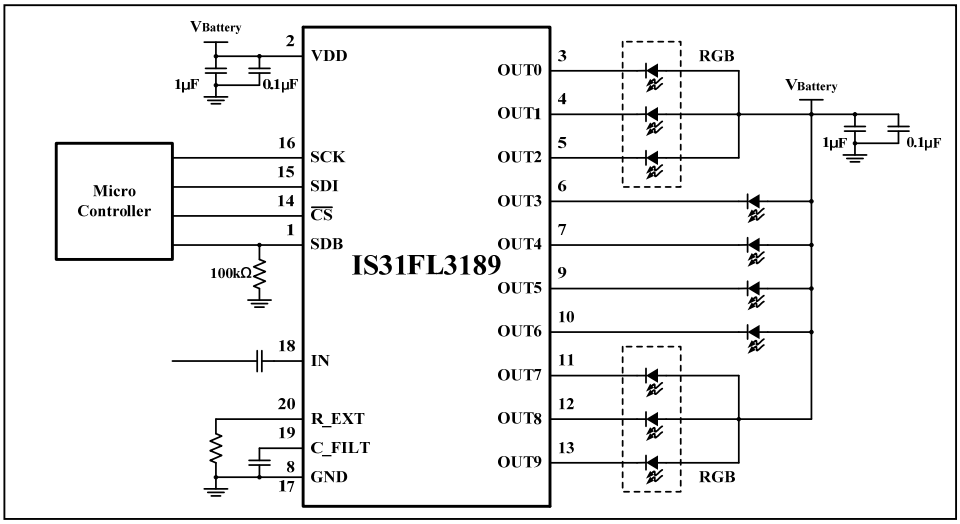
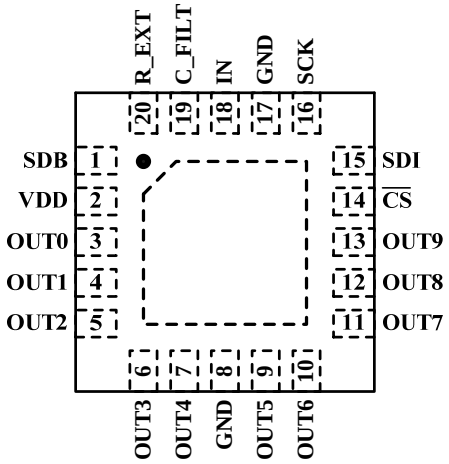


Figure 1 Typical Application Circuit

PIN CONFIGURATION

Package	Pin Configurations (Top View)
QFN-20	

PIN DESCRIPTION

No.	Pin	Description
1	SDB	Shutdown, pull to GND for shutdown mode.
2	VDD	Power supply.
3~7, 9~13	OUT0 ~ OUT9	LED outputs.
8,17	GND	Ground.
14	$\overline{CS}$	Chip select, active is low.
15	SDI	Input serial data for data shift resister.
16	SCK	Input clock for data shift on rising edge.
18	IN	Audio signal input.
19	C_FILT	Low pass filter input.
20	R_EXT	External resistor (R_{EXT}) connect pin to regulate the output current.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION
Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31FL3189-QFLS2-TR	QFN-20, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	−0.3V ~ +6.0V
Voltage at any input pin	−0.3V ~ V_{DD}+0.3V
Junction temperature, T_{JMAX}	−40°C ~ +150°C
Storage temperature range, Tstg	−65°C ~ +150°C
Operating temperature ratings	−40°C ~ +85°C
Junction temperature	150°C
Solder Information, Vapor phase (60s) Infrared (15s)	215°C 220°C

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{DD} = 5V, unless otherwise noted. Limits apply for T_A = 25°C. (*Note 1*)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.0		5.5	V
I_{DD}	Quiescent power supply current	V_{SDB} = V_{DD}		0.7	1.0	mA
I_{SD}	Shutdown current	V_{SDB} = GND		0.04	1.0	μA
	Software shutdown	V_{SDB} = VDD		1.7	3	μA
I_{OUT}	Average output current	Audio synchronization mode V_{DS} = 0.6V, gain = 12dB, R_{EXT} = 1kΩ Vin = 0.5Vp-p square wave		6.9		mA
		Top-down scan mode, Audio input Gain Register with default value V_{DS} = 0.6V, R_{EXT} = 1kΩ When OUT_X turned on		11.4		mA
		Interface Intensity Control mode PWM duty cycle = 0xFF,V_{DS} = 0.6V OUT0~OUT2, OUT7~OUT9		38.9		mA
V_{HR}	Current sink headroom voltage	I_{OUT} = 38.9mA		400.0		mV
SCK, SDI,$\overline{CS}$, SDB Logic Electrical Characteristics						
$V_{IN(0)}$	Logic "0" input voltage	V_{DD} = 3V			0.4	V
$V_{IN(1)}$	Logic "1" input voltage	V_{DD} = 5.5V	1.4			V
$I_{IN(0)}$	Logic "0" input current	V_{IN} = 0V		5.0		nA (Note 2)
$I_{IN(1)}$	Logic "1" input current	V_{IN} = V_{DD}		5.0		nA (Note 2)

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 2)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{CK}	SCK Frequency				1.0	MHz
t_{CH}	SCK High Time		200			ns
t_{CL}	SCK Low Time		200			ns
t_{DH}	SDI SetupTime		50			ns
t_{DS}	SDI High Time		50			ns
t_{CSS}	$\overline{CS}$ to SCK Rise Setup Time		250			ns
t_{CSCP}	$\overline{CS}$ Rising Edge to SCK Rising Edge		200			ns
t_{CSH}	$\overline{CS}$ Pulse High Time		300			ns

Note 1: Production testing of the device is performed at 25°C. Functional operation of the device and parameters specified over other temperature range, are guaranteed by design, characterization and process control.
Note 2: Guaranteed by design.

SPI INTERFACE

The IS31FL3189 contains a 16bit SPI interface to access the internal data and control registers of the device (see Registers Definitions). This module is used to receive the commands transmitted by MCU. The 16-bit serial interface uses three pins, SDI, SCK and $\overline{CS}$ to enter data, Table 1 shows the functions of these three pins. Data read is not available and data entered must be 16 bits.

Table 2 shows the structure of the 16-bit command word and Figure 2 shows the timing diagram of this serial interface. When the SPI block is idle, the MCU must maintain HIGH. For the MCU to transmit data to the IS31FL3189, $\overline{CS}$ must be pulled LOW and remain LOW during the time of command transmission. The first 8 bits are address bits and the remaining 8 bits are data bits.

Table 1 Serial Pins

Signal Name	Attribute	Direction	Description
SCK	Edge Triggered	MCU-> IS31FL3189	Serial bus clock
SDI	Level	MCU -> IS31FL3189	Serial data
$\overline{CS}$	Active Low	MCU -> IS31FL3189	SPI bus selection

Table 2 16-Bit Serial Data Format

A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
MSB	Register Address (see Table 3)						LSB	MSB	Data						LSB

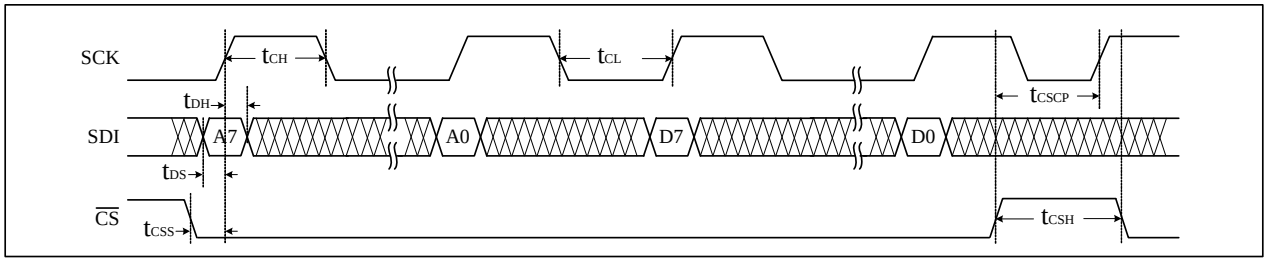


Figure 2 Interface Timing

REGISTERS DEFINITION

The IS31FL3189 device contains 32 Registers, which are listed in Table 3. Communication to the IS31FL3189 is via the serial interface. The command consists of an 8-bit address word followed by an 8-bit data word.

Table 3 Register Function Map

Address	Name	Function	Table	Default
00h	Configuration	Configure the operation mode	4	0000 0001
01h	Audio input gain	Set audio input gain	5	0000 0000
02h	RGB mode	Set RGB mode	6	
03h	RGB Gain1	Set RGB current	7	
04h	OUT0_PWM	Set OUT0 PWM duty cycle	8	0000 0000 (Note 1)
05h	OUT1_PWM	Set OUT1 PWM duty cycle	8	
06h	OUT2_PWM	Set OUT2 PWM duty cycle	8	
07h	OUT7_PWM	Set OUT7 PWM duty cycle	8	
08h	OUT8_PWM	Set OUT8 PWM duty cycle	8	
09h	OUT9_PWM	Set OUT9 PWM duty cycle	8	
0Ah	OUT0_T0	OUT0 holdoff delay time	9	0000 0000 (Note 2)
0Bh	OUT1_T0	OUT1 holdoff delay time	9	
0Ch	OUT2_T0	OUT2 holdoff delay time	9	
0Dh	OUT7_T0	OUT7 holdoff delay time	9	
0Eh	OUT8_T0	OUT8 holdoff delay time	9	
0Fh	OUT9_T0	OUT9 holdoff delay time	9	
10h	OUT0_T1&T2	OUT0 ramping up time and hold time	10	
11h	OUT1_ T1&T2	OUT1 ramping up time and hold time	10	
12h	OUT2_ T1&T2	OUT2 ramping up time and hold time	10	
13h	OUT7_ T1&T2	OUT7 ramping up time and hold time	10	
14h	OUT8_ T1&T2	OUT8 ramping up time and hold time	10	
15h	OUT9_ T1&T2	OUT9 ramping up time and hold time	10	
16h	OUT0_T3&T4	OUT0 ramping down time and off time	11	
17h	OUT1_T3&T4	OUT1 ramping down time and off time	11	
18h	OUT2_T3&T4	OUT2 ramping down time and off time	11	
19h	OUT7_T3&T4	OUT7 ramping down time and off time	11	
1Ah	OUT8_T3&T4	OUT8 ramping down time and off time	11	
1Bh	OUT9_T3&T4	OUT9 ramping down time and off time	11	
1Ch	Update	Update data of register 0Ah~1Bh		xxxx xxxx (Note 3)
1Dh	OUT7-0_EN	Enable OUT7~0	12	1111 1111 (Note 4)
1Eh	OUT9-8_EN	Enable OUT9~8	13	11xx xxxx (Note 4)
1Fh	Town-down_EN	Top-down scan mode enable	14	00000000
20h	RGB Gain2	Set RGB current	15	00000000

Note:
1. In Interface Intensity Control mode, the PWM duty cycle is defined by input data set in register 04h-09h.
2. In One Shot Programming mode, the PWM duty cycle is defined by T0-T4.T0 is holdoff delay time.T1 is Gamma-Corrected ramping up time.T2 is hold time.T3 is Gamma-Corrected ramping down time.T4 is off time. The section Embedded Breathing RGB Lighting Effects in application discuss more about time registers.
3. Write any 8 bit data to the update register after set the value of T0~T4 to update the value of them.
4. In OUT7-0_EN register, OUT7 is controlled by the MSB. For example, we send 0111 1111 to OUT7-0_EN register to disable OUT7，but other output channels are enabled. In OUT9-8_EN register, D7 controls the OUT9, D6 controls the OUT8.

Table 4 Configuration Register (00h)

Bit	D7:D6	D5	D4	D3:D1	D0
Name	MOD	SDRGB1	SDRGB2	SR	SSD
Default	00	0	0	000	1

The Configuration Register controls IS31FL3189 operation mode.

MOD IS31FL3189 Mode Selection
00 Top-down Scan Plus Audio Synchronization Mode
01 Audio Synchronization Mode
10 Top-down Scan Mode

SDRGB1 RGB1 (OUT0~OUT2) PWM Control Mode Enable
0 Disable
1 Enable

SDRGB2 RGB2 (OUT7~OUT9) PWM Control Mode Enable
0 Disable
1 Enable

SR Scan Rate of Top-down Scan Mode Selection
000 Normal Rate, Δt=22ms
001 Normal Rate×2
010 Normal Rate×4
011 Normal Rate/2
100 Normal Rate/4

SSD Software Shutdown Mode Enable
0 Chip Enable
1 Chip Disable

Table 5 Audio Input Gain Register (01h)

Bit	D7:D5	D4:D2	D1:D0
Name	AG	RC	-
Default	000	000	00

The Audio Input Gain Register sets the audio input gain of IS31FL3189 and the current of scan mode

AG Audio Gain Adjust Bits
000 0dB
001 3dB
010 6dB
011 9dB
101 12dB
110 16dB
111 20dB
100 24dB

RC Current of Scan Mode Selection
000 11mA
001 17mA
010 24mA
011 30mA
100 40mA
101 9mA
110 7mA
111 5mA

Table 6. RGB Mode Register (02h)

Bit	D7	D6	D5	D4	D3:D0
Name	BK1	BK2	MRGB1	MRGB2	-
Default	0	0	0	0	0000

When PWM control mode is aroused (D5 or D4 of 00h is set to 1), the RGB Mode Register selects the operation mode.

BK1 RGB1 (OUT0~OUT2) Blinking With Audio Enable
0 Disable
1 Enable

BK2 RGB2 (OUT7~OUT9) Blinking With Audio Enable
0 Disable
1 Enable

MRGB1 RGB1 (OUT0~OUT2) Mode Selection
0 Interface Intensity Control Mode
1 One Shot Programming Mode

MRGB2 RGB2 (OUT7~OUT9) mode selection
0 Interface Intensity Control Mode
1 One Shot Programming Mode

Table 7 RGB Gain1 Register (03h)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BG1		BG2		RGB1_C		RGB2_C	
Default	0	0	0	0	0	0	0	0

When PWM control mode is aroused (D5 or D4 of 00h is set to 1), The RGB Gain1 Register selects the gain and maximum current.

BG1 Audio Gain of RGB1 When Blinking With Audio
00 0dB
01 3dB
10 6dB
11 -3dB

BG2 Audio Gain Of RGB2 When Blinking With Audio
00 0dB
01 3dB
10 6dB
11 -3dB

RGB1_MAX Maximum Current For RGB1 (Typ.)
00 38.9mA
01 46.7mA
10 66.5mA
11 28.9mA

RGB2_MAX Maximum Current For RGB2 (Typ.)
00 38.9mA
01 46.7mA
10 66.5mA
11 28.9mA

Default the outputs each with 38.9mA current capability, they are adjustable. The RGB current register allows the maximum output current to be scaled as indicated in Table above. The IS31FL3189 provides for a maximum current ranging as high as 66.5mA and as low as 28.9mA. Care must be taken so as not to exceed the maximum allowable power dissipation for the device.

Table 8 OUTx_PWM Register (04h~09h)

Bit	D7:D0
Name	PWM
Default	0000 0000

In Interface Intensity Control mode, the PWM duty cycle is defined by input data set in register 04h-09h.

OUT0_PWM register acts when D5 of RGB mode register is set to 0, the value of OUT0_PWM register decides the average output current of OUT0, the average output current may be computed using the formula,

$$I_{OUT} = \frac{38.9mA}{256} * \sum_{n=0}^{7} 2^n$$

Where n stands for the set bit sequence number, for D4, n=4. An example:

D7~D0=10110101,

I_{OUT} =38.9mA*(2^0+2^2+2^4+2^5+2^7)/256

=27.4mA.

See Table 14 in Application Information for more.

OUT1 ~OUT2, OUT7 ~OUT9 PWM register are the same as OUT0 PWM register.

Time Registers

In One Shot Programming mode, the PWM duty cycle is defined by T0-T4.

By programming different values of T0~T4 for the different outputs, OUT0~OUT2, OUT7~OUT9, many different combinations LED effects can be created.

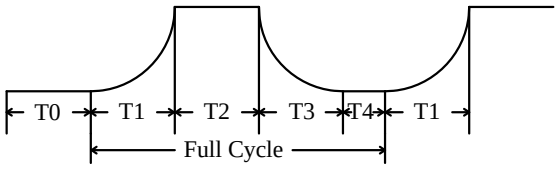


Figure 3 Timing Parameters

The complete waveform period consists of the summation of all times T1~T4.

Table 9 OUTx_T0 Register (0Ah~ 0Fh)

Bit	D7:D4	D3:D0
Name	T0	-
Default	0000	0000

T0 is the holdoff delay before the waveform (described by the values of T1~T4) begins as shown in Figure 3. The holdoff delay occurs only after 1) any 8-bit value is written to the update register (0Ch), or 2) turn on the One Shot Programming mode by programming the RGB Mode Register (02h)

All output T0 registers (0Ah~0Fh) are programmed in the same manner.

T0	Time Delay Of Output Current		
0000	0s	0001	0.13s
0010	0.26s	0011	0.52s
0100	1.04s	0101	2.08s
0110	4.16s	0111	8.32s
1000	16.64s	1001	33.28s
1010	66.56s		

Table 10 OUTx_T1&T2 Register (10h~15h)

Bit	D7:D5	D4:D1	D0
Name	T1	T2	-
Default	000	0000	0

T1: T1 is the time that the output current ramps up to its final value. It is Gamma-Corrected and consists of 32 steps and the PWM duty cycle is increasing at each step as shown in Table 17.

T2: T2 is the time the output holds its maximum current.

All output T1, T2 registers (10h~15h) are programmed in the same manner.

T1	Ramping Up Time		
000	0.13s	001	0.26s
010	0.52s	011	1.04s
100	2.08s	101	4.16s
110	8.32s	111	16.64s

T2	Holding Full Current Time		
0000	0s	0001	0.13s
0010	0.26s	0011	0.52s
0100	1.04s	0101	2.08s
0110	4.16s	0111	8.32s
1000	16.64s		

Table 11 OUTx_T3&T4 Register (16h~1Bh)

Bit	D7:D5	D4:D1	D0
Name	T3	T4	-
Default	000	0000	0

T3: T3 is the time that the output current ramps down from the maximum value to zero. It is Gamma-Corrected and consists of 32 steps and the PWM duty cycle is reducing at each step as shown in Table 17.

T4: T4 is the time delay before repeating the next cycle.

All output T3, T4 registers (16h~1Bh) are programmed in the same manner.

T3	Ramping Down Time		
000	0.13s	001	0.26s
010	0.52s	011	1.04s
100	2.08s	101	4.16s
110	8.32s	111	16.64s

T4	Holding Off Time		
0000	0s	0001	0.13s
0010	0.26s	0011	0.52s
0100	1.04s	0101	2.08s
0110	4.16s	0111	8.32s
1000	16.64s	1001	33.28s
1010	66.56s		

Update Register (1Ch)

Once configured, the timing parameters, T0 thru T4, may only be changed by modifying the values stored in the timing registers (0Ah~1Bh), followed by writing any 8-bit value to the update register. The new timing parameters will take effect following the write to the update register.

Table 12 OUT7-0_EN Register (1Dh)

Bit	D7	D6:D1	D0
Name	OUT7_EN	OUT6_EN: OUT1_EN	OUT0_EN
Default	1	111 111	1

Table 13 OUT9-8_EN Register (1Eh)

Bit	D7	D6	D5: D0
Name	OUT9_EN	OUT8_EN	-
Default	1	1	xx xxxx

OUTx_EN Register controls the on or off state of each output.

Notice in register 1Dh, the MSB D7 enables the OUT7, while the LSB D0 enables the OUT0; in register 1Eh, the MSB D7 enables the OUT9, D6 enables the OUT8.

OUTx_EN	Output States
0	Output Off
1	Output On

Table 14 Top-down_EN Registers (1Fh)

Bit	D7:D5	D4	D3: D0
Name	-	$\overline{\text{Top-down\_EN}}$	-
Default	000	0	0000

Top-down_EN Register controls the on or off state of top-down scan mode. This function is designed for the application where constant output current is needed.

When IS31FL3189 is working in top-down scan mode, setting

D4 of Top-down register to “1”， the IS31FL3189 can keep the output always turned on, and the output current range can be set by writing the RC register (D4:D2 of Audio Input Gain Register(01h)).

$\overline{\text{Top-down\_EN}}$	Top-down Scan Mode Enable
0	Enable
1	Disable

Table 15 RGB Gain2 Register (20h)

Bit	D7:D2	D1	D0
Function	-	RGB1_C	RGB2_C
Default	000000	0	0

RGB Gain2 Register makes RGB current on the fifth setting at 17.5mA.

D1	RGB1 Current Setting
1	RGB1 Current is Set To 17.5mA
0	RGB1 Current is Set By REG 03h

D0	RGB2 Current Setting
1	RGB2 Current is Set To 17.5mA
0	RGB2 Current is Set By REG 03h

APPLICATION INFORMATION

INITIAL POWER-UP

On initial power-up, the IS31FL3189 registers are reset to their default values, it operates in Top-down scan plus Audio synchronization mode and the RGB outputs are not enabled.

SOFTWARE SHUTDOWN

The IS31FL3189 device features a shutdown mode. Shutdown mode is entered via a write to the Configuration Register (see Table 4). In shutdown mode all of the output current sources are switched off. Shutdown mode can either be used as a means to reduce power consumption or for generating a flashing display (repeatedly entering and leaving shutdown mode).

Note: During shutdown mode the Digit-Registers maintain their data.

CONSTANT CURRENT

The maximum current of OUT0 ~ OUT2, OUT7 ~ OUT9, are internally set to one of 5 constant current levels (17.5mA, 28.9mA, 38.9mA, 46.7mA or 66.5mA (typical)). The constant current sinks maintain the output current at the programmed level when sinking current.

When set to sink 38.9mA, if the voltage at the output pin falls below 0.4V, because of a large LED forward voltage (V_F) or falling supply voltage, then the output current will begin to fall off as decrease of headroom voltage. The selection for the constant current level is made by programming the RGB Gain registers as shown in Table 7 and Table 15.

AUDIO SYNCHRONIZATION ONLY MODE

The IS31FL3189 features an audio synchronization only mode where each LED driver's output current is dependent on the audio input signal. The intensity of any given LED output is dependent upon the amplitude of the audio signal. An increase in the amplitude of the audio signal will increase the output current of LED driver. The audio synchronization only mode allows each LED output to react to the amplitude of the audio input signal. Audio synchronization only mode is activated by programming the configuration byte bit D7 low and bit D6 high.

The IS31FL3189 has one single-ended analog audio input designated IN, where voice data, MP3, or FM radio data is routed to IN. The gain of the audio input summing amplifier is programmed by the Audio input gain register bit D7~D5. Increasing the gain of the audio input summing amplifier will increase the intensity of the LEDs in audio synchronization only mode.

When the IS31FL3189 is configured to operate in Audio Synchronization only mode and the voltage of the output pin is above the minimum headroom voltage, VDS≥ headroom voltage, the maximum output current of each channel is dependent upon the value of the external programming resistor, R_{EXT}, If the voltage at the output pin is below the minimum headroom voltage, V_{DS}< headroom voltage, the output current will drop to a certain value of current whose headroom is equal to V_{DS}. The maximum output current of each channel is set by an external resistor R_{EXT}, as show in figure 4.

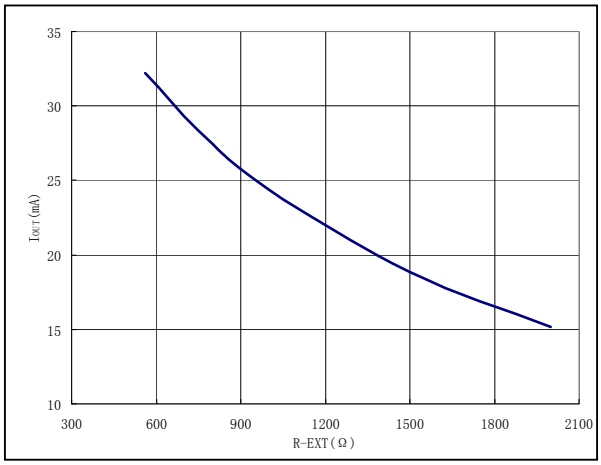


Figure 4 I_{OUT} vs. R_{EXT}

When V_{IN} = 1.35Vp-p sine wave, Gain = 12dB

Careful selection of R_{EXT} and gain setting is required so as not to exceed output current designed for the system. Audio input DC filtering capacitor is absolutely necessary for better signal-to-noise ratio, LED output current uniformity and lighting effects.

TOP-DOWN SCAN MODE

When the IS31FL3189 is configured to operate in Top-down Scan mode, the constant current output is programmed by the Audio input gain register bit D4~D2.

TOP-DOWN SCAN MODE (1)

The IS31FL3189 offers a special lighting effect by controlling the duty cycle and timing of each channel. When RGB mode is enabled, OUT0~OUT2 and OUT7~OUT9 are controlled by RGB mode register bytes, and OUT3~OUT6 will operate as shown below in figure 5 when Configuration register D3~D1 are set low. When the Configuration register D3~D1 are set different, the scan rate can be changed as the commentary of Configuration register.

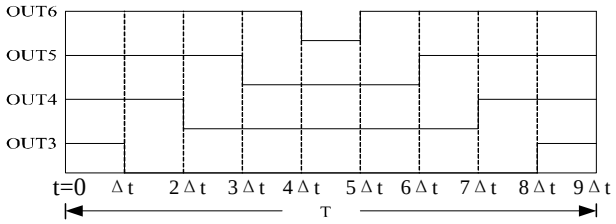


Figure 5 Timing of Top-down Scan Mode (1)

This waveform describes the output voltage of OUT3~OUT6. The output is on when it is low.

0~Δt, all channels turn off, where Δt is 22ms；

Δt~2Δt, OUT3 turns on, OUT4~OUT6 turn off;

2Δt~3Δt, OUT3, OUT4 turn on, OUT5 and OUT6 turn off;

……

7Δt~8Δt, OUT3 turns on, OUT4~OUT6 turn off;

Then next cycle starts again.

TOP-DOWN SCAN MODE (2)

Each RGB can be disabled via Configuration register bit D4 and bit D5.When RGB mode is disabled, The function of OUT0~OUT2 and OUT7~OUT9 is the same as OUT3~OUT6, operating as described by the waveforms below in figure 6 when the Configuration register D3~D1 are set low.

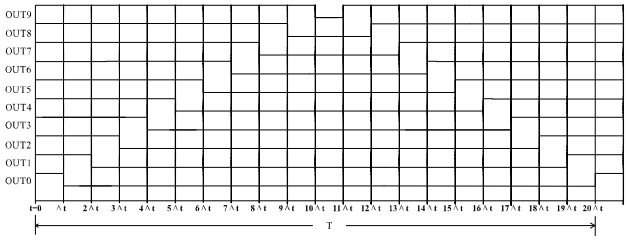


Figure 6 Timing of Top-down Scan Mode (2)

CONSTANT CURRENT MODE

This mode is based on Top-down scan mode and can be enabled by setting D4 of register 1Fh in Table 14, it can maintain a constant current without scan.

The current can be adjusted by programming the current of scan mode, D4:D2 of Audio Input Gain Register.

AUDIO SYNCHRONIZATION PLUS TOP-DOWN SCAN MODE

When initially powering the IC or if the IS31FL3189 is configured to operate in Audio synchronization plus Top-down Scan mode, the output current is programmed as described in Audio synchronization mode section, and the Top-down scan rate is set by the Configuration register D3~D1.

INTERFACE INTENSITY CONTROL MODE

When configuration register (00H) D5 and D4 are set high, the maximum current of output is selected via RGB current register (03H) bits D3~D0. Outputs operate in Interface Intensity Control mode when you clear the RGB mode register bits D5&D4. In this control mode, you must send data if you want to change the PWM intensity of the RGB LEDs.

The IS31FL3189's PWM LED outputs can be used to drive individual color LEDs or RGB LED modules. When driving an RGB LED module, the intensity of each LED in the module is programmable allowing the RGB LED module to be set to many different colors, based on the value of the PWM byte.

When Interface Intensity Control mode is enabled, the average output current of OUT0~OUT2, OUT7~OUT9, is dependent upon the PWM duty cycle. LEDs driven with a higher duty cycle results in a higher luminous intensity. For example, if the maximum output current is 38.9mA, the table below gives some average I_{OUT} values controlled by PWM bytes. The average output current can be adjusted in 256 steps of PWM control.

Table 16 256 Steps Output Current

PMW Byte	I_{OUT} (mA)
0x00	0
0x01	0.15
0x02	0.30
0x03	0.46
… …	… …
0xFF	38.9

ONE SHOT PROGRAMMING MODE

Outputs work in One Shot Programming mode when you set RGB mode register bits D5&D4 to '1'. When the IS31FL3189 is operating in One Shot Programming mode, the output waveform is user configurable by the selection of T0~T4. New values written to T0~T4 will take effect after writing any 8 bits of data to the Update register.

In One Shot Programming mode, the PWM duty cycle is defined by T0-T4.

T0: T0 is the holdoff delay before the waveform (described by the values of T1~T4) begins as shown in Figure 3. The holdoff delay occurs only after 1) any 8-bit value is written to the update register, or 2) turn on the One Shot Programming mode by programming the RGB Mode Register (02h)

T1: T1 is the time that the output current ramps up to its final value. It consists of 32 steps and the PWM duty cycle is increasing at each step as shown in Table 17.

T2: T2 is the time the output holds its maximum current.

T3: T3 is the time that the output current ramps down

from the maximum value to zero. It consists of 32 steps and the PWM duty cycle is reducing at each step as shown in Table 17.

T4: T4 is the time delay before repeating the next cycle.

By programming different values of T0~T4 for the different outputs, OUT0~OUT2, OUT7~OUT9, many different combinations LED effects can be created.

The complete waveform period consists of the summation of all times T1~T4.

Table 17 Gamma-Corrected PWM Duty Cycle (Gamma=1.8)

Gray Scale Data	Duty Cycle (1/256)	Gray Scale Data	Duty Cycle (1/256)
0	0	16	85
1	1	17	95
2	3	18	105
3	5	19	115
4	8	20	125
5	12	21	136
6	16	22	148
7	21	23	160
8	26	24	172
9	32	25	185
10	38	26	198
11	45	27	211
12	52	28	225
13	60	29	239
14	68	30	254
15	76	31	255

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

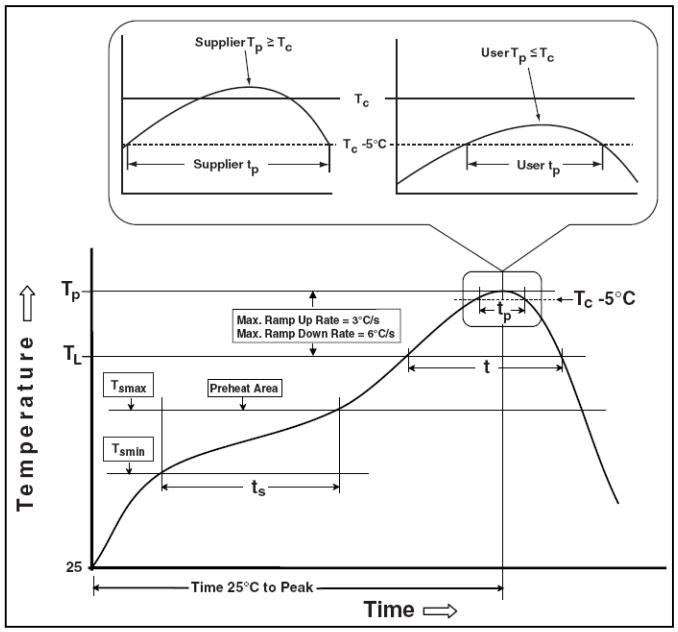
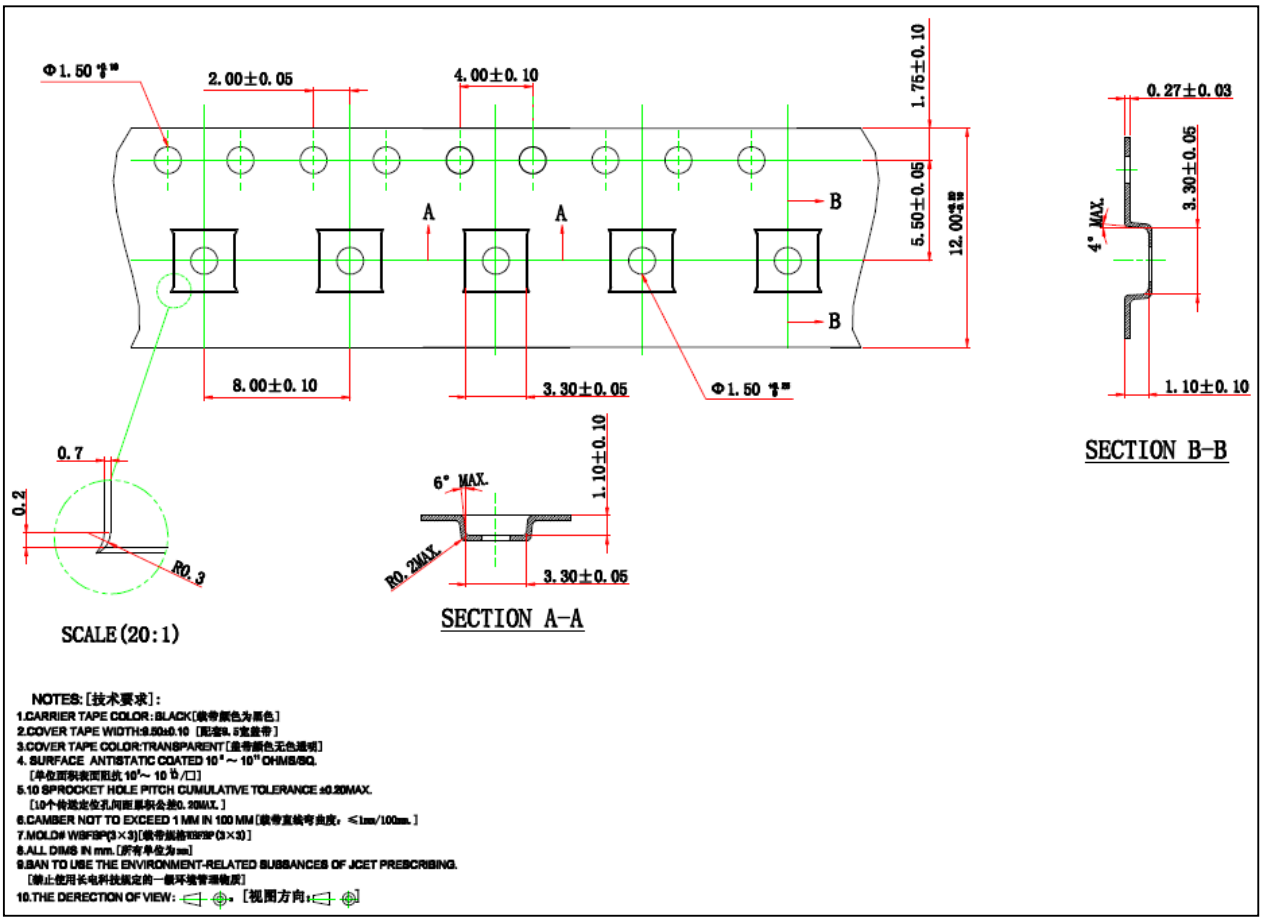


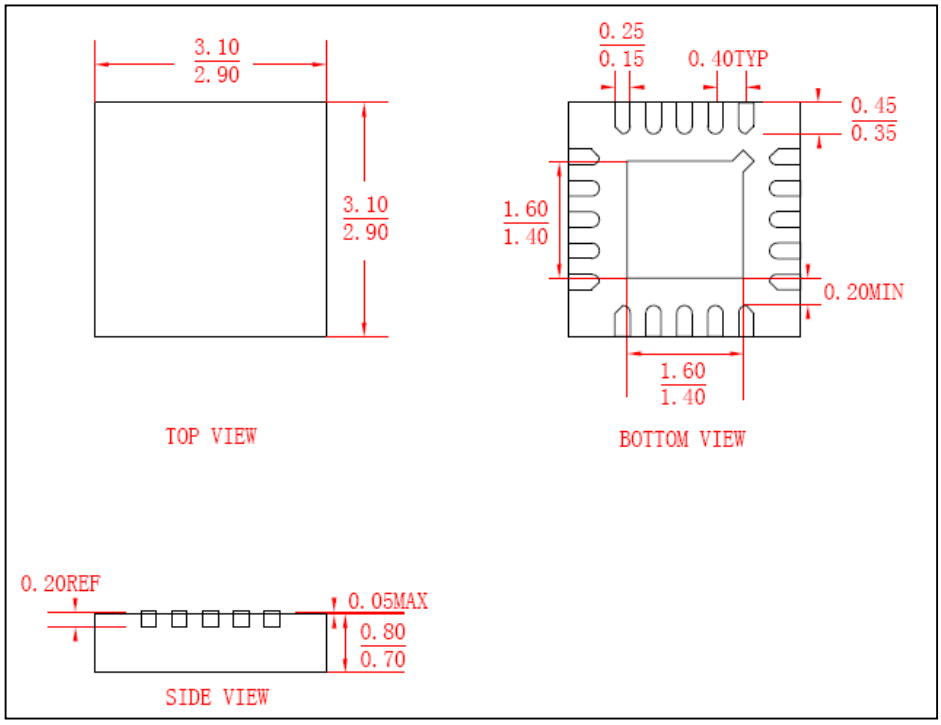
Figure 7 Classification Profile

TAPE AND REEL INFORMATION



PACKAGE INFORMATION

QFN-20



Note: All dimensions in millimeters unless otherwise stated.