IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 16-BIT GENERIC HOST INTERFACES

SCAS190E - JUNE 1990 - REVISED JANUARY 1997

- Members of the Texas Instruments
 SCOPE™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Control Operation of Up to Six Parallel Target Scan Paths
- Accommodate Pipeline Delay to Target of Up to 31 Clock Cycles
- Scan Data Up to 2³² Clock Cycles

- Execute Instructions for Up to 2³² Clock Cycles
- Each Device Includes Four Bidirectional Event Pins for Additional Test Capability
- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- Packaged in 44-Pin Plastic Leaded Chip Carrier (FN), 68-Pin Ceramic Pin Grid Array (GB), and 68-Pin Ceramic Quad Flat Packages (HV)

description

The 'ACT8990 test-bus controllers (TBC) are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of components supports IEEE Standard 1149.1-1990 (JTAG) boundary scan to facilitate testing of complex circuit-board assemblies. The 'ACT8990 differ from other SCOPE™ integrated circuits. Their function is to control the JTAG serial-test bus rather than being target boundary-scannable devices.

The required signals of the JTAG serial-test bus – test clock (TCK), test mode select (TMS), test data input (TDI), and test data output (TDO) can be connected from the TBC to a target device without additional logic. This is done as a chain of IEEE Standard 1149.1-1990 boundary-scannable components that share the same serial-test bus. The TBC generates TMS and TDI signals for its target(s), receives TDO signals from its target(s), and buffers its test clock input (TCKI) to a test clock output (TCKO) for distribution to its target(s). The TMS, TDI, and TDO signals can be connected to a target directly or via a pipeline, with a retiming delay of up to 31 bits. Since the TBC can be configured to generate up to six separate TMS signals [TMS (5–0)], it can be used to control up to six target scan paths that are connected in parallel (i.e., sharing common TCK, TDI, and TDO signals).

While most operations of the TBC are synchronous to TCKI, a test-off (TOFF) input is provided for output control of the target interface, and a test-reset (TRST) input is provided for hardware/software reset of the TBC. In addition, four event [EVENT (3–0)] I/Os are provided for asynchronous communication to target device(s). Each event has its own event generation/detection logic, and detected events can be counted by two 16-bit counters.

The TBC operates under the control of a host microprocessor/microcontroller via the 5-bit address bus [ADRS (4–0)] and the 16-bit read/write data bus [DATA (15–0)]. Read (\overline{RD}) and write (\overline{WR}) strobes are implemented such that the critical host-interface timing is independent of the TCKI period. Any one of 24 registers can be addressed for read and/or write operations. In addition to control and status registers, the TBC contains two command registers, a read buffer, and a write buffer. Status of the TBC is transmitted to the host via ready (\overline{RDY}) and interrupt (\overline{INT}) outputs.

Major commands can be issued by the host to cause the TBC to generate the TMS sequences necessary to move the target(s) from any stable test-access-port (TAP) controller state to any other stable TAP state, to execute instructions in the Run-Test/Idle TAP state, or to scan instruction or test data through the target(s). A 32-bit counter can be preset to allow a predetermined number of execution or scan operations.

Serial data that appears at the selected TDI input (TDI1 or TDI0) is transferred into the read buffer, which can be read by the host to obtain up to 16 bits of the serial-data stream. Serial data that is transmitted from the TDO output is written by the host to the write buffer.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SCOPE and EPIC are trademarks of Texas Instruments Incorporated.



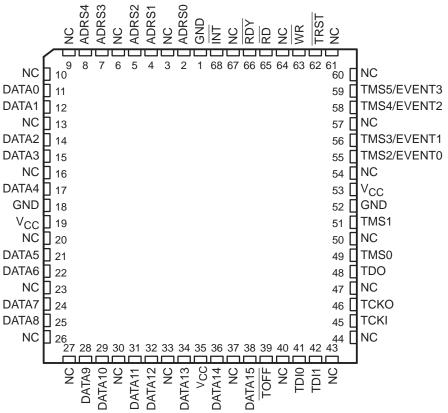
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 16-BIT GENERIC HOST INTERFACES

SCAS190E - JUNE 1990 - REVISED JANUARY 1997

description (continued)

The SN54ACT8990 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT8990 is characterized for operation from 0°C to 70°C.

SN54ACT8990 . . . HV PACKAGE (TOP VIEW)

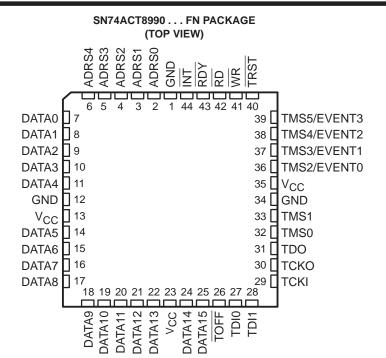


NC - No internal connection



IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 16-BIT GENERIC HOST INTERFACES

SCAS190E - JUNE 1990 - REVISED JANUARY 1997



SN54ACT8990 . . . GB PACKAGE (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
Α		0	0	0	0	0	0	0	0	0	
В	0	0	0	0	\odot	0	\odot	\odot	\odot	0	0
С	0	\odot	\odot							0	0
D	0	0								0	0
Е	0	0								0	0
F	0	0								0	0
G	0	0								0	0
н	0	0								\odot	0
J	0	\odot								\odot	0
ĸ	0	\odot	\odot	\odot	0	\odot	0	0	\odot	\odot	0
L		0	0	0	0	0	0	\odot	0	\odot	

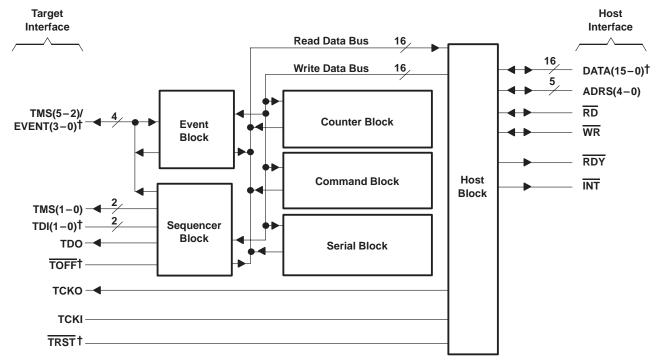


Table 1. Terminal Assignments

TI	ERMINAL		TERMINAL	TI	ERMINAL	Т	ERMINAL
NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME
A2	NC	B10	NC	F11	NC	K6	NC
А3	ADRS4	B11	NC	G1	DATA5	K7	VCC
A4	NC	C1	DATA2	G2	NC	K8	DATA15
A5	ADRS1	C2	DATA1	G10	NC	K9	TDI0
A6	ADRS0	C3	NC	G11	TMS1	K10	NC
A7	NC	C10	TMS4/EVENT2	H1	NC	K11	TCKI
A8	ĪNT	C11	TMS5/EVENT3	H2	DATA6	L2	DATA9
A9	RD	D1	DATA4	H10	TDO	L3	NC
A10	TRST	D2	DATA3	H11	TMS0	L4	DATA12
B1	DATA0	D10	TMS3/EVENT1	J1	DATA8	L5	DATA13
B2	NC	D11	NC	J2	DATA7	L6	NC
В3	ADRS3	E1	NC	J10	TCKO	L7	DATA14
B4	ADRS2	E2	GND	J11	NC	L8	TOFF
B5	NC	E10	VCC	K1	NC	L9	TDI1
B6	NC	E11	TMS2/EVENT0	K2	NC	L10	NC
B7	GND	F1	Vcc	K3	DATA10		·
B8	RDY	F2	NC	K4	DATA11		
B9	WR	F10	GND	K5	NC		

NC - No internal connection

functional block diagram



[†] Inputs have internal pullup resistors.



IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 16-BIT GENERIC HOST INTERFACES SCAS190E – JUNE 1990 – REVISED JANUARY 1997

Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION						
ADRS4-ADRS0	I	Address inputs. ADRS4 – ADRS0 form the 5-bit address bus that interfaces the TBC to its host. These inputs specify the TBC register to be read from or written to.						
DATA15-DATA0	I/O	Data inputs and outputs. DATA15-DATA0 form the 16-bit bidirectional data bus that interfaces the TBC to i host. Data is read from or written to the TBC register using this data bus.						
GND		Ground						
ĪNT	0	Interrupt. INT transmits an interrupt signal to the host. When the TBC requires service from the host, INT is asserted (low). INT will remain asserted (low) until the host has completed the required service.						
NC		No connection						
RD	I	Read strobe. \overline{RD} is the active low output enable for the data bus. \overline{RD} is used as the strobe for reading data from the selected TBC register.						
RDY	0	Ready. $\overline{\text{RDY}}$ transmits a status signal to the host. When the TBC is ready to accept a read or write operation from the host, $\overline{\text{RDY}}$ is asserted (low). $\overline{\text{RDY}}$ is not asserted (high) when the TBC is in recovery from a read, write, command, or reset operation.						
тскі	I	Test clock input. TCKI is the clock input for the TBC. Most operations of the TBC are synchronous to TCKI. When enabled, all target interface outputs change on the falling edge of TCKI. Sampling of target interface inputs are configured to occur on either the rising edge or falling edge of TCKI.						
тско	0	Test clock output. TCKO distributes TCK to the target(s). The TCKO is configured to be disabled, constant zero, constant one, or to follow TCKI. When TCKO follows TCKI, it is delayed to match the delay of generating the TDO and TMS signals.						
TDI1-TDI0	I	Test data inputs. The TDI1-TDI0 serial inputs are used for shifting test data from the target(s). The TDI inputs can be directly connected to the TDO pin(s) of the target(s).						
TDO	0	Test data output. TDO is used for shifting test data into the target(s). TDO can be directly connected to the TDI terminal(s) of the target(s).						
TMS1-TMS0	0	Test mode select outputs. These parallel outputs transmit TMS signals to the target(s), which direct them through their TAP controller states. TMS1-TMS0 can be directly connected to the TMS terminals of the target(s).						
TMS5-TMS2/ EVENT3-EVENT0	I/O	Test mode select outputs or event inputs/outputs. These I/Os can be configured for use as either TMS outputs or event inputs/outputs. As TMS outputs, they function similarly to TMS1-TMS0 above. As event I/Os, they can be used to receive/transmit interrupt signals to/from the target(s).						
TOFF	I	Test-off input. TOFF is the active low output disable for all outputs and I/Os of the target interface (TCKO, TDO, TMS, TMS/EVENT).						
TRST	I	Test-reset input. TRST is used to initiate hardware and software reset operations of the TBC. Hardware reset begins when TRST is asserted (low). Software reset begins when TRST is released (high) and proceeds synchronously to TCKI to completion in a predetermined number of cycles.						
WR	I	Write input. WR is the strobe for writing data to a TBC data register. Signals present at the data and address buses are captured on the rising edge of WR.						
Vcc		Supply voltage						



SN54ACT8990, SN74ACT8990 **TEST-BUS CONTROLLERS**

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 16-BIT GENERIC HOST INTERFACES SCAS190E – JUNE 1990 – REVISED JANUARY 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	\dots -0.5 V to 7 V
Input voltage range, V _I (see Note 1)	\dots -0.5 V to V _{CC}
Output voltage range, V _O (see Note 1)	\dots -0.5 V to V _{CC}
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 2): FN package	
Storage temperature range, T _{stq}	. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book, literature number SCBD002.

recommended operating conditions

		SN54A	CT8990	SN74A	UNIT	
		MIN	MAX	MIN	MAX	ONII
VCC	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
٧ı	Input voltage	0	VCC	0	VCC	V
Vo	Output voltage	0	VCC	0	VCC	V
IOH	High-level output current		-8		-8	mA
loL	Low-level output current		8		8	mA
TA	Operating free-air temperature	-55	125	0	70	°C



IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 16-BIT GENERIC HOST INTERFACES SCAS190E – JUNE 1990 – REVISED JANUARY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ADAMETED	TEST	CONDITIONS	Т	A = 25°C	;	SN54A	CT8990	SN74A	UNIT		
PARAMETER		TEST	CONDITIONS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII	
		$V_{CC} = 4.5 \text{ V}$ $I_{OH} = -20 \mu A$		4.4			4.4		4.4			
,		VCC = 4.5 V	$I_{OH} = -8 \text{ mA}$	3.7			3.7		3.7		V	
VOH		V _{CC} = 5.5 V	I _{OH} = -20 μA	5.4			5.4		5.4] v	
		VCC = 5.5 V	$I_{OH} = -8 \text{ mA}$	4.7			4.7		4.7			
VOL		V _{CC} = 4.5 V	I _{OL} = 20 μA			0.1		0.1		0.1		
VOL	_	to 5.5 V	I _{OL} = 8 mA			0.5		0.5		0.5	V	
	ADRS, RD, WR, TCKI	V _{CC} = 5.5 V,	$V_{I} = V_{CC}$ or GND			±1		±1		±1		
11	TDI, TOFF,	V _{CC} = 5.5 V	$V_I = V_{CC}$			±1		±1		±1	μΑ	
	TRST	vCC = 3.5 v	V _I = GND	-35	-70	-250	-35	-250	-35	-250		
	INT, RDY, TCKO, TDO, TMS	$V_{CC} = 5.5 \text{ V},$	$V_O = V_{CC}$ or GND			±10		±10		±10		
loz‡	DATA,	V00 - 5 5 V	VO = VCC			±10		±10		±10	μΑ	
	TMS/EVENT	V _{CC} = 5.5 V	$V_O = GND$	-35	-70	-250	-35	-250	-35	-250		
		$V_{CC} = 5.5 \text{ V},$ $I_{O} = 0,$	$V_I = V_{CC}$ or GND			450*		450		450	μΑ	
Icc		$V_{CC} = 5.5 \text{ V},$	C _L = 50 pF		100						mA	
		f _{clock} = 30 MH:		100						IIIA		
Ci		V _I = V _{CC} or GND			5*						pF	
Cio		V _I = V _{CC} or G	ND		9*						pF	
Co		V _I = V _{CC} or G	ND		8*						pF	

^{*} On products compliant to MIL-PRF-38535, this parameter does not apply.

[†] Typical values are at $V_{CC} = 5 \text{ V}$.

[‡] For I/O ports, the parameter IOZ includes the input leakage.

SN54ACT8990, SN74ACT8990 **TEST-BUS CONTROLLERS**

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 16-BIT GENERIC HOST INTERFACES SCAS190E – JUNE 1990 – REVISED JANUARY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

			SN54A	CT8990	SN74A	CT8990	UNIT
			MIN	MAX	MIN	MAX	1 UNII
f _{clock}	Clock frequency		0	30	0	30	MHz
		RD low†			5.5		ns
		WR low	5.5		5.5		
t _W	Pulse duration	EVENT high or low	8		8		1
		TCKI high or low	10.5		10.5		ns
		TRST low	6		6		1
		ADRS [†] before RD↑			6.5		ns
		ADRS before WR↑	6.5		6.5		
		DATA before WR↑	6		6		1
t _{su}	Setup time	EVENT before TCKI↑	6		5.5		1
		EVENT before TCKI↓	5		5		ns
		TDI before TCKI↑	2		2		1
		TDI before TCKI↓	2		2		1
		ADRS [†] after RD [↑]			5		ns
		ADRS after WR↑	5.5		5		
		DATA after WR↑	5.5		5.5		1
t _h	Hold time	EVENT after TCKI↑	5.5		5]
		EVENT after TCKI↓	5		5		ns
		TDI after TCKI↑	4		2.5]
		TDI after TCKI↓	4		2.5		1

[†] Applies only in the case where ADRS (4-0) = 10110 (read buffer).



IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 16-BIT GENERIC HOST INTERFACES SCAS190E – JUNE 1990 – REVISED JANUARY 1997

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

DADAMETER	FROM	то	SN54A	CT8990	SN74A	UNIT		
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	I UNII	
f _{max}			30		30		MHz	
^t PLH	ADRS	DATA	8	43	19.5	39.3		
^t PHL	ADRS	DATA	8	43	19.5	39.3	ns	
	RD↑		5.3	17	5.3	13.8		
tPLH -	WR↑	RDY	2.5	16	2.5	13	ns	
^t PLH	- 0.44	ĪNT	3.7	16	3.7	12.9		
^t PHL	TCKI↑	INI	5.5	15	5.5	13.1	ns	
^t PHL	TCKI↑	RDY	4.4	15	4.4	13.4	ns	
^t PLH	TCKI↑	TCKO	3.3	17	3.3	14.1	ns	
^t PLH	TOVI	TOVO	2.3	19	2.3	15.9		
^t PHL	TCKI↓	TCKO	3.6	17	3.6	15.6	ns	
^t PLH	TCKI↓	TDO	2.9	19	2.9	17.5		
^t PHL	ICKI↓	TDO	5.2	20	5.2	17.9	ns	
^t PLH	TOKI	TNO	3.1	19	3.1	17.5		
^t PHL	TCKI↓	TMS	5.1	19	5.1	18.2	ns	
^t PLH	TOM	T140/51/51/T	1.5	19	1.5	17.5		
^t PHL	TCKI↓	TMS/EVENT	3.5	20	3.5	18.9	ns	
^t PZH	=-	5.474	3.8	21	3.8	17.6		
^t PZL	RD↓	DATA	6.8	28	6.8	22.6	ns	
		ĪNT	4.9	19	4.9	15.3		
^t PZH	TCKI↑	RDY	3.6	19	3.6	15.3	ns	
^t PZH	TOM	T01/0	4.1	23	4.1	19.2		
t _{PZL}	TCKI↓	тско	4.8	20	4.8	17.4	ns	
^t PZH	TOKAL	TDO	4.3	22	4.3	19.5		
tPZL	TCKI↓	TDO	5	20	5	17.7	ns	
^t PZH	TOW	T140	4.6	23	4.6	19.9		
^t PZL	TCKI↓	TMS	5.1	20	5.1	18.5	ns	
^t PZH	TOKI	TMO/EN/ENIT	2	21	2	18.8		
^t PZL	TCKI↓	TMS/EVENT	3.2	20	3.2	18.7	ns	
^t PZH	^	TO//O	4.6	16	4.6	12.2		
t _{PZL}	TOFF↑	ТСКО	3.1	14	3.1	10.3	ns	
^t PZH		TDO	4.4	15	4.4	12.2		
t _{PZL}	TOFF↑	TDO	3.5	14	3.5	10.8	ns	
^t PZH		TMC	3.1	16.2	3.1	14.7		
t _{PZL}	IOFF	TMS	1.9	16.7	1.9	13.6	ns	



SN54ACT8990, SN74ACT8990 **TEST-BUS CONTROLLERS**

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 16-BIT GENERIC HOST INTERFACES SCAS190E – JUNE 1990 – REVISED JANUARY 1997

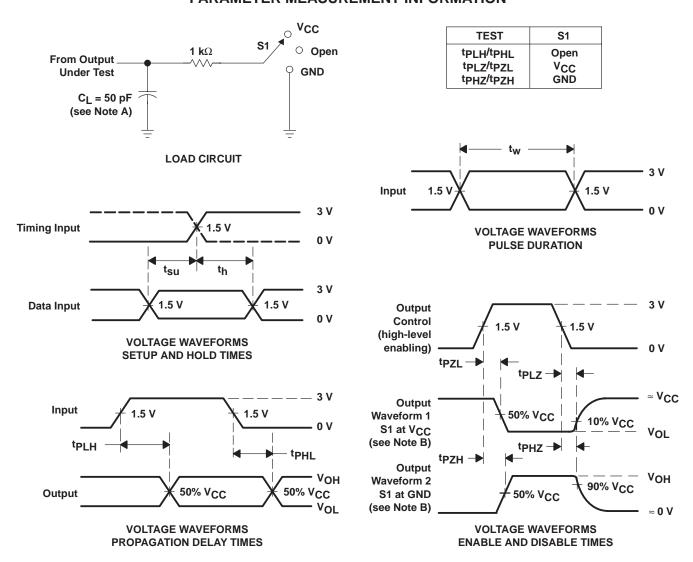
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (continued) (see Figure 1)

DADAMETED	FROM	ТО	SN54A	CT8990	SN74A	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	I UNII
^t PZH		TMC/EV/ENIT	2.3	15.3	2.3	13.8	
^t PZL	TOFF [↑]	TMS/EVENT	2.7	16.4	2.7	13.9	ns
^t PHZ	 RD↑	DATA	3.8	18.4	3.8	15.4	
tPLZ	RDI	DATA	4.1	17.1	4.1	14.8	ns
^t PHZ	TOVI	TOVO	6.7	20.4	6.7	19.8	
t _{PLZ}	TCKI↓	ТСКО	4.8	21.1	4.8	20.4	ns
^t PHZ	TCKI↓	TDO	5.1	21.7	5.1	21.3	
^t PLZ	ICKI↓	100	5	20.7	5	20.3	ns
^t PHZ	TOVI	TMC	6.9	22.4	6.9	21.9	
^t PLZ	TCKI↓	TMS	4.6	20.6	4.6	20.1	ns
^t PHZ	TOVI	TMC/EV/ENIT	4.7	22.5	4.7	22.1	
^t PLZ	TCKI↓	TMS/EVENT	2.8	20.5	2.8	20.1	ns
^t PHZ	U7	TOVO	5	15.6	5	15.4	ns
t _{PLZ}	TOFF↓	ТСКО	4.4	15.5	4.4	15.3	
^t PHZ	====	TDO	5.6	16.6	5.6	16.5	ns
^t PLZ	TOFF↓	TDO	4.6	15.4	4.6	15.4	
^t PHZ	====	TAAC	4.8	19.1	4.8	17.1	
t _{PLZ}	TOFF↓	TMS	4.4	17	4.4	15.8	ns
^t PHZ		T140/F1/F11T	4.5	18.8	4.5	17.3	
t _{PLZ}	TOFF↓	TMS/EVENT	2.4	17.1	2.4	16.2	ns
^t PHZ		DATA	5.7	23	5.7	20.8	
^t PLZ	TRST↓	DATA	4.2	20.3	4.2	20	ns
^t PHZ			6	19.6	8	19.5	T
^t PLZ	TRST↓	ĪNT	6.1	18	6.1	17.8	ns
^t PHZ			6.5	18.8	6.5	18.7	
t _{PLZ}	TRST↓	RDY	4.8	17.8	4.8	17.8	ns
^t PHZ	TD0T	TAAO/EV/ENIT	6	21.1	6	21.1	ns
t _{PLZ}	TRST↓	TMS/EVENT	4.2	20	4.2	19.9	



SCAS190E - JUNE 1990 - REVISED JANUARY 1997

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns, $t_f \leq 3$ ns. For testing pulse duration: $t_r = t_f = 1$ to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





w.ti.com 5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9322801MXA	ACTIVE	CFP	HV	68	1	TBD	Call TI	Call TI	
5962-9322801MYA	ACTIVE	CPGA	GB	68	1	TBD	Call TI	Call TI	
SN74ACT8990FN	ACTIVE	PLCC	FN	44	26	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
SN74ACT8990FNR	ACTIVE	PLCC	FN	44	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
SNJ54ACT8990GB	ACTIVE	CPGA	GB	68	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ACT8990HV	ACTIVE	CFP	HV	68	1	TBD	Call TI	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





www.ti.com 5-Sep-2011

OTHER QUALIFIED VERSIONS OF SN54ACT8990, SN74ACT8990:

◆ Catalog: SN74ACT8990

Military: SN54ACT8990

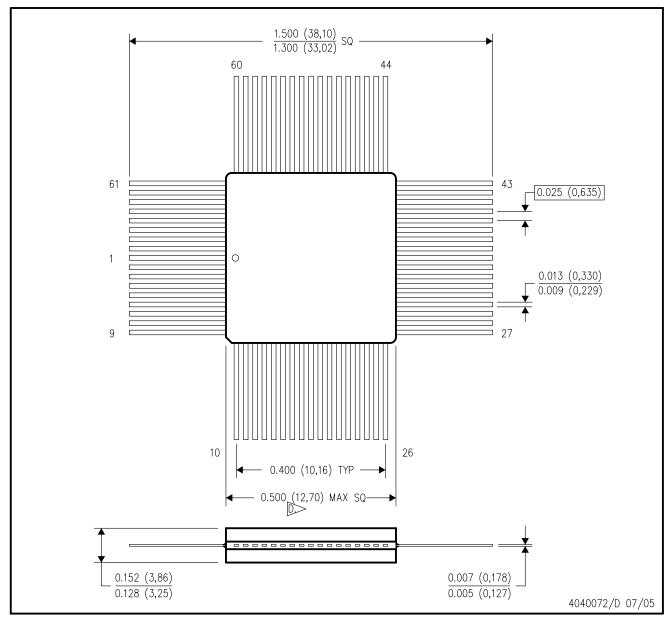
NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

HV (S-GQFP-F68)

CERAMIC QUAD FLATPACK



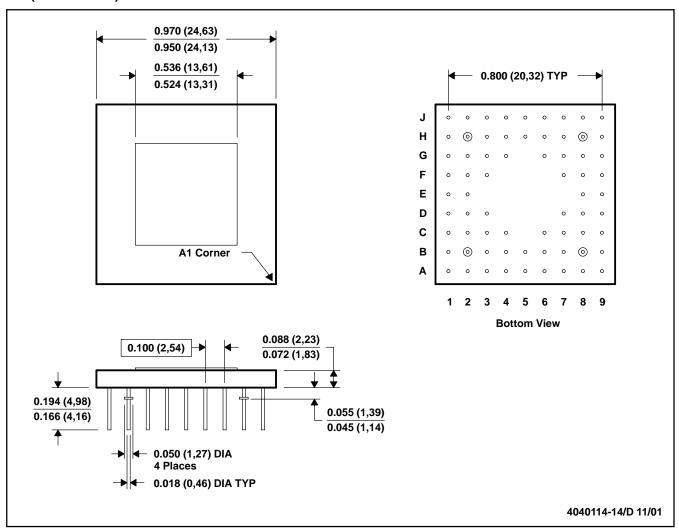
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- This dimension allows for package edge anomalies caused by material protrusion, such as rough ceramic, misaligned ceramic layers and lids, meniscus, and glass overrun.



GB (S-CPGA-P68)

CERAMIC PIN GRID ARRAY



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Index mark may appear on top or bottom depending vendor.
 - D. Pins are located within 0.010 (0,25) diameter of true position relative to each other at maximum material condition and within 0.030 (0,76) diameter relative to the edges of the ceramic.
 - E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
 - F. The pins can be gold plated or solder dipped.
 - G. Falls within MIL STD 1835 CMGA1-PN, CMGA13-PN and JEDEC MO-067 AA, MO-066 AA respectively

FN (S-PQCC-J**)

20 PIN SHOWN

PLASTIC J-LEADED CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-018



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Applications

interface.ti.com

Audio www.ti.com/audio Communications and Telecom www.ti.com/communications **Amplifiers** amplifier.ti.com Computers and Peripherals www.ti.com/computers dataconverter.ti.com Consumer Electronics www.ti.com/consumer-apps **Data Converters DLP® Products** www.dlp.com **Energy and Lighting** www.ti.com/energy DSP dsp.ti.com Industrial www.ti.com/industrial Clocks and Timers www.ti.com/clocks Medical www.ti.com/medical

Logic logic.ti.com Space, Avionics and Defense www.ti.com/space-avionics-defense

Security

Power Mgmt power.ti.com Transportation and Automotive www.ti.com/automotive

Microcontrollers microcontroller.ti.com Video and Imaging www.ti.com/video

RFID <u>www.ti-rfid.com</u>

OMAP Mobile Processors www.ti.com/omap

Interface

Wireless Connctivity www.ti.com/wirelessconnectivity

TI E2E Community Home Page <u>e2e.ti.com</u>

www.ti.com/security