

FEATURES DGG OR DGV PACKAGE Member of the Texas Instruments Widebus™ (TOP VIEW) Family OEAB 56 CEAB **UBT™** Transceiver Combines D-Type Latches 1 55 CLKAB LEAB and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, and A1 | 3 54 🛛 B1 GND 4 53 GND **Clock-Enabled Modes** A2 5 52 B2 **TI-OPC™** Circuitry Limits Ringing on . A3 🛛 6 51 🛛 B3 **Unevenly Loaded Backplanes** 50 BIAS V<sub>CC</sub> V<sub>CC</sub> 7 OEC<sup>™</sup> Circuitry Improves Signal Integrity and 49 🛛 B4 A4 8 **Reduces Electromagnetic Interference** 48 B5 A5 🛛 9 **Bidirectional Interface Between GTLP Signal** 47 B6 A6 10 Levels and LVTTL Logic Levels 46 GND GND 11 **LVTTL Interfaces Are 5-V Tolerant** 45 🛛 B7 A7 🛛 12 Medium-Drive GTLP Outputs (50 mA) 44**1** B8 A8 13 43 🛛 B9 A9 14 LVTTL Outputs (-24 mA/24 mA) A10 15 42 B10 **GTLP** Rise and Fall Times Designed for A11 16 41 B11 **Optimal Data-Transfer Rate and Signal** 40 B12 A12 17 Integrity in Distributed Loads 39 GND GND | 18 I<sub>off</sub>, Power-Up 3-State, and BIAS V<sub>CC</sub> Support . 38 🛛 B13 A13 19 Live Insertion A14 20 37 B14 **Bus Hold on A-Port Data Inputs** 36 B15 A15 21 Distributed V<sub>CC</sub> and GND Pins Minimize V<sub>CC</sub> 22 35 V<sub>RFF</sub> **High-Speed Switching Noise** A16 23 34 B16 Latch-Up Performance Exceeds 100 mA Per A17 24 33 B17 JESD 78, Class II GND 25 32 GND A18 26 31 B18 ESD Protection Exceeds JESD 22 30 CLKBA OEBA 27 - 2000-V Human-Body Model (A114-A) 29 CEBA LEBA 28 - 200-V Machine Model (A115-A) - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

The SN74GTLPH16912 is a medium-drive, 18-bit UBT™ transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It allows for transparent, latched, clocked, and clock-enabled modes of data transfer. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH16912 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL ( $V_{TT} = 1.2$  V and  $V_{RFF} = 0.8$  V) or GTLP  $(V_{TT} = 1.5 \text{ V and } V_{RFF} = 1 \text{ V})$  signal levels.



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## **DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs.  $V_{REF}$  is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using  $I_{off}$ , power-up 3-state, and BIAS  $V_{CC}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS  $V_{CC}$  circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V<sub>CC</sub> is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ( $\overline{OE}$ ) input should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH16912GR	GTLPH16912
	TVSOP – DGV	Tape and reel	SN74GTLPH16912VR	GL912

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTIONAL DESCRIPTION

The SN74GTLPH16912 is a medium-drive (50-mA), 18-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, clocked, or clock-enabled modes and can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH16912 UBT Transceiver Replacement Functions
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FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	'245, '623, '645	'863	'861	'16245, '16623	'16863
Buffer/driver	'241, '244, '541		'827	'16241, '16244, '16541	'16825
Latched transceiver	'543			'16543	'16472
Latch	'373, '573	'843	'841	'16373	'16843
Registered transceiver	'646, '652			'16646, '16652	'16474
Flip-flop	'374, '574		'821	'16374	
Standard UBT					'16500, '16501
Universal bus driver					'16835
Registered transceiver with clock enable	'2952			'16470, '16952	
Flip-flop with clock enable	'377	'823			'16823
Standard UBT with clock enable					'16600, '16601

Data flow in each direction is controlled by clock enables (CEAB and CEBA), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA), and output enables (OEAB and OEBA). CEAB and CEBA and OEAB and OEBA control the 18 bits of data for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow, when CEAB is low, the device operates on the low-to-high transition of CLKAB for the flip-flop and on the high-to-low transition of LEAB for the latch path, i.e., if CEAB and LEAB are low, the A data is latched, regardless of the state of CLKAB (high or low). If LEAB is high, the device is in transparent mode. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to that of A to B, except CEBA, OEBA, LEBA, and CLKBA are used.

INPUTS				OUTPUT	MODE	
CEAB	OEAB	LEAB	CLKAB	Α	В	MODE
Х	Н	Х	Х	Х	Z	Isolation
L	L	L	Н	Х	B <sub>0</sub> <sup>(2)</sup>	Latabad storage of A data
L	L	L	L	Х	B <sub>0</sub> <sup>(3)</sup>	Latched storage of A data
Х	L	Н	Х	L	L	
Х	L	н	Х	н	н	True transparent
L	L	L	$\uparrow$	L	L	Clashed starsge of A data
L	L	L	$\uparrow$	н	н	Clocked storage of A data
Н	L	L	Х	Х	B <sub>0</sub> <sup>(3)</sup>	Clock inhibit

#### FUNCTION TABLE<sup>(1)</sup>

(1) A-to-B data flow is shown. B-to-A data flow is similar, but uses CEBA, OEBA, LEBA, and CLKBA. The condition when OEAB and OEBA are both low at the same time is not recommended.

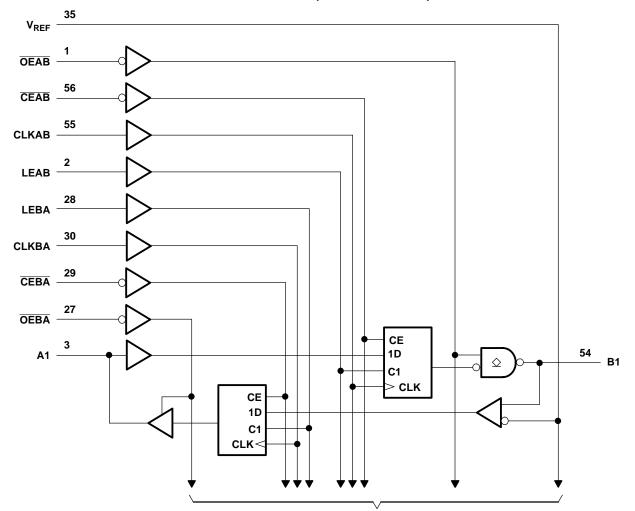
(2) Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

(3) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)

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## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub> BIAS V <sub>CC</sub>	Supply voltage range		-0.5	4.6	V
M	Input voltage range (2)	A-port and control inputs	-0.5	7	V
VI	Input voltage range <sup>(2)</sup>	B port and V <sub>REF</sub>	-0.5	4.6	v
M	Voltage range applied to any output in the	A port	-0.5	7	V
Vo	high-impedance or power-off state	B port	-0.5	4.6	v
1		A port		48	
lo	Current into any output in the low state	B port		100	mA
I <sub>O</sub>	Current into any A-port output in the high state	(3)		48	mA
	Continuous current through each $V_{CC}$ or GND			±100	mA
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
0	Declare the much impedance (4)	DGG package		64	0000
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGV package		48	°C/W
T <sub>stg</sub>	Storage temperature range	· ·	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating" conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(2)

(3) (4)

This current flows only when the output is in the high state and  $V_0 > V_{CC}$ . The package thermal impedance is calculated in accordance with JESD 51-7.

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## Recommended Operating Conditions<sup>(1)(2)(3)(4)</sup>

			MIN	NOM	MAX	UNIT
V <sub>CC</sub> BIAS V <sub>CC</sub>	Supply voltage		3.15	3.3	3.45	V
V	Termination voltage	GTL	1.14	1.2	1.26	V
V <sub>TT</sub>	remination voltage	GTLP	1.35	1.5	1.65	v
M		GTL	0.74	0.8	0.87	V
V <sub>REF</sub>	Reference voltage	GTLP	0.87	1	1.1	V
N/		B port			V <sub>TT</sub>	V
VI	Input voltage	Except B port		V <sub>CC</sub>	5.5	V
N/		B port	V <sub>REF</sub> + 0.05			V
V <sub>IH</sub>	High-level input voltage	Except B port	2			V
M		B port			V <sub>REF</sub> – 0.05	V
V <sub>IL</sub>	Low-level input voltage	Except B port			0.8	V
I <sub>IK</sub>	Input clamp current				–18	mA
I <sub>OH</sub>	High-level output current	A port			-24	mA
	Level and a dead assessed	A port			24	
I <sub>OL</sub>	Low-level output current	w-level output current B port			50	mA
$\Delta t / \Delta V$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t / \Delta V_{CC}$	Power-up ramp rate		20			μs/V
T <sub>A</sub>	Operating free-air temperature		-40		85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS  $V_{CC} = 3.3 \text{ V}$  first, I/O second, and  $V_{CC} = 3.3 \text{ V}$  last, because the BIAS  $V_{CC}$  precharge circuitry is disabled when any  $V_{CC}$  pin is connected. The control and  $V_{REF}$  inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is (2) acceptable, but generally, GND is connected first.

(3)  $V_{TT}$  and  $R_{TT}$  can be adjusted to accommodate backplane impedances if the dc recommended  $I_{OL}$  ratings are not exceeded. (4)  $V_{REF}$  can be adjusted to optimize noise margins, but normally is two-thirds  $V_{TT}$ . TI-OPC circuitry is enabled in the A-to-B direction and is activated when  $V_{TT} > 0.7$  V above  $V_{REF}$ . If operated in the A-to-B direction,  $V_{REF}$  should be set to within 0.6 V of  $V_{TT}$  to minimize current drain.

### **Electrical Characteristics**

over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>IK</sub>		V <sub>CC</sub> = 3.15 V,	I <sub>I</sub> = -18 mA			-1.2	V	
		V <sub>CC</sub> = 3.15 V to 3.45 V,	I <sub>OH</sub> = −100 μA	V <sub>CC</sub> – 0.2				
V <sub>OH</sub>	A port	N 045 V	I <sub>OH</sub> = -12 mA	2.4			V	
		V <sub>CC</sub> = 3.15 V	I <sub>OH</sub> = -24 mA	2				
		V <sub>CC</sub> = 3.15 V to 3.45 V,	I <sub>OL</sub> = 100 μA			0.2		
	A port	N 045 V	I <sub>OL</sub> = 12 mA			0.4		
		V <sub>CC</sub> = 3.15 V	I <sub>OL</sub> = 24 mA			0.5		
V <sub>OL</sub>		$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V},$	I <sub>OL</sub> = 100 μA			0.2	V	
	Dinart		I <sub>OL</sub> = 10 mA			0.2		
	B port	V <sub>CC</sub> = 3.15 V	I <sub>OL</sub> = 40 mA			0.4		
			I <sub>OL</sub> = 50 mA			0.55		
A	A-port and		$V_{I} = 0 \text{ or } V_{CC}$			±10	0	
<sub> </sub> (2)		V <sub>CC</sub> = 3.45 V	V <sub>I</sub> = 5.5 V			±20	μA	
	B port	_	V <sub>I</sub> = 0 to 1.5 V			±10		
BHL <sup>(3)</sup>	A port	V <sub>CC</sub> = 3.15 V,	V <sub>I</sub> = 0.8 V	75			μΑ	
внн <sup>(4)</sup>	A port	V <sub>CC</sub> = 3.15 V,	V <sub>1</sub> = 2 V	-75			μΑ	
BHLO <sup>(5)</sup>	A port	V <sub>CC</sub> = 3.45 V,	$V_{I} = 0$ to $V_{CC}$	500			μA	
BHHO <sup>(6)</sup>	A port	V <sub>CC</sub> = 3.45 V,	$V_{I} = 0$ to $V_{CC}$	-500			μΑ	
		$V_{CC} = 3.45 \text{ V}, I_{C} = 0,$	Outputs high			50		
cc	A or B port	$V_{I}$ (A-port or control input) = $V_{CC}$ or GND,	Outputs low			50	mA	
	$V_1$ (B port) = $V_{TT}$ or GND		Outputs disabled			50		
∆I <sub>CC</sub> <sup>(7)</sup>	·	$V_{CC}$ = 3.45 V, One A-port or control input at V Other A-port or control inputs at V <sub>CC</sub> or GND	/ <sub>CC</sub> – 0.6 V,			1.5	mA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3.15 V or 0			4	5.5	pF	
<u>^</u>	A port	V <sub>O</sub> = 3.15 V or 0			7	8.5	- 5	
C <sub>io</sub>	B port	$V_{0} = 1.5 \text{ V or } 0$			8.5	9.5	pF	

 All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.
For I/O ports, the parameter I<sub>I</sub> includes the off-state output leakage current.
The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub>max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to  $V_{\text{IL}}\text{max}.$ 

(4) The bus-hold circuit can source at least the minimum high sustaining current at VIHmin. IBHH should be measured after raising VIN to VCC and then lowering it to  $V_{\text{IH}}\text{min.}$ 

An external driver must source at least  $I_{BHLO}$  to switch this node from low to high. An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low. (5)

(6)

This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND. (7)

#### **Hot-Insertion Specifications for A Port**

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS				UNIT
I <sub>off</sub>	$V_{CC} = 0,$	BIAS $V_{CC} = 0$ ,	$V_1 \text{ or } V_0 = 0 \text{ to } 5.5 \text{ V}$		10	μΑ
I <sub>OZPU</sub>	$V_{CC} = 0$ to 1.5 V,	$V_{O}$ = 0.5 V to 3 V,	$\overline{OE} = 0$		±30	μΑ
I <sub>OZPD</sub>	$V_{CC} = 1.5 V \text{ to } 0,$	$V_0 = 0.5 V$ to 3 V,	$\overline{OE} = 0$		±30	μΑ

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### Live-Insertion Specifications for B Port

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I <sub>off</sub>	$V_{CC} = 0,$	BIAS $V_{CC} = 0$ ,	$V_1 \text{ or } V_0 = 0 \text{ to } 1.5 \text{ V}$		10	μA
I <sub>OZPU</sub>	$V_{CC} = 0$ to 1.5 V,	BIAS $V_{CC} = 0$ ,	$V_{O} = 0.5 \text{ V to } 1.5 \text{ V}, \overline{OE} = 0$		±30	μA
I <sub>OZPD</sub>	V <sub>CC</sub> = 1.5 V to 0,	BIAS $V_{CC} = 0$ ,	$V_{O} = 0.5 \text{ V to } 1.5 \text{ V}, \overline{OE} = 0$		±30	μA
	V <sub>CC</sub> = 0 to 3.15 V		V <sub>O</sub> (B port) = 0 to 1.5 V	5	mA	
$I_{CC}$ (BIAS $V_{CC}$ )	$V_{CC}$ = 3.15 V to 3.45 V	BIAS $V_{CC}$ = 3.15 V to 3.45 V,	$v_0$ (B poin) = 0 to 1.5 v		10	μA
Vo	$V_{CC} = 0,$	BIAS $V_{CC}$ = 3.3 V,	$I_{O} = 0$	0.95	1.05	V
Ι <sub>Ο</sub>	$V_{CC} = 0,$	BIAS $V_{CC}$ = 3.15 V to 3.45 V,	$V_O$ (B port) = 0.6 V	-1		μA

### **Timing Requirements**

over recommended ranges of supply voltage and operating free-air temperature,  $V_{\rm TT}$  = 1.5 V and  $V_{\rm REF}$  = 1 V for GTLP (unless otherwise noted)

			MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency			175	MHz
	Pulse duration	LEAB or LEBA high	2.8		
t <sub>w</sub>	Pulse duration	CLKAB or CLKBA high or low	2.8		ns
		A before CLKAB↑	1.8		
		B before CLKBA↑	1.5		
	Setup time	A before LEAB↓	1		ns
t <sub>su</sub>		B before LEBA↓	2		
		CEAB before CLKAB↑	1.5		
		CEBA before CLKBA↑	1.4		
		A after CLKAB↑	0.3		
		B after CLKBA↑	0.4		
t <sub>h</sub> Hold time		A after LEAB↓	1.1		
	Hold time	B after LEBA↓	0.4		ns
		CEAB after CLKAB↑	1		
		CEBA after CLKBA↑	1		

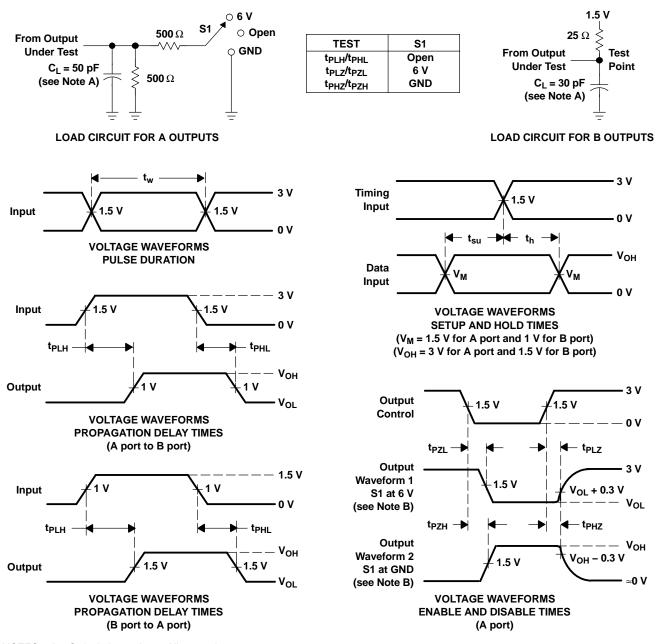
## **Switching Characteristics**

over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT}$  = 1.5 V and  $V_{REF}$  = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN TY	P <sup>(1)</sup> MAX	UNIT
f <sub>max</sub>			175		MHz
t <sub>PLH</sub>	А	В	2.1	6	-
t <sub>PHL</sub>	A	D	2.1	6	ns
t <sub>PLH</sub>		В	2.2	6.3	20
t <sub>PHL</sub>	LEAB	D	2.2	6.3	ns
t <sub>PLH</sub>		D	2.2	6.5	20
t <sub>PHL</sub>	– CLKAB	В	2.2	6.5	ns
t <sub>en</sub>		В	2	6.5	20
t <sub>dis</sub>	OEAB	D	2	6.1	ns
t <sub>r</sub>	Rise time, B outp	uts (20% to 80%)		2.4	
t <sub>f</sub>	Fall time, B output	uts (80% to 20%)		2	ns
t <sub>PLH</sub>	В		1.8	5.8	~~~
t <sub>PHL</sub>	В	А	1.8	5.8	ns
t <sub>PLH</sub>		۸	0.4	5.3	20
t <sub>PHL</sub>	LEBA	А	0.4	5.3	ns
t <sub>PLH</sub>		۸	0.6	5.6	20
t <sub>PHL</sub>	CLKBA	А	0.6	5.7	ns
t <sub>en</sub>	OEBA	۸	0.3	6.2	
t <sub>dis</sub>	OEBA	А	0.3	5.9	ns

(1) All typical values are at V\_{CC} = 3.3 V, T\_A = 25 ^{\circ}C.

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PARAMETER MEASUREMENT INFORMATION

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

- Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\approx$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\approx$  2 ns, t<sub>f</sub>  $\approx$  2 ns.

D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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#### Distributed-Load Backplane Switching Characteristics

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

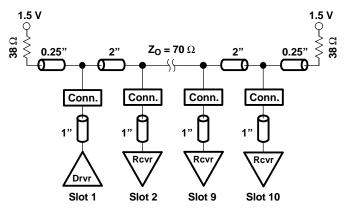


Figure 2. Medium-Drive Test Backplane

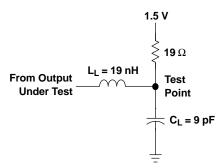


Figure 3. Medium-Drive RLC Network

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#### **Switching Characteristics**

over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT}$  = 1.5 V and  $V_{REF}$  = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP <sup>(1)</sup>	UNIT
t <sub>PLH</sub>	٨	В	4.5	20
t <sub>PHL</sub>	A	D	4.5	ns
t <sub>PLH</sub>		D	4.7	20
t <sub>PHL</sub>	LEAD	LEAB B -	4.7	ns
t <sub>PLH</sub>		R	4.7	20
t <sub>PHL</sub>	CLKAB B	4.7	ns	
t <sub>en</sub>	OFAR	В	4.8	20
t <sub>dis</sub>	OEAB	D	4.4	ns
t <sub>r</sub>	Rise time, B outputs (20% to 80%)			ns
t <sub>f</sub>	Fall time, B output	ts (80% to 20%)	2.5	ns

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C. All values are derived from TI-SPICE models.





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### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
74GTLPH16912GRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74GTLPH16912GRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH16912GR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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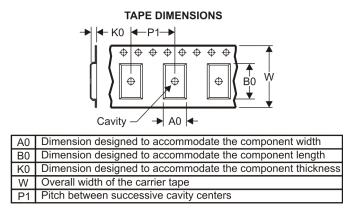
# PACKAGE MATERIALS INFORMATION

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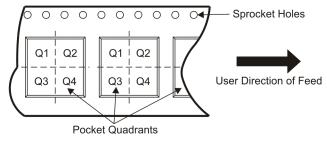
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### TAPE AND REEL INFORMATION





### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	

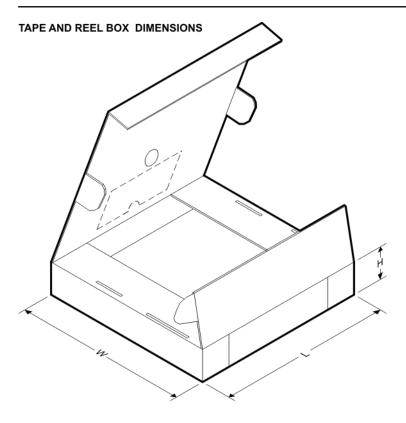
Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTLPH16912GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TEXAS INSTRUMENTS

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29-Jul-2011



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTLPH16912GR	TSSOP	DGG	56	2000	346.0	346.0	41.0

## **MECHANICAL DATA**

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

#### DGG (R-PDSO-G\*\*)

### PLASTIC SMALL-OUTLINE PACKAGE

**48 PINS SHOWN** 



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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